

# TGU968

COM Express Compact Module  
User's Manual

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## COM Express Specification Reference

PICMG® COM Express® Module Base Specification.  
<http://www.picmg.org/>

## FCC and DOC Statement on Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio TV technician for help.

## Notice:

- The changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.
- Shielded interface cables must be used in order to comply with the emission limits.

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## About this Manual

This manual can be downloaded from the website.

The manual is subject to change and update without notice, and may be based on editions that do not resemble your actual products. Please visit our website or contact our sales representatives for the latest editions.

## Warranty

- Warranty does not cover damages or failures that occur from misuse of the product, inability to use the product, unauthorized replacement or alteration of components and product specifications.
- The warranty is void if the product has been subjected to physical abuse, improper installation, modification, accidents or unauthorized repair of the product.
- Unless otherwise instructed in this user's manual, the user may not, under any circumstances, attempt to perform service, adjustments or repairs on the product, whether in or out of warranty. It must be returned to the purchase point, factory or authorized service agency for all such work.
- We will not be liable for any indirect, special, incidental or consequential damages to the product that has been modified or altered.

## Static Electricity Precautions

It is quite easy to inadvertently damage your PC, system board, components or devices even before installing them in your system unit. Static electrical discharge can damage computer components without causing any signs of physical damage. You must take extra care in handling them to ensure against electrostatic build-up.

- To prevent electrostatic build-up, leave the system board in its anti-static bag until you are ready to install it.
- Wear an antistatic wrist strap.
- Do all preparation work on a static-free surface.
- Hold the device only by its edges. Be careful not to touch any of the components, contacts or connections.
- Avoid touching the pins or contacts on all modules and connectors. Hold modules or connectors by their ends.



### Important:

Electrostatic discharge (ESD) can damage your processor, disk drive and other components. Perform the upgrade instruction procedures described at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

## Safety Measures

- To avoid damage to the system, use the correct AC input voltage range.
- To reduce the risk of electric shock, unplug the power cord before removing the system chassis cover for installation or servicing. After installation or servicing, cover the system chassis before plugging the power cord.

## About the Package

The package contains the following items. If any of these items are missing or damaged, please contact your dealer or sales representative for assistance.

- 1 TGU968 board

## Optional Items

The board and accessories in the package may not come similar to the information listed above. This may differ in accordance with the sales region or models in which it was sold. For more information about the standard package in your region, please contact your dealer or sales representative.

## Before Using the System Board

Before using the system board, prepare basic system components.

If you are installing the system board in a new system, you will need at least the following internal components.

- Storage devices such as hard disk drive, etc.

You will also need external system peripherals you intend to use which will normally include at least a keyboard, a mouse and a video display monitor.

## Chapter 1 - Introduction

### ► Specifications

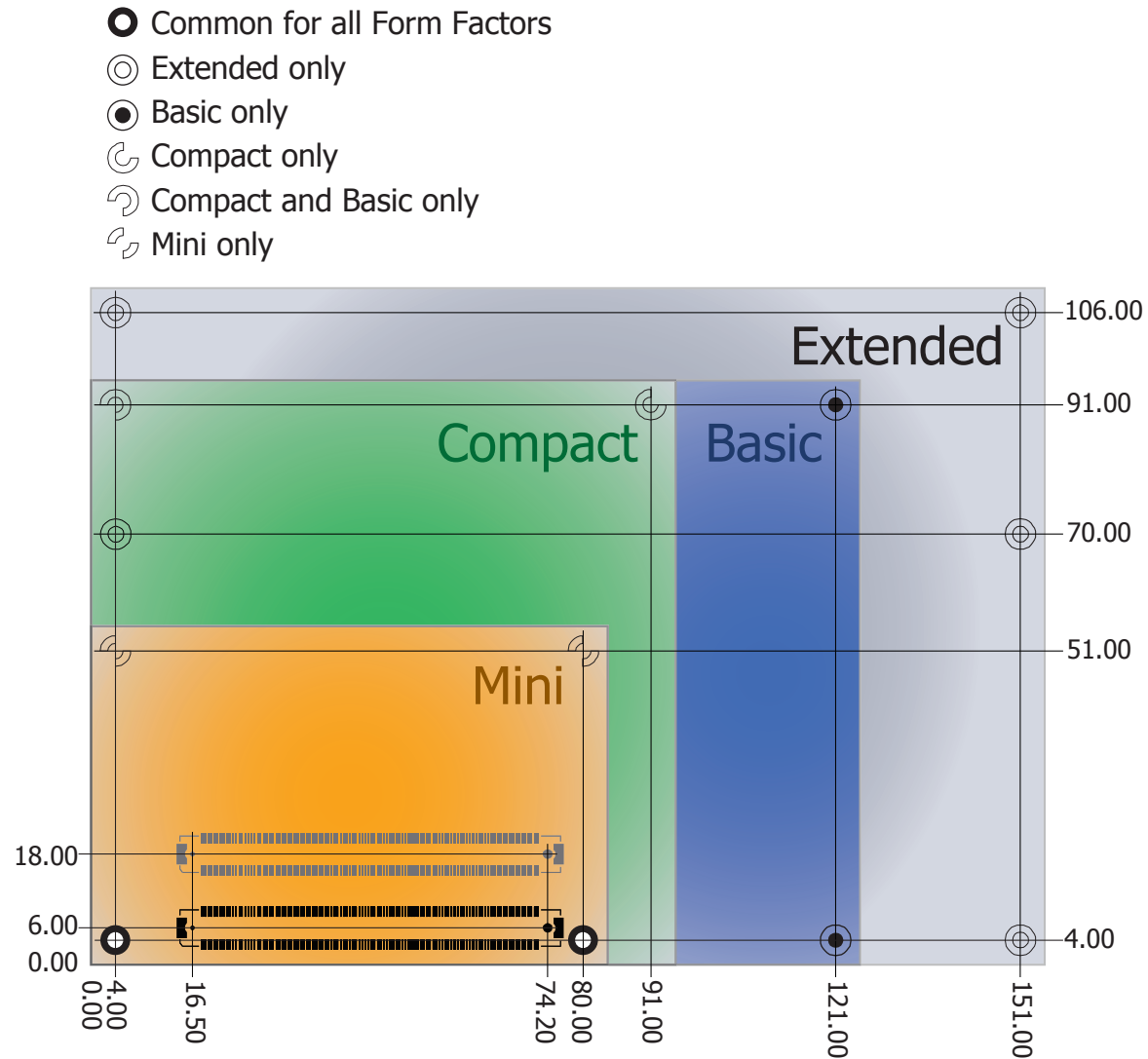
<b>SYSTEM</b>	<b>Processor</b>	Intel® Core™ i7-1185G7E Processor (Core 4; Max speed 2.8 GHz; TDP 15-28W) Intel® Core™ i7-1185GRE Processor (Core 4; Max speed 2.8 GHz; TDP 15-28W) Support In-band ECC Intel® Core™ i5-1145G7E Processor (Core 4; Max speed 2.6 GHz; TDP 15-28W) Intel® Core™ i5-1145GRE Processor (Core 4; Max speed 2.6 GHz; TDP 15-28W) Support In-band ECC Intel® Core™ i3-1115G4E Processor (Core 2; Max speed 3.0 GHz; TDP 15-28W) Intel® Core™ i3-1115GRE Processor (Core 2; Max speed 3.0 GHz; TDP 15-28W) Support In-band ECC Intel® Celeron® 6305E Processor (Core 2; Max speed 1.8 GHz; TDP 15W)
	<b>Memory</b>	Two 260-Pin SO-DIMM up to 64GB, Dual Channel DDR4 2666Mhz
	<b>BIOS</b>	AMI BIOS
	<b>GRAPHICS</b>	<b>Controller</b> Intel® UHD Graphics for 11th Gen Intel® Processors
	<b>Feature</b>	OpenGL 5.0, DirectX 12, OpenCL 2.1 HW Decode: WMV9, AVC/H264, JPEG/MJPEG, HEVC/H265, VP9, AV1 HW Encode: AVC/H264, JPEG, HEVC/H265, VP9
	<b>Display</b>	1 x VGA 1 x LVDS/eDP (eDP available upon request) 3 x DDI * VGA: resolution up to 1920x1200 @ 60Hz * LVDS: dual channel 24-bit, resolution up to 1920x1200 @ 60Hz * eDP: resolution up to 4096x2304 @ 60Hz * HDMI: resolution up to 4096x2160 @ 30Hz * DP++: resolution up to 4096x2304 @ 60Hz
	<b>Triple Displays</b>	VGA + LVDS + DDI DDI + eDP + DDI (available upon request)
<b>EXPANSION</b>	<b>Interface</b>	1 x PCIe x4 (Gen 4) 5 x PCIe x1 (Gen3) (8 x PCIe x1 available upon request) 1 x I2C 1 x SMBus 1 x SPI 2 x UART (TX/RX)
<b>AUDIO</b>	<b>Interface</b>	HD Audio
<b>ETHERNET</b>	<b>Controller</b>	1 x Intel® i226 series (10/100/1000Mbps/2.5G), co-lay PCIe x1 (available upon request)
<b>I/O</b>	<b>USB</b>	4 x USB 3.2 Gen.2 8 x USB 2.0
	<b>SATA</b>	2 x SATA 3.0 (up to 6Gb/s), co-lay PCIe x1 (available upon request)
	<b>NVMe SSD</b>	1 x 64GB/128GB/256GB/512GB/1024GB on board SSD (available upon request)
	<b>DIO</b>	1 x 8-bit DIO

<b>WATCHDOG TIMER</b>	Output & Interval	System Reset, Programmable via Software from 1 to 255 Seconds
<b>SECURITY</b>	TPM	Available Upon Request
<b>Power</b>	Type	8.5~20V, 5VSB, VCC_RTC (ATX mode) 8.5~12V, VCC_RTC (AT mode)
	Consumption	Boot up: i7-1185GRE: 12V @ 2.03A (24.36W); Idle: i7-1185GRE: 12V @ 0.86A (10.2W); Max.: i7-1185GRE: 12V @ 3.35A (40.2W)
<b>OS SUPPORT</b>		Windows: Windows 10 IoT Enterprise 64-bit Linux
<b>ENVIRONMENT</b>	Temperature	Operating: 0 to 60°C, -40 to 85°C Storage: -40 to 85°C
	Humidity	Operating: 10 to 90% RH Storage: 10 to 90% RH
	MTBF	1,083,012 hrs @ 25°C; 730,611 hrs @ 45°C; 513,984 hrs @ 60°C; 398,344 hrs @ 70°C; 266,028 hrs @ 85°C
<b>MECHANICAL</b>	Dimensions	COM Express® Compact 95mm (3.74") x 95mm (3.74")
	Compliance	PICMG COM Express® R3.0, Type 6
<b>STANDARDS AND CERTIFICATIONS</b>	Certification	CE, FCC

## Chapter 2 - Concept

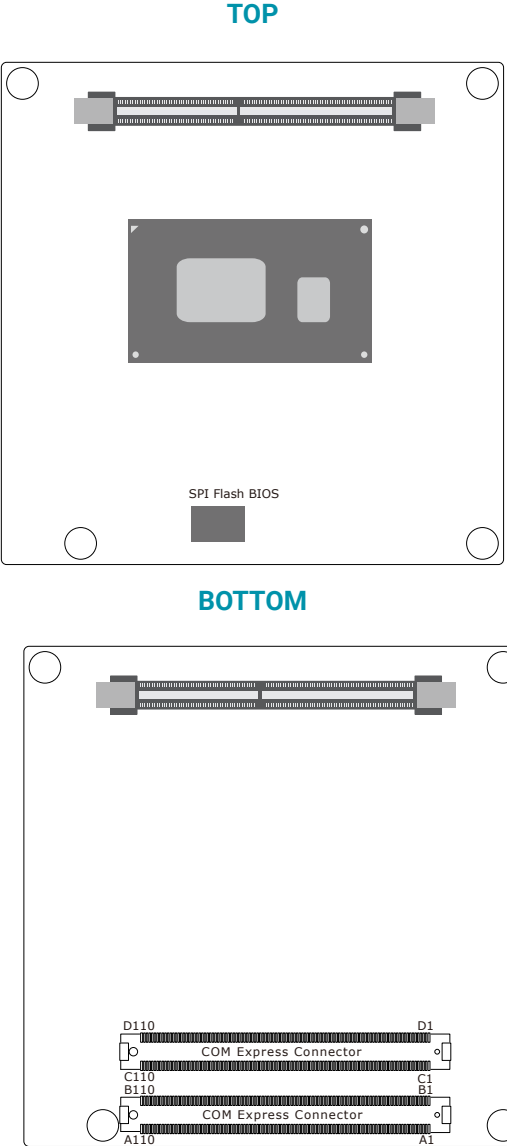
### ► COM Express Module Standards

The figure below shows the dimensions of the different types of COM Express modules. TGU968 is a COM Express Compact. The dimension is 95mm x 95mm.

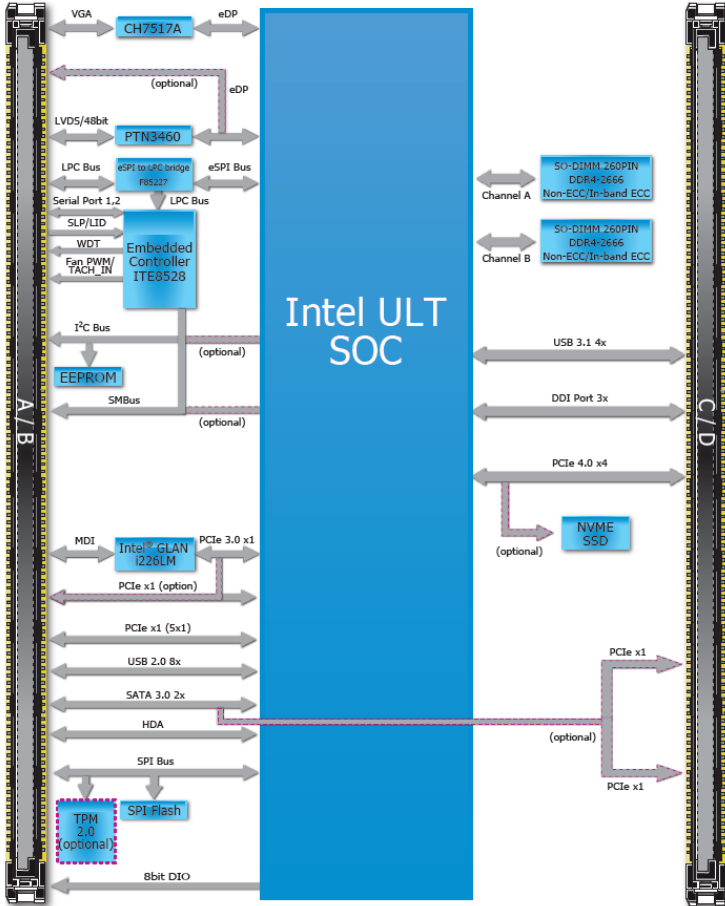


# Chapter 3 - Hardware Installation

## ▶ Board Layout



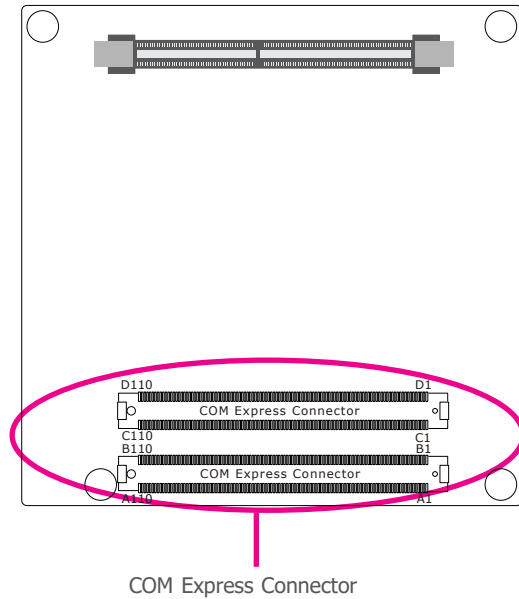
## ▶ Block Diagram



► Connector

COM Express Connector

The COM Express connector is used to interface the TGU968 COM Express board to a carrier board. Connect the COM Express connector (located on the solder side of the board) to the COM Express connector on the carrier board.



Refer to the following pages for the pin functions of the connector.

► COM Express Connector

Row A		Row B	
<b>A1</b>	GND (FIXED)	<b>B1</b>	GND (FIXED)
<b>A2</b>	GBE0_MDI3-	<b>B2</b>	GBE0_ACT#
<b>A3</b>	GBE0_MDI3+	<b>B3</b>	LPC_FRAME#
<b>A4</b>	Note*GBE0_LINK100#	<b>B4</b>	LPC_AD0
<b>A5</b>	Note**GBE0_LINK100#	<b>B5</b>	LPC_AD1
<b>A6</b>	GBE0_MDI2-	<b>B6</b>	LPC_AD2
<b>A7</b>	GBE0_MDI2+	<b>B7</b>	LPC_AD3
<b>A8</b>	GBE0_LINK#	<b>B8</b>	LPC_DRQ0# (NA)
<b>A9</b>	GBE0_MDI1-	<b>B9</b>	LPC_DRQ1# (NA)
<b>A10</b>	GBE0_MDI1+	<b>B10</b>	LPC_CLK
<b>A11</b>	GND (FIXED)	<b>B11</b>	GND (FIXED)
<b>A12</b>	GBE0_MDI0-	<b>B12</b>	PWRBTN#
<b>A13</b>	GBE0_MDI0+	<b>B13</b>	SMB_CK
<b>A14</b>	GBE0_CTREF	<b>B14</b>	SMB_DAT
<b>A15</b>	SUS_S3#	<b>B15</b>	SMB_ALERT#
<b>A16</b>	SATA0_TX+	<b>B16</b>	SATA1_TX+
<b>A17</b>	SATA0_TX-	<b>B17</b>	SATA1_TX-
<b>A18</b>	SUS_S4#	<b>B18</b>	SUS_STAT#
<b>A19</b>	SATA0_RX+	<b>B19</b>	SATA1_RX+
<b>A20</b>	SATA0_RX-	<b>B20</b>	SATA1_RX-
<b>A21</b>	GND (FIXED)	<b>B21</b>	GND (FIXED)
<b>A22</b>	SATA2_TX+ (NA)	<b>B22</b>	SATA3_TX+ (NA)
<b>A23</b>	SATA2_TX- (NA)	<b>B23</b>	SATA3_TX- (NA)
<b>A24</b>	SUS_S5#	<b>B24</b>	PWR_OK
<b>A25</b>	SATA2_RX+ (NA)	<b>B25</b>	SATA3_RX+ (NA)
<b>A26</b>	SATA2_RX- (NA)	<b>B26</b>	SATA3_RX- (NA)
<b>A27</b>	BATLOW#	<b>B27</b>	WDT

Row A		Row B	
<b>A28</b>	(S)ATA_ACT#	<b>B28</b>	NA
<b>A29</b>	AC/HDA_SYNC	<b>B29</b>	AC/HDA_SDIN1
<b>A30</b>	AC/HDA_RST#	<b>B30</b>	AC/HDA_SDIN0
<b>A31</b>	GND (FIXED)	<b>B31</b>	GND (FIXED)
<b>A32</b>	AC/HDA_BITCLK	<b>B32</b>	SPKR
<b>A33</b>	AC/HDA_SDOOUT	<b>B33</b>	I2C_CK
<b>A34</b>	BIOS_DIS0#	<b>B34</b>	I2C_DAT
<b>A35</b>	THRMTrip#	<b>B35</b>	THRM#
<b>A36</b>	USB6-	<b>B36</b>	USB7-
<b>A37</b>	USB6+	<b>B37</b>	USB7+
<b>A38</b>	USB_6_7_OC#	<b>B38</b>	USB_4_5_OC#
<b>A39</b>	USB4-	<b>B39</b>	USB5-
<b>A40</b>	USB4+	<b>B40</b>	USB5+
<b>A41</b>	GND (FIXED)	<b>B41</b>	GND (FIXED)
<b>A42</b>	USB2-	<b>B42</b>	USB3-
<b>A43</b>	USB2+	<b>B43</b>	USB3+
<b>A44</b>	USB_2_3_OC#	<b>B44</b>	USB_0_1_OC#
<b>A45</b>	USB0-	<b>B45</b>	USB1-
<b>A46</b>	USB0+	<b>B46</b>	USB1+
<b>A47</b>	VCC_RTC	<b>B47</b>	EXCD1_PERST#
<b>A48</b>	EXCD0_PERST#	<b>B48</b>	EXCD1_CPPE#
<b>A49</b>	EXCD0_CPPE#	<b>B49</b>	SYS_RESET#
<b>A50</b>	LPC_SERIRQ	<b>B50</b>	CB_RESET#
<b>A51</b>	GND (FIXED)	<b>B51</b>	GND (FIXED)
<b>A52</b>	PCIE_TX5+ (Optional)	<b>B52</b>	PCIE_TX5+ (Optional)
<b>A53</b>	PCIE_TX5- (Optional)	<b>B53</b>	PCIE_TX5- (Optional)
<b>A54</b>	GPIO	<b>B54</b>	GPO1
<b>A55</b>	PCIE_TX4+	<b>B55</b>	PCIE_RX4+

**Note:**  
 1. \*GBE\_LED\_100# is active during a 1Gb connection.  
 2. \*\*GBE\_LED\_1000# is active during a 2.5Gb connection.

Row A		Row B	
<b>A56</b>	PCIE_TX4-	<b>B56</b>	PCIE_RX4-
<b>A57</b>	GND	<b>B57</b>	GPO2
<b>A58</b>	PCIE_TX3+	<b>B58</b>	PCIE_RX3+
<b>A59</b>	PCIE_TX3-	<b>B59</b>	PCIE_RX3-
<b>A60</b>	GND (FIXED)	<b>B60</b>	GND (FIXED)
<b>A61</b>	PCIE_TX2+	<b>B61</b>	PCIE_RX2+
<b>A62</b>	PCIE_TX2-	<b>B62</b>	PCIE_RX2-
<b>A63</b>	GPI1	<b>B63</b>	GPO3
<b>A64</b>	PCIE_TX1+	<b>B64</b>	PCIE_RX1+
<b>A65</b>	PCIE_TX1-	<b>B65</b>	PCIE_RX1-
<b>A66</b>	GND	<b>B66</b>	WAKE0#
<b>A67</b>	GPI2	<b>B67</b>	WAKE1#
<b>A68</b>	PCIE_TX0+	<b>B68</b>	PCIE_RX0+
<b>A69</b>	PCIE_TX0-	<b>B69</b>	PCIE_RX0-
<b>A70</b>	GND(FIXED)	<b>B70</b>	GND (FIXED)
<b>A71</b>	LVDS_A0+/ eDP_TX2+	<b>B71</b>	LVDS_B0+
<b>A72</b>	LVDS_A0-/ eDP_TX2-	<b>B72</b>	LVDS_B0-
<b>A73</b>	LVDS_A1+/ eDP_TX1+	<b>B73</b>	LVDS_B1+
<b>A74</b>	LVDS_A1-/ eDP_TX1-	<b>B74</b>	LVDS_B1-
<b>A75</b>	LVDS_A2+/ eDP_TX0+	<b>B75</b>	LVDS_B2+
<b>A76</b>	LVDS_A2-/ eDP_TX0-	<b>B76</b>	LVDS_B2-
<b>A77</b>	LVDS_VDD_EN /eDP_VDD_EN	<b>B77</b>	LVDS_B3+
<b>A78</b>	LVDS_A3+	<b>B78</b>	LVDS_B3-
<b>A79</b>	LVDS_A3-	<b>B79</b>	LVDS_BKLT_EN /eDP_BKLT_EN
<b>A80</b>	GND (FIXED)	<b>B80</b>	GND (FIXED)
<b>A81</b>	LVDS_A_CK+/eDP_TX3+	<b>B81</b>	LVDS_B_CK+
<b>A82</b>	LVDS_A_CK-/eDP_TX3-	<b>B82</b>	LVDS_B_CK-

Row A		Row B	
<b>A83</b>	LVDS_I2C_CK/eDP_AUX+	<b>B83</b>	LVDS_BKLT_CTRL/eDP_BKLT_CTRL
<b>A84</b>	LVDS_I2C_DAT /eDP_AUX-	<b>B84</b>	VCC_5V_SBY
<b>A85</b>	GPI3	<b>B85</b>	VCC_5V_SBY
<b>A86</b>	RSVD	<b>B86</b>	VCC_5V_SBY
<b>A87</b>	RSVD/eDP_HPD	<b>B87</b>	VCC_5V_SBY
<b>A88</b>	PCIE0_CK_REF+	<b>B88</b>	BIOS_DIS1#
<b>A89</b>	PCIE0_CK_REF-	<b>B89</b>	VGA_RED
<b>A90</b>	GND (FIXED)	<b>B90</b>	GND (FIXED)
<b>A91</b>	SPI_POWER	<b>B91</b>	VGA_GRN
<b>A92</b>	SPI_MISO	<b>B92</b>	VGA_BLU
<b>A93</b>	GPO0	<b>B93</b>	VGA_HSYNC
<b>A94</b>	SPI_CLK	<b>B94</b>	VGA_VSYNC
<b>A95</b>	SPI_MOSI	<b>B95</b>	VGA_I2C_CK
<b>A96</b>	TPM_PP	<b>B96</b>	VGA_I2C_DAT
<b>A97</b>	Type10# (NC)	<b>B97</b>	SPI_CS#
<b>A98</b>	SER0_TX	<b>B98</b>	RSVD
<b>A99</b>	SER0_RX	<b>B99</b>	RSVD
<b>A100</b>	GND (FIXED)	<b>B100</b>	GND (FIXED)
<b>A101</b>	SER1_TX	<b>B101</b>	FAN_PWMOUT
<b>A102</b>	SER1_RX	<b>B102</b>	FAN_TACHIN
<b>A103</b>	LID#	<b>B103</b>	SLEEP#
<b>A104</b>	VCC_8.5V~ 20V	<b>B104</b>	VCC_8.5V~ 20V
<b>A105</b>	VCC_8.5V~ 20V	<b>B105</b>	VCC_8.5V~ 20V
<b>A106</b>	VCC_8.5V~ 20V	<b>B106</b>	VCC_8.5V~ 20V
<b>A107</b>	VCC_8.5V~ 20V	<b>B107</b>	VCC_8.5V~ 20V
<b>A108</b>	VCC_8.5V~ 20V	<b>B108</b>	VCC_8.5V~ 20V
<b>A109</b>	VCC_8.5V~ 20V	<b>B109</b>	VCC_8.5V~ 20V
<b>A110</b>	GND (FIXED)	<b>B110</b>	GND (FIXED)

Row C		Row D	
<b>C1</b>	GND (FIXED)	<b>D1</b>	GND (FIXED)
<b>C2</b>	GND	<b>D2</b>	GND
<b>C3</b>	USB_SSRX0-	<b>D3</b>	USB_SSTX0-
<b>C4</b>	USB_SSRX0+	<b>D4</b>	USB_SSTX0+
<b>C5</b>	GND	<b>D5</b>	GND
<b>C6</b>	USB_SSRX1-	<b>D6</b>	USB_SSTX1-
<b>C7</b>	USB_SSRX1+	<b>D7</b>	USB_SSTX1+
<b>C8</b>	GND	<b>D8</b>	GND
<b>C9</b>	USB_SSRX2-	<b>D9</b>	USB_SSTX2-
<b>C10</b>	USB_SSRX2+	<b>D10</b>	USB_SSTX2+
<b>C11</b>	GND (FIXED)	<b>D11</b>	GND (FIXED)
<b>C12</b>	USB_SSRX3-	<b>D12</b>	USB_SSTX3-
<b>C13</b>	USB_SSRX3+	<b>D13</b>	USB_SSTX3+
<b>C14</b>	GND	<b>D14</b>	GND
<b>C15</b>	DDI1_PAIR6+ (NA)	<b>D15</b>	DDI1_CTRLCLK_AUX+
<b>C16</b>	DDI1_PAIR6- (NA)	<b>D16</b>	DDI1_CTRLDATA_AUX-
<b>C17</b>	RSVD	<b>D17</b>	RSVD
<b>C18</b>	RSVD	<b>D18</b>	RSVD
<b>C19</b>	PCIE_RX6+ (Optional)	<b>D19</b>	PCIE_TX6+ (Optional)
<b>C20</b>	PCIE_RX6- (Optional)	<b>D20</b>	PCIE_TX6- (Optional)
<b>C21</b>	GND (FIXED)	<b>D21</b>	GND (FIXED)
<b>C22</b>	PCIE_RX7+ (Optional)	<b>D22</b>	PCIE_TX7+ (Optional)
<b>C23</b>	PCIE_RX7- (Optional)	<b>D23</b>	PCIE_TX7- (Optional)
<b>C24</b>	DDI1_HPD	<b>D24</b>	RSVD
<b>C25</b>	DDI1_PAIR4+ (NA)	<b>D25</b>	RSVD
<b>C26</b>	DDI1_PAIR4- (NA)	<b>D26</b>	DDI1_PAIR0+
<b>C27</b>	RSVD	<b>D27</b>	DDI1_PAIR0-

Row C		Row D	
<b>C28</b>	RSVD	<b>D28</b>	RSVD
<b>C29</b>	DDI1_PAIR5+ (NA)	<b>D29</b>	DDI1_PAIR1+
<b>C30</b>	DDI1_PAIR5- (NA)	<b>D30</b>	DDI1_PAIR1-
<b>C31</b>	GND (FIXED)	<b>D31</b>	GND (FIXED)
<b>C32</b>	DDI2_CTRLCLK_AUX+	<b>D32</b>	DDI1_PAIR2+
<b>C33</b>	DDI2_CTRLDATA_AUX-	<b>D33</b>	DDI1_PAIR2-
<b>C34</b>	DDI2_DDC_AUX_SEL	<b>D34</b>	DDI1_DDC_AUX_SEL
<b>C35</b>	RSVD	<b>D35</b>	RSVD
<b>C36</b>	DDI3_CTRLCLK_AUX+	<b>D36</b>	DDI1_PAIR3+
<b>C37</b>	DDI3_CTRLDATA_AUX-	<b>D37</b>	DDI1_PAIR3-
<b>C38</b>	DDI2_DDC_AUX_SEL	<b>D38</b>	RSVD
<b>C39</b>	DDI3_PAIR0+	<b>D39</b>	DDI2_PAIR0+
<b>C40</b>	DDI3_PAIR0-	<b>D40</b>	DDI2_PAIR0-
<b>C41</b>	GND (FIXED)	<b>D41</b>	GND (FIXED)
<b>C42</b>	DDI3_PAIR1+	<b>D42</b>	DDI2_PAIR1+
<b>C43</b>	DDI3_PAIR1-	<b>D43</b>	DDI2_PAIR1-
<b>C44</b>	DDI3_HPD	<b>D44</b>	DDI2_HPD
<b>C45</b>	RSVD	<b>D45</b>	RSVD
<b>C46</b>	DDI3_PAIR2+	<b>D46</b>	DDI2_PAIR2+
<b>C47</b>	DDI3_PAIR2-	<b>D47</b>	DDI2_PAIR2-
<b>C48</b>	RSVD	<b>D48</b>	RSVD
<b>C49</b>	DDI3_PAIR3+	<b>D49</b>	DDI2_PAIR3+
<b>C50</b>	DDI3_PAIR3-	<b>D50</b>	DDI2_PAIR3-
<b>C51</b>	GND (FIXED)	<b>D51</b>	GND (FIXED)
<b>C52</b>	PEG_RX0+ (Optional)	<b>D52</b>	PEG_TX0+ (Optional)
<b>C53</b>	PEG_RX0- (Optional)	<b>D53</b>	PEG_TX0- (Optional)
<b>C54</b>	TYPE0# (NC)	<b>D54</b>	PEG_LANE_RV# (Optional)
<b>C55</b>	PEG_RX1+ (Optional)	<b>D55</b>	PEG_TX1+ (Optional)

Row C		Row D	
<b>C56</b>	PEG_RX1- (Optional)	<b>D56</b>	PEG_TX1- (Optional)
<b>C57</b>	TYPE1# (NC)	<b>D57</b>	TYPE2# (GND)
<b>C58</b>	PEG_RX2+ (Optional)	<b>D58</b>	PEG_TX2+ (Optional)
<b>C59</b>	PEG_RX2- (Optional)	<b>D59</b>	PEG_TX2- (Optional)
<b>C60</b>	GND (FIXED)	<b>D60</b>	GND (FIXED)
<b>C61</b>	PEG_RX3+ (Optional)	<b>D61</b>	PEG_TX3+ (Optional)
<b>C62</b>	PEG_RX3- (Optional)	<b>D62</b>	PEG_TX3- (Optional)
<b>C63</b>	RSVD	<b>D63</b>	RSVD
<b>C64</b>	RSVD	<b>D64</b>	RSVD
<b>C65</b>	PEG_RX4+ (NA)	<b>D65</b>	PEG_TX4+ (NA)
<b>C66</b>	PEG_RX4- (NA)	<b>D66</b>	PEG_TX4- (NA)
<b>C67</b>	RAPID_SHUTDOWN	<b>D67</b>	GND
<b>C68</b>	PEG_RX5+ (NA)	<b>D68</b>	PEG_TX5+ (NA)
<b>C69</b>	PEG_RX5- (NA)	<b>D69</b>	PEG_TX5- (NA)
<b>C70</b>	GND (FIXED)	<b>D70</b>	GND (FIXED)
<b>C71</b>	PEG_RX6+ (NA)	<b>D71</b>	PEG_TX6+ (NA)
<b>C72</b>	PEG_RX6- (NA)	<b>D72</b>	PEG_TX6- (NA)
<b>C73</b>	GND	<b>D73</b>	GND
<b>C74</b>	PEG_RX7+ (NA)	<b>D74</b>	PEG_TX7+ (NA)
<b>C75</b>	PEG_RX7- (NA)	<b>D75</b>	PEG_TX7- (NA)
<b>C76</b>	GND	<b>D76</b>	GND
<b>C77</b>	RSVD	<b>D77</b>	RSVD
<b>C78</b>	PEG_RX8+ (NA)	<b>D78</b>	PEG_TX8+ (NA)
<b>C79</b>	PEG_RX8- (NA)	<b>D79</b>	PEG_TX8- (NA)
<b>C80</b>	GND (FIXED)	<b>D80</b>	GND (FIXED)
<b>C81</b>	PEG_RX9+ (NA)	<b>D81</b>	PEG_TX9+ (NA)
<b>C82</b>	PEG_RX9- (NA)	<b>D82</b>	PEG_TX9- (NA)

Row C		Row D	
<b>C83</b>	RSVD	<b>D83</b>	RSVD
<b>C84</b>	GND	<b>D84</b>	GND
<b>C85</b>	PEG_RX10+ (NA)	<b>D85</b>	PEG_TX10+ (NA)
<b>C86</b>	PEG_RX10- (NA)	<b>D86</b>	PEG_TX10- (NA)
<b>C87</b>	GND	<b>D87</b>	GND
<b>C88</b>	PEG_RX11+ (NA)	<b>D88</b>	PEG_TX11+ (NA)
<b>C89</b>	PEG_RX11- (NA)	<b>D89</b>	PEG_TX11- (NA)
<b>C90</b>	GND (FIXED)	<b>D90</b>	GND (FIXED)
<b>C91</b>	PEG_RX12+ (NA)	<b>D91</b>	PEG_TX12+ (NA)
<b>C92</b>	PEG_RX12- (NA)	<b>D92</b>	PEG_TX12- (NA)
<b>C93</b>	GND	<b>D93</b>	GND
<b>C94</b>	PEG_RX13+ (NA)	<b>D94</b>	PEG_TX13+ (NA)
<b>C95</b>	PEG_RX13- (NA)	<b>D95</b>	PEG_TX13- (NA)
<b>C96</b>	GND	<b>D96</b>	GND
<b>C97</b>	RSVD	<b>D97</b>	RSVD
<b>C98</b>	PEG_RX14+ (NA)	<b>D98</b>	PEG_TX14+ (NA)
<b>C99</b>	PEG_RX14- (NA)	<b>D99</b>	PEG_TX14- (NA)
<b>C100</b>	GND (FIXED)	<b>D100</b>	GND (FIXED)
<b>C101</b>	PEG_RX15+ (NA)	<b>D101</b>	PEG_TX15+ (NA)
<b>C102</b>	PEG_RX15- (NA)	<b>D102</b>	PEG_TX15- (NA)
<b>C103</b>	GND	<b>D103</b>	GND
<b>C104</b>	VCC_8.5V~ 20V	<b>D104</b>	VCC_8.5V~ 20V
<b>C105</b>	VCC_8.5V~ 20V	<b>D105</b>	VCC_8.5V~ 20V
<b>C106</b>	VCC_8.5V~ 20V	<b>D106</b>	VCC_8.5V~ 20V
<b>C107</b>	VCC_8.5V~ 20V	<b>D107</b>	VCC_8.5V~ 20V
<b>C108</b>	VCC_8.5V~ 20V	<b>D108</b>	VCC_8.5V~ 20V
<b>C109</b>	VCC_8.5V~ 20V	<b>D109</b>	VCC_8.5V~ 20V
<b>C110</b>	GND (FIXED)	<b>D110</b>	GND (FIXED)

## ► COM Express Connector Signal Description

AC97/HDA Signals Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGU968	Carrier Board	Description
AC/HAD_RST#	A30	O CMOS	3.3V Suspend/3.3V		Connect to CODEC pin 11 RESET#	Reset output to CODEC, active low.
AC/HDA_SYNC	A29	O CMOS	3.3V/3.3V		Connect to CODEC pin 10 SYNC	Sample-synchronization signal to the CODEC(s).
AC/HDA_BITCLK	A32	I/O CMOS	3.3V/3.3V		Connect to CODEC pin 6 BIT_CLK	Serial data clock generated by the external CODEC(s).
AC/HDA_SDOOUT	A33	O CMOS	3.3V/3.3V		Connect to CODEC pin 5 SDATA_OUT	Serial TDM data output to the CODEC.
AC/HDA_SDIN2	B28	I/O CMOS	3.3V Suspend/3.3V	HDA_SDIN2 NA	NC	
AC/HDA_SDIN1	B29	I/O CMOS	3.3V Suspend/3.3V		Connect 33 Ω in series to CODEC1 pin 8 SDATA_IN	Serial TDM data inputs from up to 3 CODECs.
AC/HDA_SDIN0	B30	I/O CMOS	3.3V Suspend/3.3V		Connect 33 Ω in series to CODEC0 pin 8 SDATA_IN	

Gigabit Ethernet Signals Descriptions																										
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGU968	Carrier Board	Description																				
GBE0_MDIO+	A13	I/O MDI	Less than 3.3V May be active in Suspend	i225 2.5GbE signal	Connect to Magnetics Module MDIO+/-	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes or in 2.5, 5.0 and 10 Gbps modes. Some pairs are unused in some modes, per the following:																				
GBE0_MDIO+	A10	I/O MDI	Less than 3.3V May be active in Suspend		Connect to Magnetics Module MDIO+/-																					
GBE0_MDIO-	A9	I/O MDI	Less than 3.3V May be active in Suspend			<table border="1"> <thead> <tr> <th></th> <th>1000BASE-T 2.5GBASE-T 5.0GBASE-T 10GBASE-T</th> <th>100BASE-TX</th> <th>10BASE-T</th> </tr> </thead> <tbody> <tr> <td>MDIO0+/-</td> <td>B1_DA+/-</td> <td>TX+/-</td> <td>TX+/-</td> </tr> <tr> <td>MDIO1+/-</td> <td>B1_DB+/-</td> <td>RX+/-</td> <td>RX+/-</td> </tr> <tr> <td>MDIO2+/-</td> <td>B1_DC+/-</td> <td></td> <td></td> </tr> <tr> <td>MDIO3+/-</td> <td>B1_DD+/-</td> <td></td> <td></td> </tr> </tbody> </table>		1000BASE-T 2.5GBASE-T 5.0GBASE-T 10GBASE-T	100BASE-TX	10BASE-T	MDIO0+/-	B1_DA+/-	TX+/-	TX+/-	MDIO1+/-	B1_DB+/-	RX+/-	RX+/-	MDIO2+/-	B1_DC+/-			MDIO3+/-	B1_DD+/-		
	1000BASE-T 2.5GBASE-T 5.0GBASE-T 10GBASE-T	100BASE-TX	10BASE-T																							
MDIO0+/-	B1_DA+/-	TX+/-	TX+/-																							
MDIO1+/-	B1_DB+/-	RX+/-	RX+/-																							
MDIO2+/-	B1_DC+/-																									
MDIO3+/-	B1_DD+/-																									
GBE0_MDIO2+	A7	I/O MDI	Less than 3.3V May be active in Suspend		Connect to Magnetics Module MDIO2+/-																					
GBE0_MDIO2-	A6	I/O MDI	Less than 3.3V May be active in Suspend																							
GBE0_MDIO3+	A3	I/O MDI	Less than 3.3V May be active in Suspend		Connect to Magnetics Module MDIO3+/-																					
GBE0_MDIO3-	A2	I/O MDI	Less than 3.3V May be active in Suspend																							
GBE0_ACT#	B2	OD CMOS	3.3V Suspend/3.3V		Connect to LED and recommend current limit resistor 150 Ω to 3.3VSB	Gigabit Ethernet Controller 0 activity indicator, active low.																				
GBE0_LINK#	A8	OD CMOS	3.3V Suspend/3.3V		NC	Gigabit Ethernet Controller 0 link indicator, active low.																				
GBE0_LINK_100#	A4	OD CMOS	3.3V Suspend/3.3V	LED for link speed with 1Gbps	Connect to LED and recommend current limit resistor 150Ω to 3.3VSB	Gigabit Ethernet Controller MID Speed Link indicator. Active low. If active, the link is established but at a speed lower than the maximum speed supported by the Ethernet controller. Note that based on capabilities of the Ethernet controller used this signal might not be active for all possible lower link speeds. This Module pin should be capable of sinking up to 20 mA at a Voh of 0.4 max. Was GBE0_LINK_MID# in COM Express Rev. 3.0.																				
GBE0_LINK_1000#	A5	OD CMOS	3.3V Suspend/3.3V	LED for link speed with 2.5Gbps	Connect to LED and recommend current limit resistor 150Ω to 3.3VSB	Gigabit Ethernet Controller MAX Speed Link Indicator. Active low. If active, the link is established at the maximum link speed supported by the controller. This Module pin should be capable of sinking up to 20 mA at a Voh of 0.4 max. Was GBE0_LINK_MAX# in COM Express Rev. 3.0.																				

SATA Signals Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGU968	Carrier Board	Description
SATA0_TX+	A16	O SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATA0 Conn TX pin	Serial ATA or SAS Channel 0 transmit differential pair.
SATA0_TX-	A17	O SATA	AC coupled on Module	AC Coupling capacitor		
SATA0_RX+	A19	I SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATA0 Conn RX pin	Serial ATA or SAS Channel 0 receive differential pair.
SATA0_RX-	A20	I SATA	AC coupled on Module	AC Coupling capacitor		
SATA1_TX+	B16	O SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATA1 Conn TX pin	Serial ATA or SAS Channel 1 transmit differential pair.
SATA1_TX-	B17	O SATA	AC coupled on Module	AC Coupling capacitor		
SATA1_RX+	B19	I SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATA1 Conn RX pin	Serial ATA or SAS Channel 1 receive differential pair.
SATA1_RX-	B20	I SATA	AC coupled on Module	AC Coupling capacitor		
SATA2_TX+	A22	O SATA	AC coupled on Module	NA	NA (No support)	NA (No support)
SATA2_TX-	A23	O SATA	AC coupled on Module	NA	NA (No support)	NA (No support)
SATA2_RX+	A25	I SATA	AC coupled on Module	NA	NA (No support)	NA (No support)
SATA2_RX-	A26	I SATA	AC coupled on Module	NA	NA (No support)	NA (No support)
SATA3_TX+	B22	O SATA	AC coupled on Module	NA	NA (No support)	NA (No support)
SATA3_TX-	B23	O SATA	AC coupled on Module	NA	NA (No support)	NA (No support)
SATA3_RX+	B25	I SATA	AC coupled on Module	NA	NA (No support)	NA (No support)
SATA3_RX-	B26	I SATA	AC coupled on Module	NA	NA (No support)	NA (No support)
ATA_ACT#	A28	I/O CMOS	3.3V / 3.3V	PU 47K to 3.3V	Connect to LED and <b>recommend</b> current limit resistor 220Ω to 3.3V	ATA (parallel and serial) or SAS activity indicator, active low.

PCI Express Lanes Signals Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGU968	Carrier Board	Description
PCIE_TX0+	A68	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express differential transmit pairs 0
PCIE_TX0-	A69	O PCIE	AC coupled on Module	AC Coupling capacitor		
PCIE_RX0+	B68	I PCIE	AC coupled off Module		<b>Device</b> - Connect AC Coupling cap 0.1uF <b>Slot</b> - Connect to PCIE Conn pin	PCI Express differential receive pairs 0
PCIE_RX0-	B69	I PCIE	AC coupled off Module			
PCIE_TX1+	A64	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express differential transmit pairs 1
PCIE_TX1-	A65	O PCIE	AC coupled on Module	AC Coupling capacitor		
PCIE_RX1+	B64	I PCIE	AC coupled off Module		<b>Device</b> - Connect AC Coupling cap 0.1uF <b>Slot</b> - Connect to PCIE Conn pin	PCI Express differential receive pairs 1
PCIE_RX1-	B65	I PCIE	AC coupled off Module			
PCIE_TX2+	A61	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express differential transmit pairs 2
PCIE_TX2-	A62	O PCIE	AC coupled on Module	AC Coupling capacitor		
PCIE_RX2+	B61	I PCIE	AC coupled off Module		<b>Device</b> - Connect AC Coupling cap 0.1uF <b>Slot</b> - Connect to PCIE Conn pin	PCI Express differential receive pairs 2
PCIE_RX2-	B62	I PCIE	AC coupled off Module			
PCIE_TX3+	A58	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express differential transmit pairs 3
PCIE_TX3-	A59	O PCIE	AC coupled on Module	AC Coupling capacitor		
PCIE_RX3+	B58	I PCIE	AC coupled off Module		<b>Device</b> - Connect AC Coupling cap 0.1uF (This Port is BOM Option with On board LAN) <b>Slot</b> - Connect to PCIE Conn pin	PCI Express differential receive pairs 3
PCIE_RX3-	B59	I PCIE	AC coupled off Module			
PCIE_TX4+	A55	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express differential transmit pairs 4
PCIE_TX4-	A56	O PCIE	AC coupled on Module	AC Coupling capacitor		

PCI Express Lanes Signals Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGU968	Carrier Board	Description
PCIE_RX4+	B55	I PCIE	AC coupled off Module	Optional	<b>Device</b> - Connect AC Coupling cap 0.1uF <b>Slot</b> - Connect to PCIE Conn pin	PCI Express differential receive pairs 4
PCIE_RX4-	B56			Optional		
PCIE_TX5+(Optional to LAN i225)	A52	O PCIE	AC coupled on Module	Optional	Connect to PCIE device or slot (This Port is BOM Option with On board LAN)	PCI Express differential transmit pairs 5 (This Port is BOM Option with i225)
PCIE_TX5-(Optional to LAN i225)	A53			Optional		
PCIE_RX5+(Optional to LAN i225)	B52	I PCIE	AC coupled off Module	Optional	<b>Device</b> - Connect AC Coupling cap 0.1uF (This Port is BOM Option with On board LAN) <b>Slot</b> - Connect to PCIE Conn pin	PCI Express differential receive pairs 5 (This Port is BOM Option with i225)
PCIE_RX5-(Optional to LAN i225)	B53			Optional		
PCIE_TX6+ (Optional to SATA port)	D19	O PCIE	AC coupled on Module	Optional	Optional to PCIE or SATA	PCI Express differential transmit pairs 6
PCIE_TX6- (Optional to SATA port)	D20			Optional		
PCIE_RX6+(Optional to SATA port)	C19	I PCIE	AC coupled off Module	Optional	Optional to PCIE or SATA	PCI Express differential receive pairs 6
PCIE_RX6-(Optional to SATA port)	C20			Optional		
PCIE_TX7+ (Optional to SATA port)	D22	O PCIE	AC coupled on Module	Optional	Optional to PCIE or SATA	PCI Express differential transmit pairs 7
PCIE_TX7- (Optional to SATA port)	D23			Optional		
PCIE_RX7+ (Optional to SATA port)	C22	I PCIE	AC coupled off Module	Optional	Optional to PCIE or SATA	PCI Express differential receive pairs 7
PCIE_RX7- (Optional to SATA port)	C23			Optional		
PCIE0_CK_REF+	A88	O PCIE	PCIE		Connect to PCIE device, <b>PCIE CLK Buffer</b> or slot	Reference clock output for all PCI Express and PCI Express Graphicslanes.
PCIE0_CK_REF-	A89					

PEG Signals Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGU968	Carrier Board	Description
PEG_TX0+ (Optional)	D52	O PCIE	AC coupled on Module	Optional	Optional to PCIE or NVMe SSD	Optional by module
PEG_TX0- (Optional)	D53			Optional		
PEG_RX0+ (Optional)	C52	I PCIE	AC coupled off Module		PCI Express Graphics receive differential pairs 0	PEG channel 0, Receive Input differential pair
PEG_RX0- (Optional)	C53					
PEG_TX1+ (Optional)	D55	O PCIE	AC coupled on Module	Optional	Optional to PCIE or NVMe SSD	Optional by module
PEG_TX1- (Optional)	D56			Optional		
PEG_RX1+ (Optional)	C55	I PCIE	AC coupled off Module		PCI Express Graphics receive differential pairs 1	PEG channel 1, Receive Input differential pair
PEG_RX1- (Optional)	C56					
PEG_TX2+ (Optional)	D58	O PCIE	AC coupled on Module	Optional	Optional to PCIE or NVMe SSD	Optional by module
PEG_TX2- (Optional)	D59			Optional		
PEG_RX2+ (Optional)	C58	I PCIE	AC coupled off Module		PCI Express Graphics receive differential pairs 2	PEG channel 2, Receive Input differential pair
PEG_RX2- (Optional)	C59					
PEG_TX3+ (Optional)	D61	O PCIE	AC coupled on Module	Optional	Optional to PCIE or NVMe SSD	Optional by module
PEG_TX3- (Optional)	D62			Optional		
PEG_RX3+ (Optional)	C61	I PCIE	AC coupled off Module		PCI Express Graphics receive differential pairs 3	PEG channel 3, Receive Input differential pair
PEG_RX3- (Optional)	C62					
PEG_TX4+	D65	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 4
PEG_TX4-	D66			NA		
PEG_RX4+	C65	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 4
PEG_RX4-	C66			NA		
PEG_TX5+	D68	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 5
PEG_TX5-	D69			NA		
PEG_RX5+	C68	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 5
PEG_RX5-	C69			NA		
PEG_TX6+	D71	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 6
PEG_TX6-	D72			NA		
PEG_RX6+	C71	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 6
PEG_RX6-	C72			NA		
PEG_TX7+	D74	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 7
PEG_TX7-	D75			NA		
PEG_RX7+	C74	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 7
PEG_RX7-	C75			NA		
PEG_TX8+	D78	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 8
PEG_TX8-	D79			NA		
PEG_RX8+	C78	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 8
PEG_RX8-	C79			NA		
PEG_TX9+	D81	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 9
PEG_TX9-	D82			NA		
PEG_RX9+	C81	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 9
PEG_RX9-	C82			NA		
PEG_TX10+	D85	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 10
PEG_TX10-	D86			NA		
PEG_RX10+	C85	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 10
PEG_RX10-	C86			NA		
PEG_TX11+	D88	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 11
PEG_TX11-	D89			NA		
PEG_RX11+	C88	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 11
PEG_RX11-	C89			NA		
PEG_TX12+	D91	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 12
PEG_TX12-	D92			NA		
PEG_RX12+	C91	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 12
PEG_RX12-	C92			NA		

PEG Signals Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGU968	Carrier Board	Description
PEG_TX13+	D94			NA		
PEG_TX13-	D95	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 13
PEG_RX13+	C94			NA		
PEG_RX13-	C95	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 13
PEG_TX14+	D98			NA		
PEG_TX14-	D99	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 14
PEG_RX14+	C98			NA		
PEG_RX14-	C99	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 14
PEG_TX15+	D101			NA		
PEG_TX15-	D102	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 15
PEG_RX15+	C101			NA		
PEG_RX15-	C102	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 15
PEG_LANE_RV#	D54	I CMOS	3.3V / 3.3V	PU 10K to 3.3V		PCI Express Graphics lane reversal input strap. Pull low on the Carrierboard to reverse lane order.

DDI Signals Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGU968	Carrier Board	Description
DDI1_PAIR0+/SDVO1_RED+	D26				Connect AC Coupling Capacitors 0.1uF to Device	
DDI1_PAIR0-/SDVO1_RED-	D27	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 1 Pair 0 differential pairs/Serial Digital Video B red output differential pair
DDI1_PAIR1+/SDVO1_GRN+	D29				Connect AC Coupling Capacitors 0.1uF to Device	
DDI1_PAIR1-/SDVO1_GRN-	D30	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 1 Pair 1 differential pairs/Serial Digital Video B green output differential pair
DDI1_PAIR2+/SDVO1_BLU+	D32				Connect AC Coupling Capacitors 0.1uF to Device	
DDI1_PAIR2-/SDVO1_BLU-	D33	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 1 Pair 2 differential pairs/Serial Digital Video B blue output differential pair
DDI1_PAIR3+/SDVO1_CK+	D36				Connect AC Coupling Capacitors 0.1uF to Device	
DDI1_PAIR3-/SDVO1_CK-	D37	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 1 Pair 3 differential pairs/Serial Digital Video B clock output differential pair.
DDI1_PAIR4+/SDVO1_INT+	C25				NA (No support)	NA (No support)
DDI1_PAIR4-/SDVO1_INT-	C26	I PCIE	AC coupled off Module		NA (No support)	NA (No support)
DDI1_PAIR5+/SDVO1_TVCLKIN+	C29				NA (No support)	NA (No support)
DDI1_PAIR5-/SDVO1_TVCLKIN-	C30	I PCIE	AC coupled off Module		NA (No support)	NA (No support)
DDI1_PAIR6+/SDVO1_FLDSTALL+	C15				NA (No support)	NA (No support)
DDI1_PAIR6-/SDVO1_FLDSTALL-	C16	I PCIE	AC coupled off Module		NA (No support)	NA (No support)
DDI1_CTRLCLK_AUX+/SDVO1_CTRLCLK	D15	I/O PCIE	AC coupled on Module	PD 100K to GND <b>(S/W IC between Rpu/PCH)</b>	Connect to DP AUX+	DP AUX+ function if DDI1_DDC_AUX_SEL is no connect
		I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V, PD 100K to GND <b>(S/W IC between Rpu/Rpd resistor)</b>	Connect to HDMI/DVI I2C CTRLCLK	HDMI/DVI I2C CTRLCLK if DDI1_DDC_AUX_SEL is pulled high
DDI1_CTRLCLK_AUX-/SDVO1_CTRLDATA	D16	I/O PCIE	AC coupled on Module	PU 100K to 3.3V <b>(S/W IC between Rpu/PCH)</b>	Connect to DP AUX-	DP AUX- function if DDI1_DDC_AUX_SEL is no connect
		I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V/PU 100K to 3.3V <b>(S/W IC between 2.2K/100K resistor)</b>	Connect to HDMI/DVI I2C CTRLDATA	HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high
DDI1_HPD	C24	I CMOS	3.3V / 3.3V		PD 1M and Connect to device Hot Plug Detect	DDI Hot-Plug Detect
DDI1_DDC_AUX_SEL	D34	I CMOS	3.3V / 3.3V	PD 1M to GND	PU 100K to 3.3V for DDC(HDMI/DVI)	Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRLDATA_AUX-. DDI1[n]_DDC_AUX_SEL shall be pulled to 3.3V on the Carrier with a 100K Ohm resistor to configure the DDI1[n]_AUX pair as the DDC channel. Carrier DDI1[n]_DDC_AUX_SEL should be connected to pin 13 of the DisplayPort
DDI2_PAIR0+	D39				Connect AC Coupling Capacitors 0.1uF to Device	
DDI2_PAIR0-	D40	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 2 Pair 0 differential pairs/Serial Digital Video B red output differential pair
DDI2_PAIR1+	D42				Connect AC Coupling Capacitors 0.1uF to Device	
DDI2_PAIR1-	D43	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 2 Pair 1 differential pairs/Serial Digital Video B green output differential pair
DDI2_PAIR2+	D46				Connect AC Coupling Capacitors 0.1uF to Device	
DDI2_PAIR2-	D47	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 2 Pair 2 differential pairs/Serial Digital Video B blue output differential pair
DDI2_PAIR3+	D49				Connect AC Coupling Capacitors 0.1uF to Device	
DDI2_PAIR3-	D50	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 2 Pair 3 differential pairs/Serial Digital Video B clock output differential pair

DDI Signals Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	TGU968	Carrier Board	Description
DDI2_CTRLCLK_AUX+	C32	I/O PCIE	AC coupled on Module	PD 100K to GND (S/W IC between Rpu/PCH)	Connect to DP AUX+	DP AUX+ function if DDI2_DDC_AUX_SEL is no connect
		I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V, PD 100K to GND (S/W IC between Rpu/Rpd resistor)	Connect to HDMI/DVI I2C CTRLCLK	HDMI/DVI I2C CTRLCLK if DDI2_DDC_AUX_SEL is pulled high
DDI2_CTRLDATA_AUX-	C33	I/O PCIE	AC coupled on Module	PU 100K to 3.3V (S/W IC between Rpu/PCH)	Connect to DP AUX-	DP AUX- function if DDI2_DDC_AUX_SEL is no connect
		I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V/PU 100K to 3.3V (S/W IC between 2.2K/100K resistor)	Connect to HDMI/DVI I2C CTRLDATA	HDMI/DVI I2C CTRLDATA if DDI2_DDC_AUX_SEL is pulled high
DDI2_HPD	D44	I CMOS	3.3V / 3.3V		PD 1M and Connect to device Hot Plug Detect	DDI Hot-Plug Detect
DDI2_DDC_AUX_SEL	C34	I CMOS	3.3V / 3.3V	PD 1M to GND	PU 100K to 3.3V for DDC(HDMI/DVI)	Selects the function of DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_AUX-. DDI[n]_DDC_AUX_SEL shall be pulled to 3.3V on the Carrier with a 100K Ohm resistor to configure the DDI[n]_AUX pair as the DDC channel. Carrier DDI[n]_DDC_AUX_SEL should be connected to pin 13 of the DisplayPort
DDI3_PAIR0+	C39	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 3 Pair 0 differential pairs/Serial Digital Video B red output differential pair
DDI3_PAIR0-	C40				Connect AC Coupling Capacitors 0.1uF to Device	
DDI3_PAIR1+	C42	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 3 Pair 1 differential pairs/Serial Digital Video B green output differential pair
DDI3_PAIR1-	C43				Connect AC Coupling Capacitors 0.1uF to Device	
DDI3_PAIR2+	C46	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 3 Pair 2 differential pairs/Serial Digital Video B blue output differential pair
DDI3_PAIR2-	C47				Connect AC Coupling Capacitors 0.1uF to Device	
DDI3_PAIR3+	C49	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 3 Pair 3 differential pairs/Serial Digital Video B clock output differential pair
DDI3_PAIR3-	C50				Connect AC Coupling Capacitors 0.1uF to Device	
DDI3_CTRLCLK_AUX+	C36	I/O PCIE	AC coupled on Module	PD 100K to GND (S/W IC between Rpu/PCH)	Connect to DP AUX+	DP AUX+ function if DDI3_DDC_AUX_SEL is no connect
		I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V, PD 100K to GND (S/W IC between Rpu/Rpd resistor)	Connect to HDMI/DVI I2C CTRLCLK	HDMI/DVI I2C CTRLCLK if DDI3_DDC_AUX_SEL is pulled high
DDI3_CTRLDATA_AUX-	C37	I/O PCIE	AC coupled on Module	PU 100K to 3.3V (S/W IC between Rpu/PCH)	Connect to DP AUX-	DP AUX- function if DDI3_DDC_AUX_SEL is no connect
		I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V/PU 100K to 3.3V (S/W IC between 2.2K/100K resistor)	Connect to HDMI/DVI I2C CTRLDATA	HDMI/DVI I2C CTRLDATA if DDI3_DDC_AUX_SEL is pulled high
DDI3_HPD	C44	I CMOS	3.3V / 3.3V		PD 1M and Connect to device Hot Plug Detect	DDI Hot-Plug Detect
DDI3_DDC_AUX_SEL	C38	I CMOS	3.3V / 3.3V	PD 1M to GND	PU 100K to 3.3V for DDC(HDMI/DVI)	Selects the function of DDI3_CTRLCLK_AUX+ and DDI3_CTRLDATA_AUX-. DDI[n]_DDC_AUX_SEL shall be pulled to 3.3V on the Carrier with a 100K Ohm resistor to configure the DDI[n]_AUX pair as the DDC channel. Carrier DDI[n]_DDC_AUX_SEL should be connected to pin 13 of the DisplayPort

USB Signals Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	TGU968	Carrier Board	Description
USB0+	A46	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 0
USB0-	A45					
USB1+	B46	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 1
USB1-	B45					
USB2+	A43	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 2
USB2-	A42					
USB3+	B43	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 3
USB3-	B42					
USB4+	A40	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 4
USB4-	A39					
USB5+	B40	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 5
USB5-	B39					
USB6+	A37	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 6
USB6-	A36					
USB7+	B37	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 7, USB7 may be configured as a USB client or as a host, or both, at the Module designer's discretion.(CR901-B default set as a host)
USB7-	B36					

USB Signals Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGU968	Carrier Board	Description
USB_0_1_OC#	B44	I CMOS	3.3V Suspend/3.3V	PU 10k to 3.3VSB	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 0 and 1. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_2_3_OC#	A44	I CMOS	3.3V Suspend/3.3V	PU 10k to 3.3VSB	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 2 and 3. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_4_5_OC#	B38	I CMOS	3.3V Suspend/3.3V	PU 10k to 3.3VSB	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 4 and 5. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_6_7_OC#	A38	I CMOS	3.3V Suspend/3.3V	PU 10k to 3.3VSB	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 6 and 7. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_SSTX0+	D4					
USB_SSTX0-	D3	O PCIE	AC coupled on Module		Connect 90Ω@100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSRX0+	C4					
USB_SSRX0-	C3	I PCIE	AC coupled off Module		Connect 90Ω@100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSTX1+	D7					
USB_SSTX1-	D6	O PCIE	AC coupled on Module		Connect 90Ω@100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSRX1+	C7					
USB_SSRX1-	C6	I PCIE	AC coupled off Module		Connect 90Ω@100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSTX2+	D10					
USB_SSTX2-	D9	O PCIE	AC coupled on Module		Connect 90Ω@100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSRX2+	C10					
USB_SSRX2-	C9	I PCIE	AC coupled off Module		Connect 90Ω@100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSTX3+	D13					
USB_SSTX3-	D12	O PCIE	AC coupled on Module		Connect 90Ω@100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSRX3+	C13					
USB_SSRX3-	C12	I PCIE	AC coupled off Module		Connect 90Ω@100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional receive signal differential pairs for the SuperSpeed USB data path.

LVDS Signals Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGU968	Carrier Board	Description
LVDS_A0+	A71				Connect to LVDS connector	
LVDS_A0-	A72	O LVDS	LVDS			
LVDS_A1+	A73				Connect to LVDS connector	
LVDS_A1-	A74	O LVDS	LVDS			
LVDS_A2+	A75				Connect to LVDS connector	
LVDS_A2-	A76	O LVDS	LVDS			
LVDS_A3+	A78				Connect to LVDS connector	
LVDS_A3-	A79	O LVDS	LVDS			
LVDS_A_CK+	A81				Connect to LVDS connector	
LVDS_A_CK-	A82	O LVDS	LVDS			LVDS Channel A differential clock
LVDS_B0+	B71				Connect to LVDS connector	
LVDS_B0-	B72	O LVDS	LVDS			
LVDS_B1+	B73				Connect to LVDS connector	
LVDS_B1-	B74	O LVDS	LVDS			
LVDS_B2+	B75				Connect to LVDS connector	
LVDS_B2-	B76	O LVDS	LVDS			
LVDS_B3+	B77				Connect to LVDS connector	
LVDS_B3-	B78	O LVDS	LVDS			
LVDS_B_CK+	B81				Connect to LVDS connector	
LVDS_B_CK-	B82	O LVDS	LVDS			LVDS Channel B differential clock
LVDS_VDD_EN	A77	O CMOS	3.3V / 3.3V		Connect to enable control of LVDS panel power circuit	LVDS panel power enable
LVDS_BKLT_EN	B79	O CMOS	3.3V / 3.3V		Connect to enable control of LVDS panel backlight power circuit.	LVDS panel backlight enable
LVDS_BKLT_CTRL	B83	O CMOS	3.3V / 3.3V		Connect to brightness control of LVDS panel backlight power circuit.	LVDS panel backlight brightness control
LVDS_I2C_CLK	A83	I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V	Connect to DDC clock of LVDS panel	I2C clock output for LVDS display use
LVDS_I2C_DAT	A84	I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V	Connect to DDC data of LVDS panel	I2C data line for LVDS display use

eDP Signals Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGU968	Carrier Board	Description
eDP_TX2+	A71					eDP differential pairs
eDP_TX2-	A72	O LV_DIFF	AC coupled off module		Connect to eDP connector	
eDP_TX1+	A73					
eDP_TX1-	A74	O LV_DIFF	AC coupled off module		Connect to eDP connector	
eDP_TX0+	A75					
eDP_TX0-	A76	O LV_DIFF	AC coupled off module		Connect to eDP connector	
eDP_TX3+	A81					eDP power enable
eDP_TX3-	A82	O LV_DIFF	AC coupled off module		Connect to eDP connector	
eDP_VDD_EN	A77	O CMOS	3.3V / 3.3V		Connect to enable eDP power.	eDP backlight enable
eDP_BKLT_EN	B79	I/O LV_DIFF	AC couple off module		Connect to enable control of eDP backlight power circuit.	eDP backlight enable
eDP_BKLT_CTRL	B83	O CMOS	3.3V / 3.3V		Connect to brightness control of eDP panel backlight power circuit.	eDP backlight brightness control
eDP_AUX+	A83	I/O LV_DIFF			eDP AUX+	I2C clock output for LVDS display use
eDP_AUX-	A84	I/O LV_DIFF	AC couple off module		eDP AUX-	I2C data line for LVDS display use
eDP_HPD	A87	I CMOS	3.3V / 3.3V		eDP connector hot plug detection	Detection of Hot Plug/ Unplug and notification of the link layer

LPC & eSPI Signals Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGU968	Carrier Board	Description
LPC_AD0	B4			LPC_ADC0 /eSPI to LPC bridge	Connect to LPC device	LPC & eSPI multi-function pin with bridge
LPC_AD1	B5			LPC_ADC1 /eSPI to LPC bridge		
LPC_AD2	B6	I/O CMOS	3.3V / 3.3V	LPC_ADC2 /eSPI to LPC bridge		
LPC_AD3	B7			LPC_ADC3 /eSPI to LPC bridge		
LPC_FRAME#	B3	O CMOS	3.3V / 3.3V	LPC_ADC0 /eSPI_CS0#		
LPC_DRQ0#	B8			LPC_ADC0 /eSPI_ALERT0#		
LPC_DRQ1#	B9	I CMOS	3.3V / 3.3V	LPC_ADC0 /eSPI_ALERT1#	LPC frame indicates the start of an LPC cycle	NA (No support)
LPC_SERIRQ	A50	I/O CMOS	3.3V / 3.3V	LPC_SERIRQ /eSPI_CS1#		LPC serial interrupt
LPC_CLK	B10	O CMOS	3.3V / 3.3V	LPC_CLK/eSPI_CK		LPC clock output - 33MHz nominal

SPI Signals Descriptions																																														
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGU968	Carrier Board	Description																																								
SPI_CS#	B97	O CMOS	3.3V Suspend/3.3V		<b>Connect a series resistor 33Ω to Carrier Board SPI Device CS# pin</b>	Chip select for Carrier Board SPI - may be sourced from chipset SPI0 or SPI1																																								
SPI_MISO	A92	I CMOS	3.3V Suspend/3.3V		<b>Connect a series resistor 33Ω to Carrier Board SPI Device S0 pin</b>	Data in to Module from Carrier SPI																																								
SPI_MOSI	A95	O CMOS	3.3V Suspend/3.3V		<b>Connect a series resistor 33Ω to Carrier Board SPI Device S1 pin</b>	Data out from Module to Carrier SPI																																								
SPI_CLK	A94	O CMOS	3.3V Suspend/3.3V		<b>Connect a series resistor 33Ω to Carrier Board SPI Device SCK pin</b>	Clock from Module to Carrier SPI																																								
SPI_POWER	A91	O	3.3V Suspend/3.3V			Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier																																								
BIOS_DIS0#	A34					Selection straps to determine the BIOS boot device. The Carrier should only float these or pull them low, please refer to COM Express Module Base Specification Revision 2.1 for strapping options of BIOS disable signals.																																								
BIOS_DIS1#	B88	I CMOS	NA			<table border="1"> <thead> <tr> <th>BIOS DIS#</th> <th>BIOS DIS0#</th> <th>Chipset SPI CS1# Destination</th> <th>Chipset SPI CS0# Destination</th> <th>Carrier SPI_CS#</th> <th>SPI Descriptor</th> <th>Bios Entry</th> <th>RefLine</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>Module</td> <td>Module</td> <td>High</td> <td>Module</td> <td>SPI0/SPI1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>Module</td> <td>Module</td> <td>High</td> <td>Module</td> <td>Carrier FWH</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>Module</td> <td>Carrier</td> <td>SPI0</td> <td>Carrier</td> <td>SPI0/SPI1</td> <td>2</td> </tr> <tr> <td>0</td> <td>0</td> <td>Carrier (Default)</td> <td>Module (Default)</td> <td>SPI1 (Default)</td> <td>Module (Default)</td> <td>SPI0/SPI1 (Default)</td> <td>3</td> </tr> </tbody> </table>	BIOS DIS#	BIOS DIS0#	Chipset SPI CS1# Destination	Chipset SPI CS0# Destination	Carrier SPI_CS#	SPI Descriptor	Bios Entry	RefLine	1	1	Module	Module	High	Module	SPI0/SPI1	0	1	0	Module	Module	High	Module	Carrier FWH	1	0	1	Module	Carrier	SPI0	Carrier	SPI0/SPI1	2	0	0	Carrier (Default)	Module (Default)	SPI1 (Default)	Module (Default)	SPI0/SPI1 (Default)	3
BIOS DIS#	BIOS DIS0#	Chipset SPI CS1# Destination	Chipset SPI CS0# Destination	Carrier SPI_CS#	SPI Descriptor	Bios Entry	RefLine																																							
1	1	Module	Module	High	Module	SPI0/SPI1	0																																							
1	0	Module	Module	High	Module	Carrier FWH	1																																							
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0	0	Carrier (Default)	Module (Default)	SPI1 (Default)	Module (Default)	SPI0/SPI1 (Default)	3																																							

VGA Signals Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	TGU968	Carrier Board	Description
VGA_RED	B89	O Analog	Analog	PD 150 to GND	PD 150R,connect to VGA connector with EMI filter & ESD protect component.	Red for monitor. Analog output
VGA_GRN	B91	O Analog	Analog	PD 150 to GND	PD 150R,connect to VGA connector with EMI filter & ESD protect component.	Green for monitor. Analog output
VGA_BLU	B92	O Analog	Analog	PD 150 to GND	PD 150R,connect to VGA connector with EMI filter & ESD protect component.	Blue for monitor. Analog output
VGA_HSYNC	B93	O CMOS	3.3V / 3.3V		Connect to VGA connector with a3.3V Buffer IC to isolate PCH & Display Device	Horizontal sync output to VGA monitor
VGA_VSYNC	B94	O CMOS	3.3V / 3.3V		Connect to VGA connector with a 3.3V Buffer IC to isolate PCH & Display Device	Vertical sync output to VGA monitor
VGA_12C_CK	B95	I/O OD CMOS	3.3V / 3.3V	PD 2.2K to 3.3V	Connect to VGA connector with a 3.3V to 5V Level shift circuit.	DDC clock line (I2C port dedicated to identify VGA monitor capabilities)
VGA_12C_DAT	B96	I/O OD CMOS	3.3V / 3.3V	PD 2.2K to 3.3V	Connect to VGA connector with a 3.3V to 5V Level shift circuit.	DDC data line.

Serial Interface Signals Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	TGU968	Carrier Board	Description
SER0_TX	A98	O CMOS	5V / 12V		PD 4.7K to GND	General purpose serial port 0 transmitter <b>(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)</b>
SER0_RX	A99	I CMOS	5V / 12V		PU 47K to 3.3V	General purpose serial port 0 receiver <b>(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)</b>
SER1_TX	A101	O CMOS	5V / 12V		PD 4.7K to GND	General purpose serial port 1 transmitter <b>(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)</b>
SER1_RX	A102	I CMOS	5V / 12V		PU 47K to 3.3V	General purpose serial port 1 receiver <b>(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)</b>

Power and System Management Signals Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	TGU968	Carrier Board	Description
PWRBTN#	B12	I CMOS	3.3V Suspend/3.3V	PU 10K to 3V3_DU_EC	PU 4.7K to 3V3_SB	A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off and other suspend states, as well as powering the system down.
SYS_RESET#	B49	I CMOS	3.3V Suspend/3.3V	PU 10K to 3V3_DU	NC PU 4.7K to 3V3_SB	Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a powercycle may be used.
CB_RESET#	B50	O CMOS	3.3V Suspend/3.3V	PD 100K to GND		Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software.
PWR_OK	B24	I CMOS	3.3V / 3.3V	PU 10K to 5V and PD 20K		Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGAs or other configurable devices time to be programmed.
SUS_STAT#	B18	O CMOS	3.3V Suspend/3.3V			Indicates imminent suspend operation; used to notify LPC devices.
SUS_S3#	A15	O CMOS	3.3V Suspend/3.3V	PD 10K to GND		Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board may be used to enable the non-standby power on a typical ATX supply.
SUS_S4#	A18	O CMOS	3.3V Suspend/3.3V	PD 10K to GND		Indicates system is in Suspend to Disk state. Active low output.
SUS_S5#	A24	O CMOS	3.3V Suspend/3.3V	PD 10K to GND		Indicates system is in Soft Off state.
WAKE0#	B66	I CMOS	3.3V Suspend/3.3V	PU 1K to 3V3_DU		PCI Express wake up signal.
WAKE1#	B67	I CMOS	3.3V Suspend/3.3V	PU 10K to 3V3_DU		General purpose wake up signal. May be used to implement wake-upon PS2 keyboard or mouse activity.
BATLOW#	A27	I CMOS	3.3V Suspend/ 3.3V	PU 10K to 3V3_DU		Indicates that external battery is low. This port provides a battery-low signal to the Module for orderlytransitioning to power saving or power cut-off ACPI modes.
LID#	A103	I OD CMOS	3.3V Suspend/12V	PU 47K to 3V3_DU_EC		LID switch. Low active signal used by the ACPI operating system for a LID switch. <b>(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)</b>
SLEEP#	B103	I OD CMOS	3.3V Suspend/12V	PU 10K to 3V3_DU_EC		Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again. <b>(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)</b>
THRM#	B35	I CMOS	3.3V / 3.3V	PU 10K to 3V3		Input from off-Module temp sensor indicating an over-temp situation.
THRMTRIP#	A35	O CMOS	3.3V / 3.3V	PU 10K to 3.3V		Active low output indicating that the CPU has entered thermal shutdown.
SMB_CK	B13	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3V3_DU_EC		System Management Bus bidirectional clock line.
SYS_RESET#	B49	I CMOS	3.3V Suspend/3.3V	PU 10K to 3V3_DU	NC PU 4.7K to 3V3_SB	Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power.
SMB_DAT	B14	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3V3_DU_EC		System Management Bus bidirectional data line.
SMB_ALERT#	B15	I CMOS	3.3V Suspend/3.3V	PU 2.2K to 3V3_DU_EC		System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.

GPIO Signals Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	TGU968	Carrier Board	Description
GPO0	A93	O CMOS	3.3V / 3.3V			General purpose output pins. <b>Upon a hardware reset, these outputs should be low.</b>
GPO1	B54					
GPO2	B57					
GPO3	B63					
GPI0	A54	I CMOS	3.3V / 3.3V	PU 10K to 3.3V		General purpose input pins. <b>Pulled high internally on the Module.</b>
GPI1	A63					
GPI2	A67					
GPI3	A85					

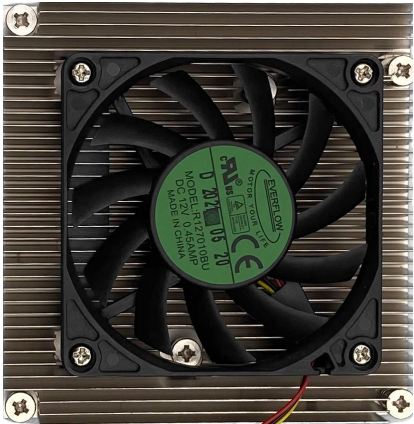
Power and GND Signal Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	TGU968	Carrier Board	Description
VCC_12V	A104~A109 B104~B109 C104~C109 D104~D109	Power				Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.
VCC_5V_SBY	B84~B87	Power				Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.
VCC_RTC	A47	Power				Real-time clock circuit-power input. Nominally +3.0V.
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1, B11, B21, B31, B41, B51, B60, B70, B80, B90, B100, B110, C1, C2, C5, C8, C11, C14, C21, C31, C41, C51, C60, C70, C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D31, D41, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Power				Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to CarrierBoard GND plane.

Miscellaneous Signal Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	TGU968	Carrier Board	Description
I2C_CLK	B33	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3.3VSB		General purpose I2C port clock output
I2C_DAT	B34	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3.3VSB		General purpose I2C port data I/O line
SPKR	B32	O CMOS	3.3V / 3.3V			Output for audio enunciator - the "speaker" in PC-AT systems. This port provides the PC beep signal and is mostly intended for debugging purposes.
WDT	B27	O CMOS	3.3V / 3.3V			Output indicating that a watchdog time-out event has occurred.
FAN_PWNOUT	B101	O OD CMOS	3.3V / 3.3V			Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM. <b>(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)</b>
FAN_TACHIN	B102	I OD CMOS	3.3V / 3.3V			Fan tachometer input for a fan with a two pulse output. <b>(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)</b>
TPM_PP	A96	I CMOS	3.3V / 3.3V	Default NA, PD 4.7K when stuff TPM chip		Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.

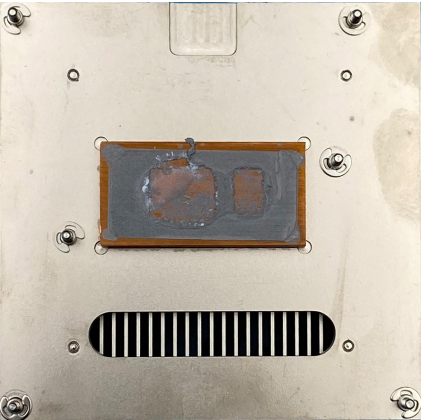
► Cooling Option

Heat Sink

The COM Express connector is used to interface the TGU968 COM Express board to a carrier board. Connect the COM Express connector (located on the solder side of the board) to the COM Express connector on the carrier board.



Top View of the Heat Sink

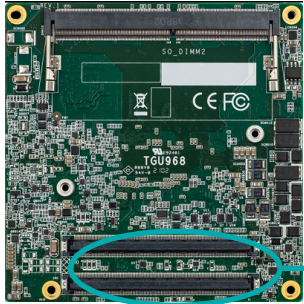


Bottom View of the Heat Sink

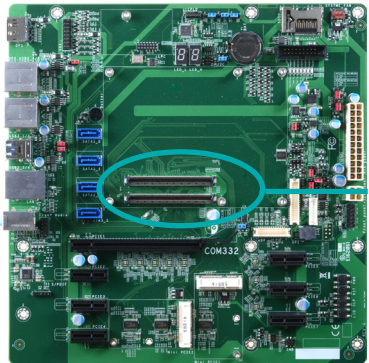
**Important:** Remove the plastic covering from the thermal pads prior to mounting the heat sink onto board.



**Important:** The carrier board (COM332-B) used in this section is for reference purpose only and may not resemble your carrier board. These illustrations are mainly to guide you on how to install TGU968 onto the carrier board of your choice. .

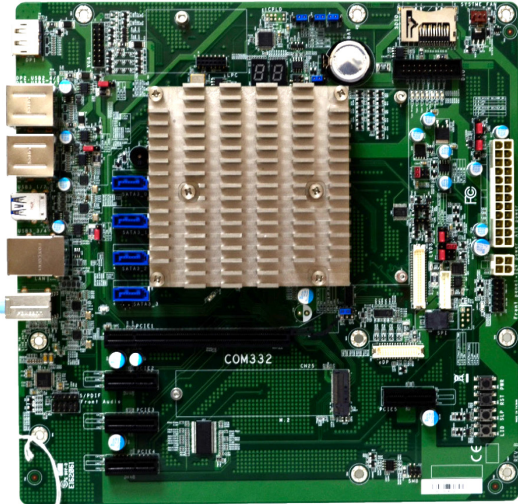


COM Express connector on TGU968



COM Express connector on the carrier board

- 2. Align the mounting holes of the heatsink with the mounting holes of the module. Use the provided mounting screws to install the heat sink onto the module.



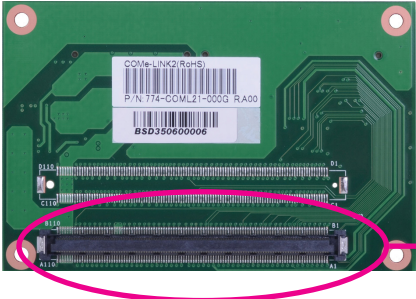
► Installing the COM Express Debug Card

**Note:**  
The system board used in the following illustrations may not resemble the actual board. These illustrations are for reference only.

- 1. COMe-LINK2 is the COM Express debug platform installed into COM Express Mini modules for the application of debugging and displaying signals and codes.



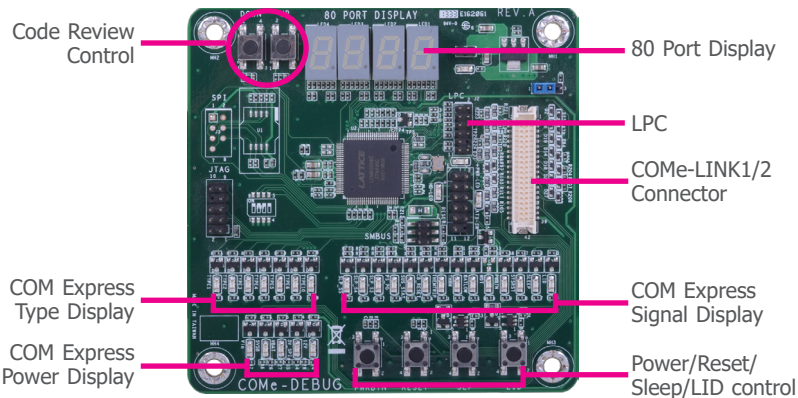
COM Express Connector



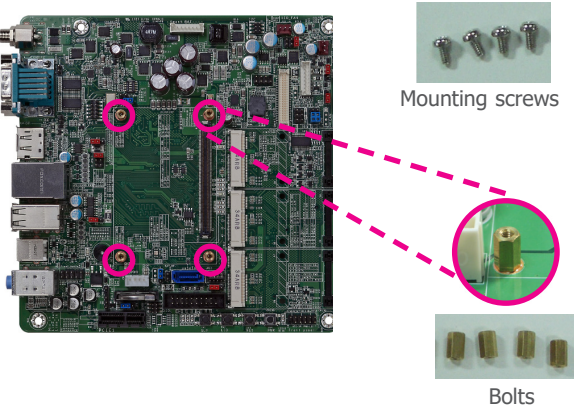
COM Express Connector

2. Connect the COMe-DEBUG card to COMe-LINK2 via a cable.

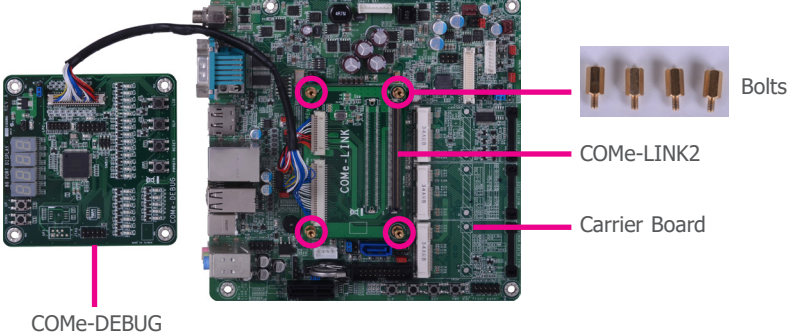
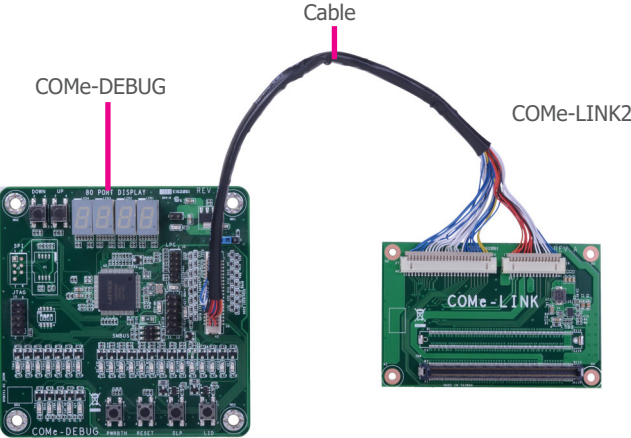
COMe-DEBUG



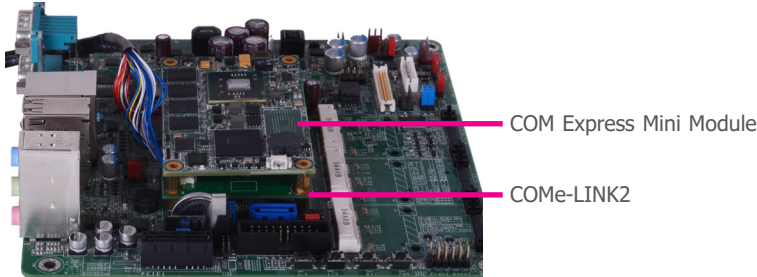
3. Fasten bolts with mounting screws through mounting holes to be fixed in place.



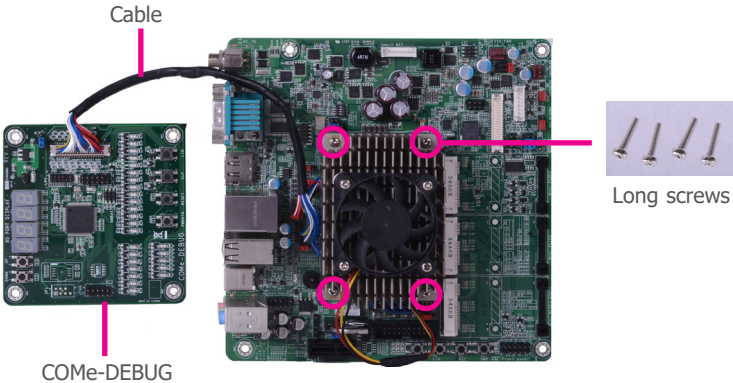
4. Use the provided bolts to fix the COMe-LINK2 debug card onto the carrier board.



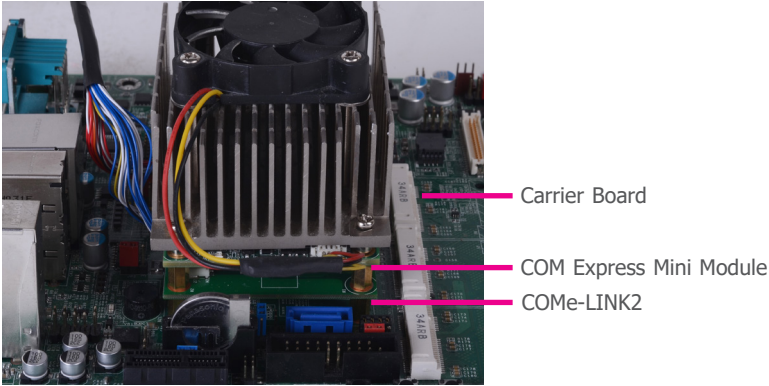
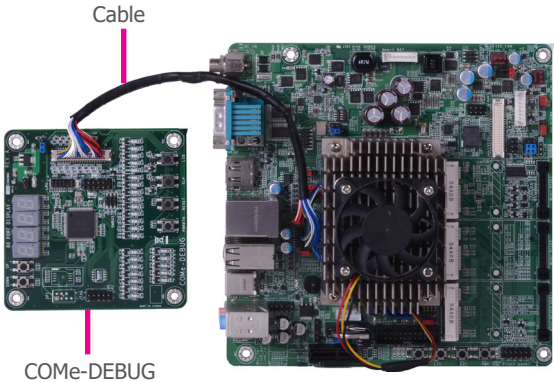
5. Grasp the COM Express Mini module by its edges to press it down on the top of the COMe-LINK2 debug card.



7. Use the long mounting screws to secure the heat sink on the top of the COM Express Mini module and the COMe-LINK2 debug card and connect the cooling fan's cable to the fan connector on the COM Express Mini module. The photo below shows the locations of long mounting screws.



6. Then, grasp the heat sink by its edges and position it down firmly on the top of the COM Express Mini module.



**Side View of the Module, Debug Card and Carrier Board**

## Chapter 4 - BIOS Settings

### ► Overview

The BIOS is a program that takes care of the basic level of communication between the CPU and peripherals. It contains codes for various advanced features found in this system board. The BIOS allows you to configure the system and save the configuration in a battery-backed CMOS so that the data retains even when the power is off. In general, the information stored in the CMOS RAM of the EEPROM will stay unchanged unless a configuration change has been made such as a hard drive replaced or a device added. It is possible that the CMOS battery will fail causing CMOS data loss. If this happens, you need to install a new CMOS battery and reconfigure the BIOS settings.



**Note:**

The BIOS is constantly updated to improve the performance of the system board; therefore the BIOS screens in this chapter may not appear the same as the actual one. These screens are for reference purpose only.

#### Default Configuration

Most of the configuration settings are either predefined according to the Load Optimal Defaults settings which are stored in the BIOS or are automatically detected and configured without requiring any actions. There are a few settings that you may need to change depending on your system configuration.

#### Entering the BIOS Setup Utility

The BIOS Setup Utility can only be operated from the keyboard and all commands are keyboard commands. The commands are available at the right side of each setup screen. The BIOS Setup Utility does not require an operating system to run. After you power up the system, the BIOS message appears on the screen and the memory count begins. After the memory test, the message "Press DEL to run setup" will appear on the screen. If the message disappears before you respond, restart the system or press the "Reset" button. You may also restart the system by pressing the <Ctrl> <Alt> and <Del> keys simultaneously.

### Legends

Keys	Function
Right / Left arrow	Move the highlight left or right to select a menu
Up / Down arrow	Move the highlight up or down between submenus or fields
<Enter>	Enter the highlighted submenu
+ (plus key)/F6	Scroll forward through the values or options of the highlighted field
- (minus key)/F5	Scroll backward through the values or options of the highlighted field
<F1>	Display general help
<F2>	Display previous values
<F7>	Popup Boot Device List
<F9>	Optimized defaults
<F10>	Save and Exit
<Esc>	Return to previous menu

#### Scroll Bar

When a scroll bar appears to the right of the setup screen, it indicates that there are more available fields not shown on the screen. Use the up and down arrow keys to scroll through all the available fields.

#### Submenu

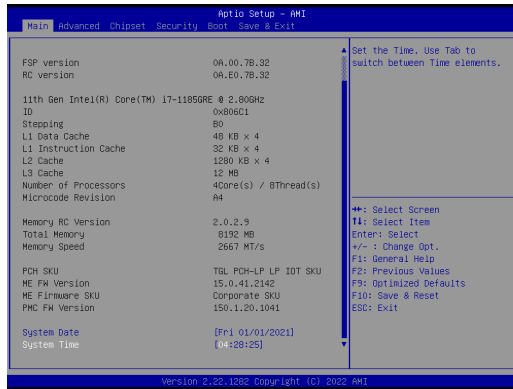
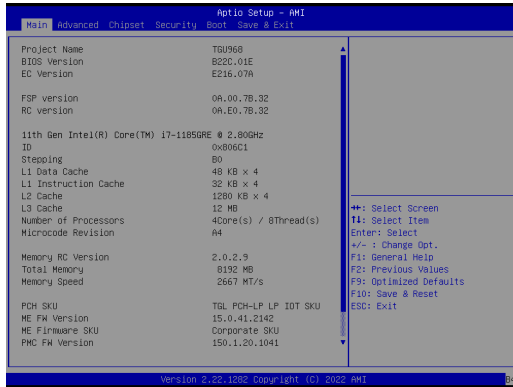
When "►" appears on the left of a particular field, it indicates that a submenu which contains additional options are available for that field. To display the submenu, move the highlight to that field and press <Enter>.

### ► Updating the BIOS

To update the BIOS, you will need the new BIOS file and a flash utility. Please contact technical support or your sales representative for the files and specific instructions about how to update BIOS with the flash utility.

► Main

The Main menu is the first screen that you will see when you enter the BIOS Setup Utility.



**System Date**

The date format is <month>, <date>, <year>. Press "Tab" to switch to the next field and press "-" or "+" to modify the value.

**System Time**

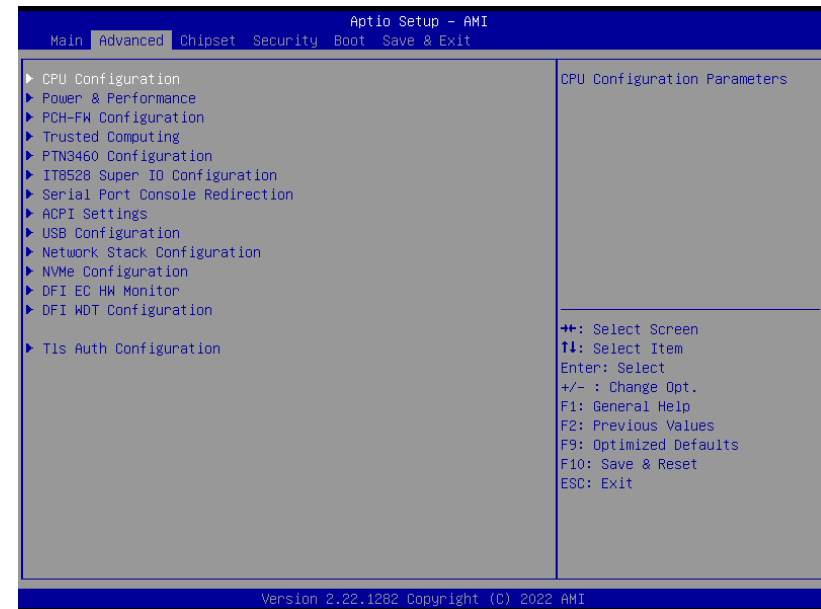
The time format is <hour>, <minute>, <second>. The time is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Hour displays hours from 00 to 23. Minute displays minutes from 00 to 59. Second displays seconds from 00 to 59.

► Advanced

The Advanced menu allows you to configure your system for basic operation. Some entries are defaults required by the system board, while others, if enabled, will improve the performance of your system or let you set some features according to your preference.

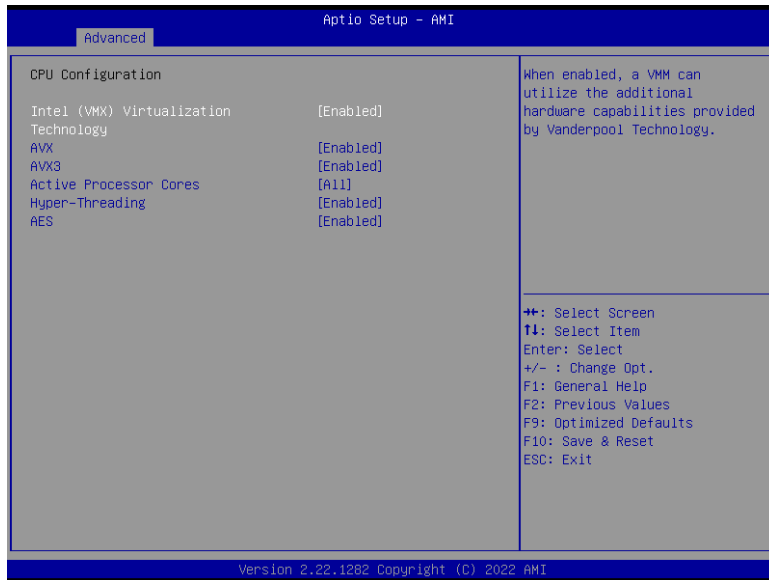


**Important:**  
Setting incorrect field values may cause the system to malfunction.



▶ Advanced

CPU Configuration



**Intel (VMX) Virtualization Technology**

When this field is set to Enabled, the VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

**Active Processor Cores**

Select number of cores to enable in each processor package.

**Hyper-threading**

Enables this field for Windows XP and Linux which are optimized for Hyper-Threading technology. Select disabled for other OSes not optimized for Hyper-Threading technology. When disabled, only one thread per enabled core is enabled.

**Hyper-threading**

Enable/Disable AES (Advanced Encryption Standard)

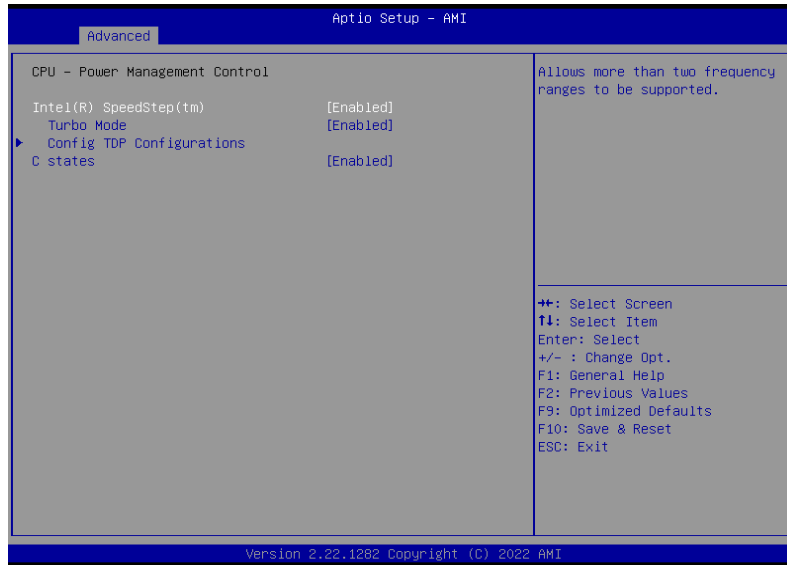
▶ Advanced

Power & Performance



▶ Advanced

Power & Performance ▶ CPU- Power Management Control



**Intel (R) SpeedStep(tm)**

This field is used to enable or disable the Intel SpeedStep® Technology, which helps optimize the balance between system's power consumption and performance. After it is enabled in the BIOS, EIST features can then be enabled via the operating system's power management.

**C states**

Enable or disable CPU Power Management. It allows CPU to enter "C states" when it's not 100% utilized.

▶ Advanced

Power & Performance ▶ CPU- Power Management Control ▶ Config TDP Configurations



**Power Limit 1**

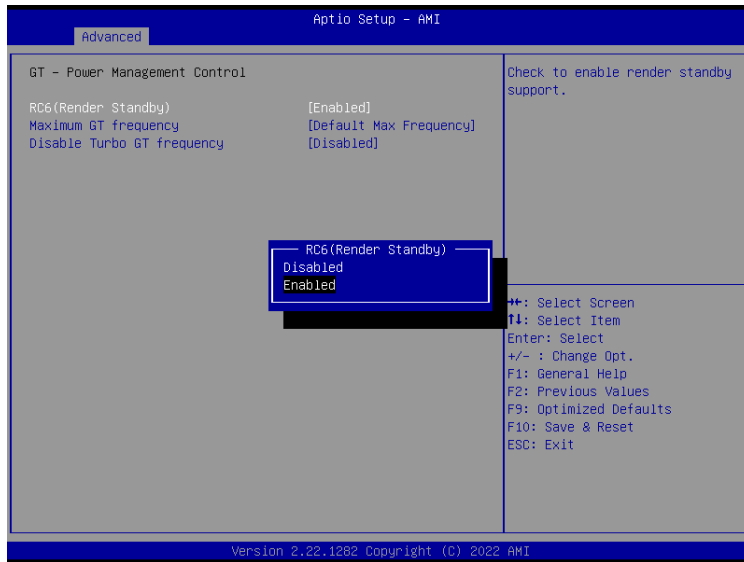
Power Limit 1 in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. Overclocking SKU: Value must be between Max and Min Power Limits (specified by PACKAGE\_POWER\_SKU\_MSR). Other between Min Power Limit and TDP Limit.

**Power Limit 2**

Power Limit 2 value in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. Processor applies control policies such that the package power does not exceed this limit.

▶ Advanced

Power & Performance ▶ GT- Power Management Control



**RC6 (Render Standby)**

Check to enable render standby support.

**Maximum GT frequency**

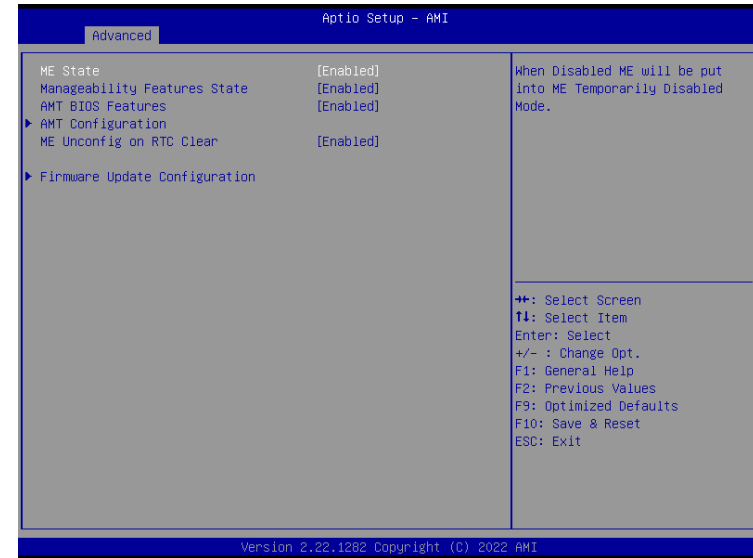
Maximum GT frequency limited by the user. Choose between 100MHz (RPN) and 1350MHZ(RPO). Value beyond the range will be clipped to min/max supported by SKU

**Disable Turbo GT frequency**

Enabled: Disables Turbo GT frequency. Disabled: GT frequency is not limited

▶ Advanced

PCH-FW Configuration



**ME State**

Enable or disable Management Engine. When this field is set to Disabled, ME will be put into ME Temporarily Disabled Mode. The following fields will only appear when ME State is enabled.

**Manageability Features State**

Enable or disable Intel(R) Manageability features. This option disables/enables Manageability Features support in FW. To disable, support platform must be in an unprovisioned state first.

**AMT BIOS Features**

When disabled, AMT BIOS features are no longer supported and user is no longer able to access MEBx Setup. This option does not disable manageability features in FW.

**AMT Configuration**

This section is used to configure Intel(R) Active Management Technology Parameters. Please refer to the following pages.

**ME Unconfig on RTC Clear**

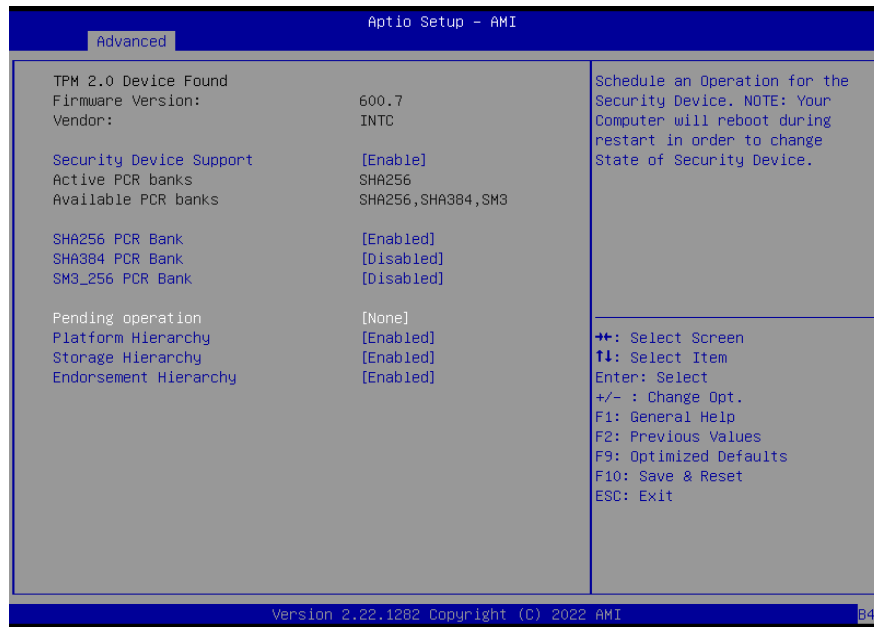
When disabled, ME will not be unconfigured on RTC Clear.

**Firmware Update Configuration**

Please refer to the following pages.

▶ Advanced

### Trusted Computing



#### Security Device Support

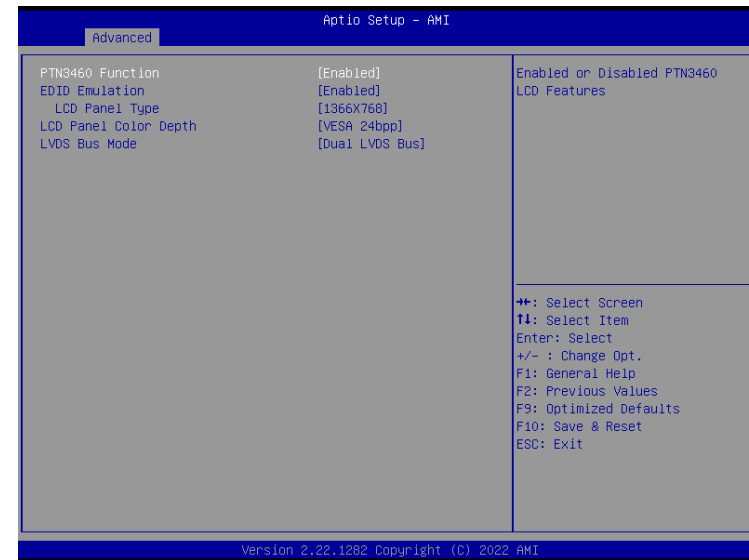
This field is used to enable or disable BIOS support for the security device such as an TPM 2.0 to achieve hardware-level security via cryptographic keys. TCG EFI protocol and INT1A interface will not be available.

#### Pending operation

To clear the existing TPM encryption, select "TPM Clear" and restart the system. This field is not available when "Security Device Support" is disabled. Schedule an Operation for the security Device. NOTE: Your computer will reboot during restart in order to change State of Security Device.

▶ Advanced

### PTN3460 Configuration



#### PTN3460 Function

Enable or Disable PTN3460 LCD Features. When this field is disabled, the following fields will remain hidden.

#### EDID Emulation

Enable or Disable PTN3460 EDID Emulation Mode

#### LCD Panel Type

Select the resolution of the LCD Panel – 800X480, 800X600, 1024X768, 1366X768, 1280X1024, 1920X1080, or 1920X1200.

#### LCD Panel Color Depth

Select the color depth of the LCD Panel – VESA 24bpp, JEIDA 24bpp, VESA and JEIDA 18 bpp.

#### LVDS Bus Mode

Select PTN3460 LVDS BUS Mode – Single LVDS Bus /Dual LVDS Bus



**Note:**

The configuration must match the specifications of your LCD Panel in order for the LCD Panel to display properly.

▶ Advanced

### IT8528 Super IO Configuration



#### Serial Port 1 Configuration

Set Parameters of Serial Port 1 (COMA)

#### Serial Port 2 Configuration

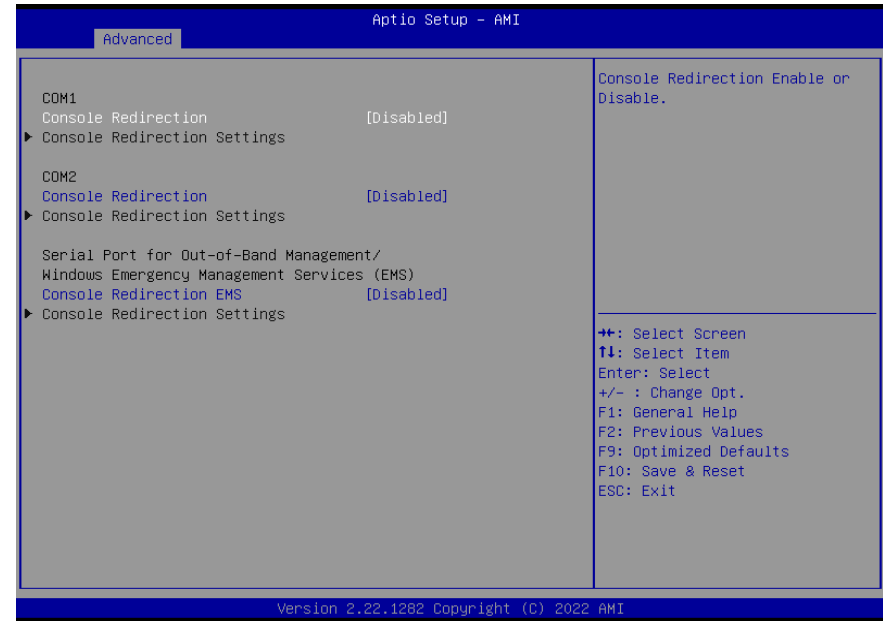
Set Parameters of Serial Port 2 (COMB)



**Note:**  
The sub-menus are detailed in following sections.

▶ Advanced

### Serial Port Console Redirection



#### Console Redirection

By enabling Console Redirection of a COM port, the sub-menu of console redirection settings will become available for configuration as detailed in the following.

► **Advanced**

**Serial Port Console Redirection** ► **Console Redirection Settings**



**Out of Band Mgmt Port**

Microsoft Windows Emergency Management Services (EMS) allows for remote management of a Windows Server OS through a serial port.

**Terminal Type EMS**

Select terminal type: VT100, VT100Plus, VT-UTF8 or ANSI.

**Bits per second EMS**

Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.

Select serial port transmission speed: 9600, 19200, 38400, 57600 or 115200.

**Flow Control EMS**

Select flow control type: None or Hardware RTS/CTS. Flow Control is for RS485 mode and is only supported by Serial Port 1 (COM1).

**Data Bits EMS**

Select data bits: 7 bits or 8 bits.

**Parity EMS**

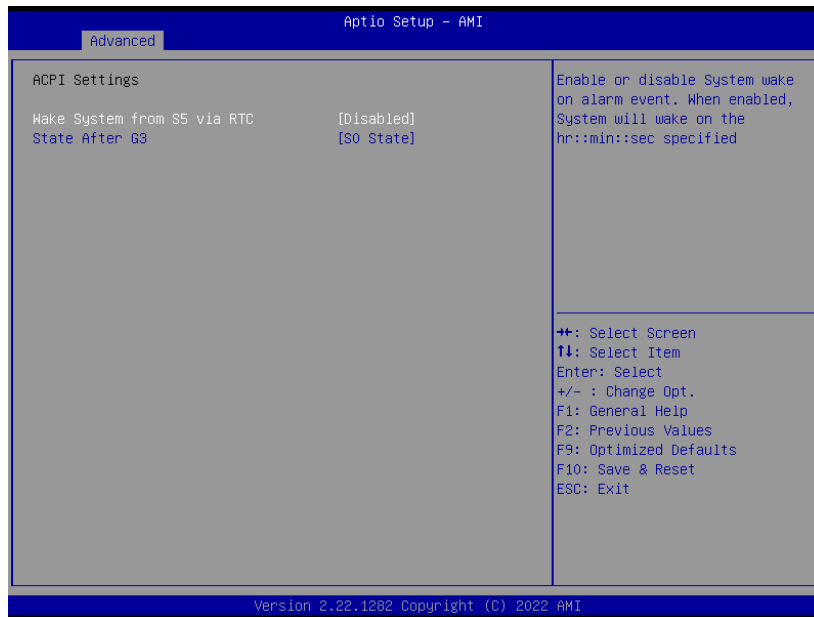
Select parity bits: None, Even, Odd, Mark or Space.

**Stop Bits EMS**

Select stop bits: 1 bit or 2 bits.

▶ Advanced

### ACPI Settings



#### Wake system from S5 via RTC

When Enabled, the system will automatically power up at a designated time every day. Once it's switched to [Enabled], please set up the time of day – hour, minute, and second – for the system to wake up.

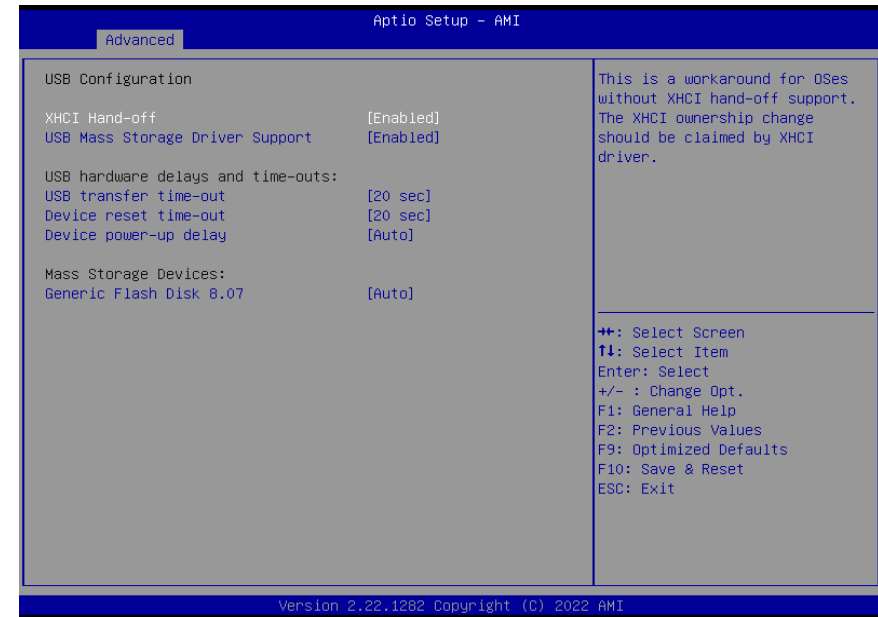
#### State After G3

Select between S0 State, and S5 State. This field is used to specify what state the system is set to return to when power is re-applied after a power failure (G3 state).

- **S0 State** The system automatically powers on after power failure.
- **S5 State** The system enter soft-off state after power failure. Power-on signal input is required to power up the system.
- **Last State** The system returns to the last state right before power failure.

▶ Advanced

### USB Configuration



#### XHCI Hand-off

Enable or disable XHCI Hand-off.

This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.

#### USB Mass Storage Driver Support

Enable or disable USB Mass Storage Driver Support.

#### USB hardware delays and time-outs:

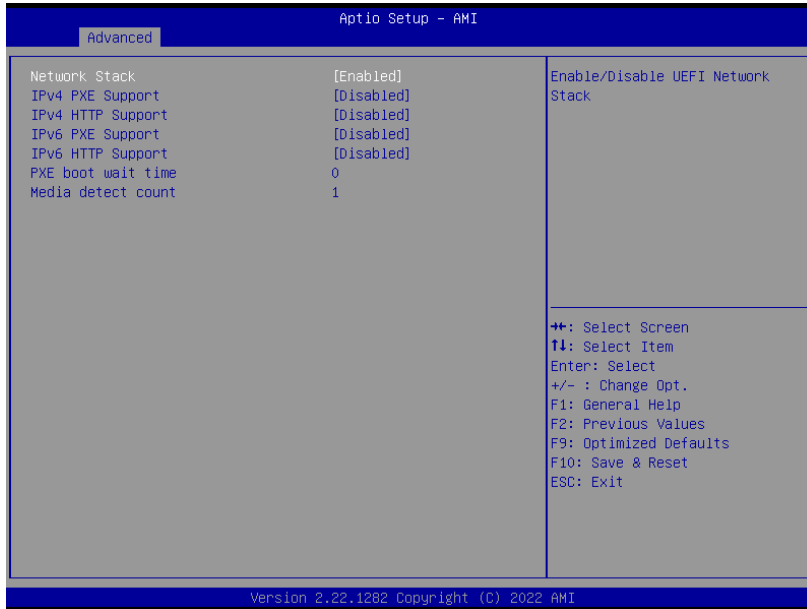
**USB transfer time-out** : The time-out value for Control, Bulk, and Interrupt transfers.

**Device reset time-out** : USB mass storage device Start Unit command time-out.

**Device power-up delay** : Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.

► **Advanced**

**Network Stack Configuration**



► **Advanced**

**Network Stack**

Enable or disable UEFI network stack. The following fields will appear when this field is enabled.

**IPv4 PXE Support**

Enable or disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.

**IPv4 HTTP Support**

Enable or disable IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be available.

**IPv6 PXE Support**

Enable or disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.

**IPv6 HTTP Support**

Enable or disable IPv6 HTTP boot support. If disabled, IPv6 HTTP boot support will not be available.

**PXE boot wait time**

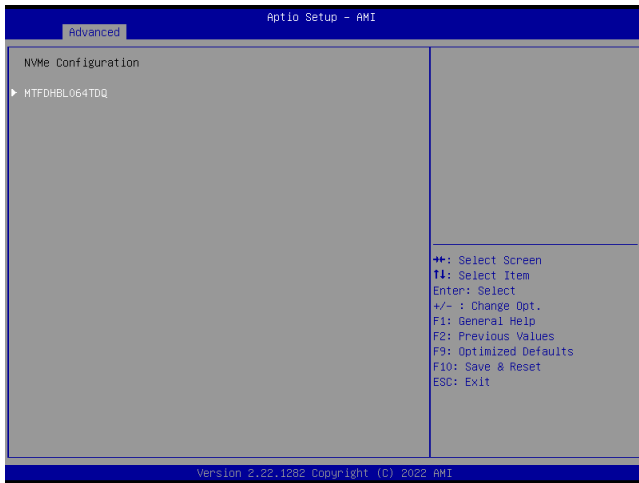
Set the wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.

**Media detect count**

Set the number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.

▶ **Advanced**

**NVMe Configuration**

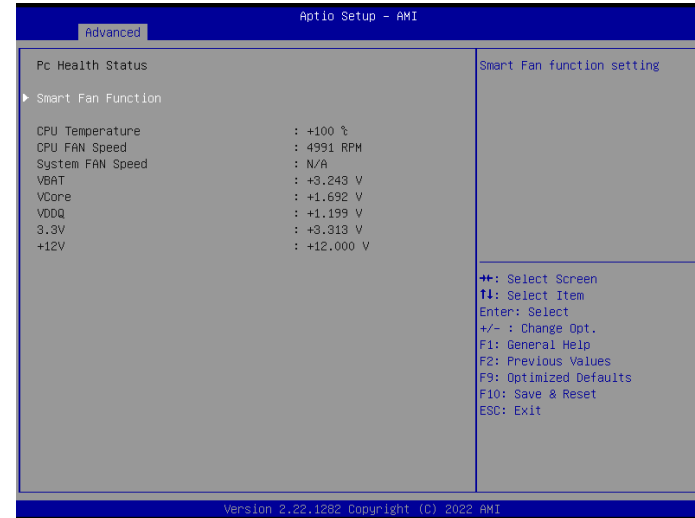


**NVMe Configuration**

NVMe Device Options Settings

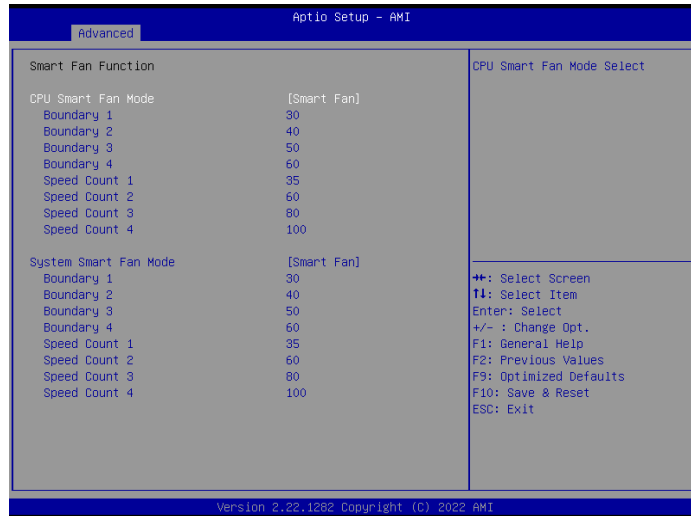
▶ **Advanced**

**DFI EC HW Monitor**



▶ Advanced

DFI EC HW Monitor ▶ Smart Fan Function



Smart Fan is a fan speed moderation strategy dependent on the current system temperature. When the system temperature goes higher than the Boundary setting, the fan speed will be turned up to the setting of the Fan Speed Count that bears the same index as the Boundary field.

▼ CPU/SYS Smart Fan Mode = [Smart Fan]

**Boundary 1 to Boundary 4**

Set the boundary temperatures that determine the fan speeds accordingly, the value ranging from 0-127°C. For example, when the system temperature reaches Boundary 1 setting, the fan speed will be turned up to the designated speed of the Fan Speed Count 1 field.

**Fan Speed Count 1 to Fan Speed Count 4**

Set the fan speed, the value ranging from 1-100%, 100% being full speed. The fans will operate according to the specified boundary temperatures above-mentioned.

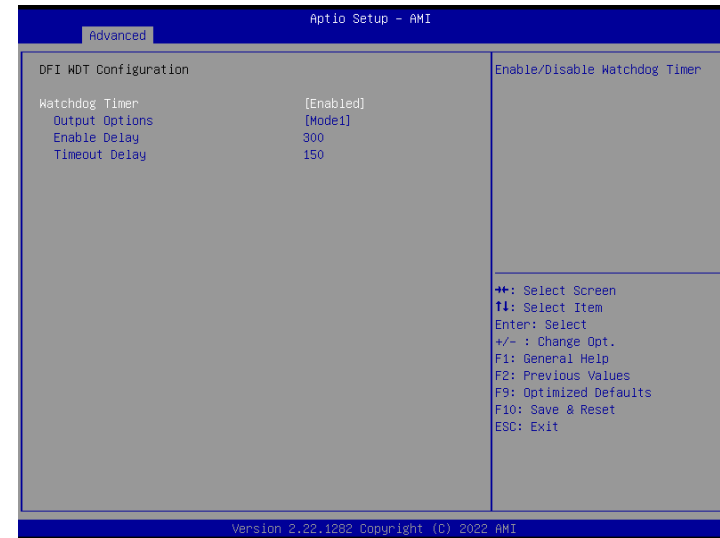
▼ CPU/SYS Smart Fan Mode = [Manual Mode]

**Fix Fan Speed Count**

Set the fan speed, the value ranging from 1-100%, 100% being full speed. The fans will always operate at the specified speed regardless of gauged temperatures.

▶ Advanced

DFI WDT Configuration



**Watchdog Timer**

Enable or disable watchdog timer.

**Output Options**

Mode1 = A Watchdog timeout causes the system to be reset.  
Mode2 = WDT pin goes high upon timeout of the watchdog timer.  
Mode3 = Generate NMI upon timeout of the watchdog timer.

**Enable Delay**

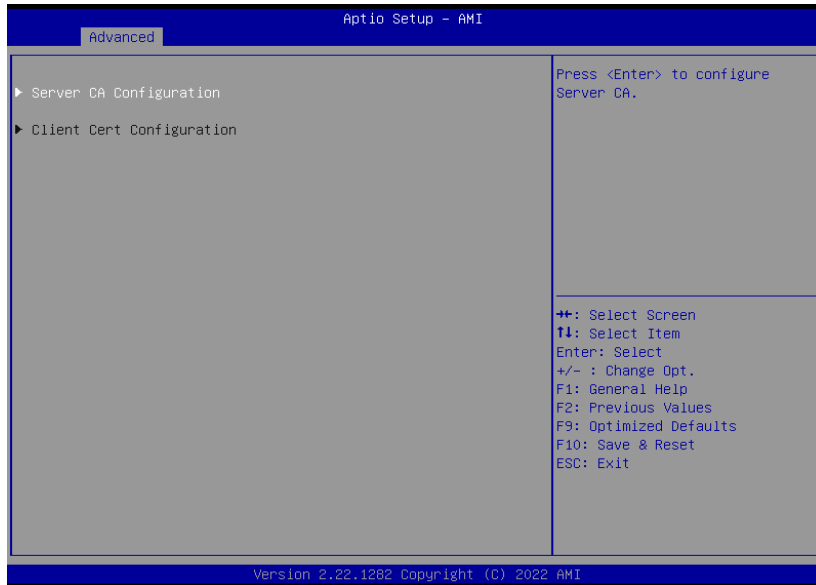
The enable delay allows time for the OS to boot and the application to load and initialize. The unit is 1 sec.

**Timeout Delay**

The timeout delay allows time for period of the watchdog timer. The unit is 0.1 sec.

► **Advanced**

**Tls Auth Configuration**



**Server CA Configuration**

Press <Enter> to configure Server CA.

► Chipset



Please select a submenu and press Enter. The submenus are detailed in the following pages.

► Chipset

System Agent (SA) Configuration



**Memory Configuration**

Memory Configuration Parameter.

**Graphics Configuration**

Settings about graphic.

**VMD setup menu**

VMD Configuration Settings

**PCI Express Configuration :**

**VT-d**

VT-d capability.

**X2APIC Opt Out**

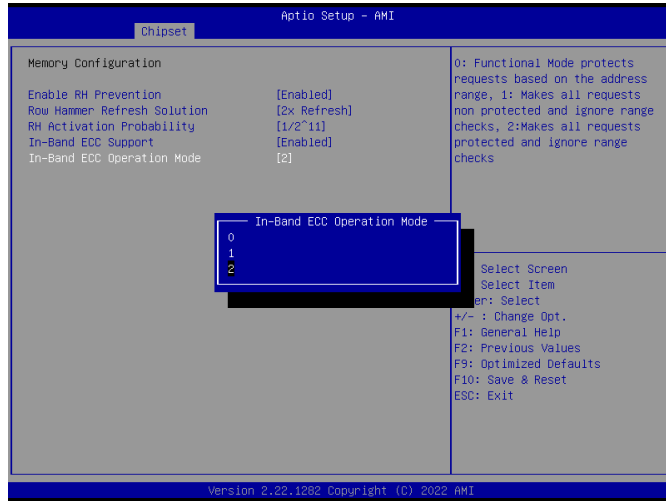
Enable/Disable X2APIC\_OPT\_OUT bit

**DMA Control Guarantee**

Enable/Disable DMA\_Control\_Guarantee bit

► Chipset

System Aget (SA) Configuration ► Memory Configuration



**Enable RH Prevention**

Actively prevent Row Hammer.

**Row Hammer Refresh Solution**

Type of Refresh Rate used to prevent Row Hammer: 2x Refresh, 4x Refresh or NORMAL Refresh.

**RH Activation Probability**

Used to adjust MC for Hardware RHP, select between:  $1/2^1 \sim 1/2^{15}$

**In-Band ECC Support**

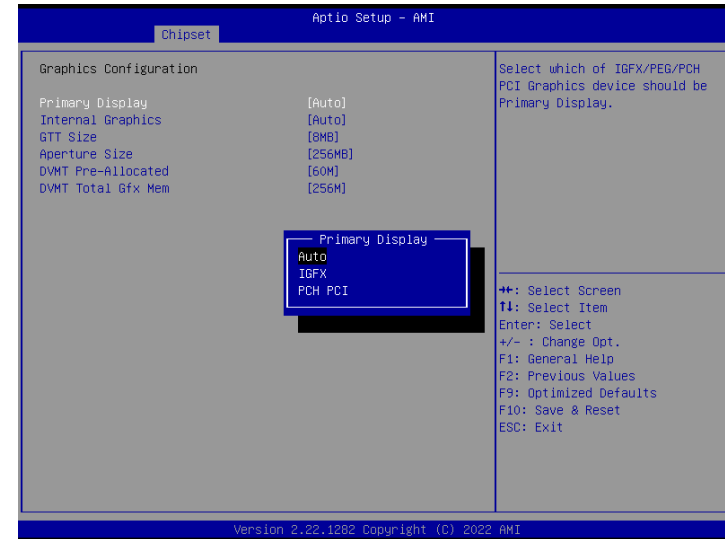
Enable/Disable In-Band ECC. Either the IBECC or the TME can be enabled.

**In-Band ECC Operation Mode**

0: Functional Mode protects requests based on the address range  
1: Makes all requests non protected and ignore range checks  
2: Makes all requests protected and ignore range checks

► Chipset

System Aget (SA) Configuration ► Graphics Configuration



**Primary Display**

Select which of IGFX/PEG/PCH PCI Graphics device should be Primary Display.

**Internal Graphics**

Keep IGFX enabled based on the setup options.

**GTT Size**

Select the GTT Size.

**Aperture Size**

Select the Aperture Size. Note : Above 4GB MMIO BIOS assignment is automatically enabled when selecting 2048MB aperture. To use this feature, please disable CSM Support.

**DVMT Pre-Allocated**

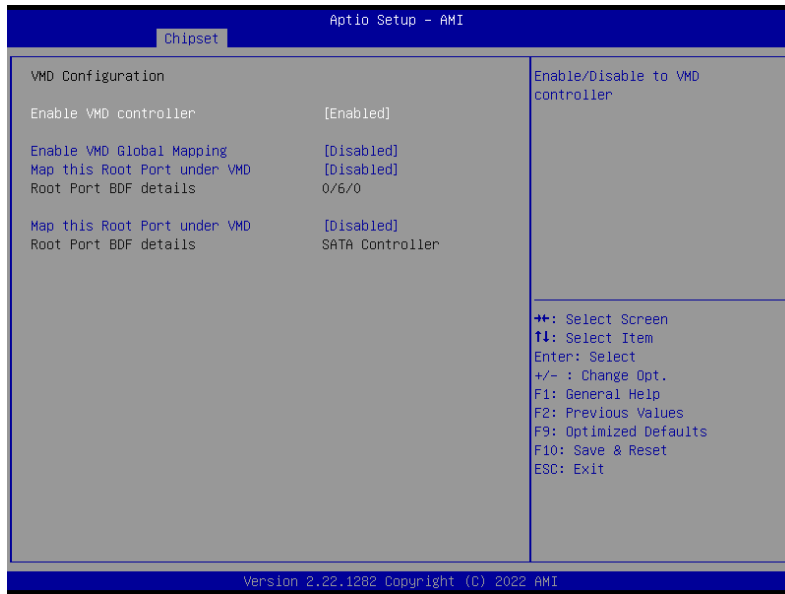
Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.

**DVMT Total Gfx Mem**

Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device.

► Chipset

System Agent (SA) Configuration ► VMD Configuration



**Enable VMD controller**

Enable/Disable to VMD controller.

**Enable VMD Global Mapping**

Enable/Disable to VMD Global Mapping

**Map this Root Port under VMD**

Map/UnMap this Root Port to VMD.

► Chipset

PCH-IO Configuration



**PCI Express Configuration**

PCI Express Configuration Settings

**SATA And RST Configuration**

SATA Device Options Settings

**HD Audio Configuration**

HD Audio Subsystem Configuration Settings

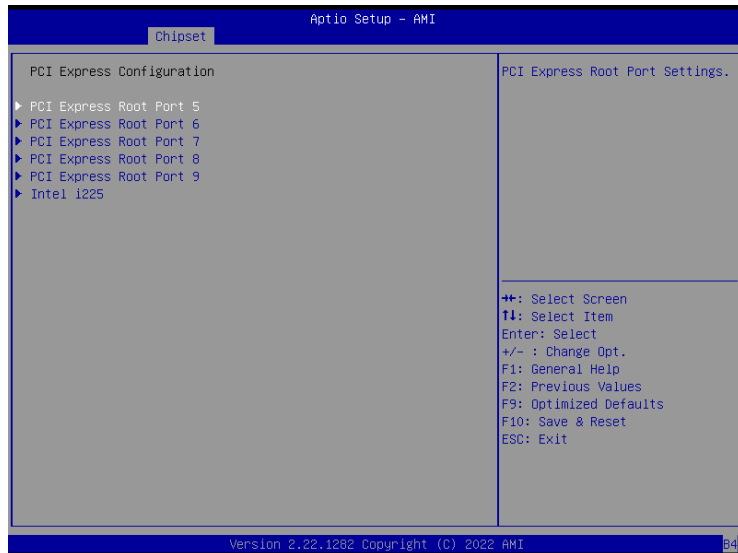


**Note:**

The sub-menus are detailed in following sections.

► Chipset

PCH-IO Configuration ► PCI Express Configuration



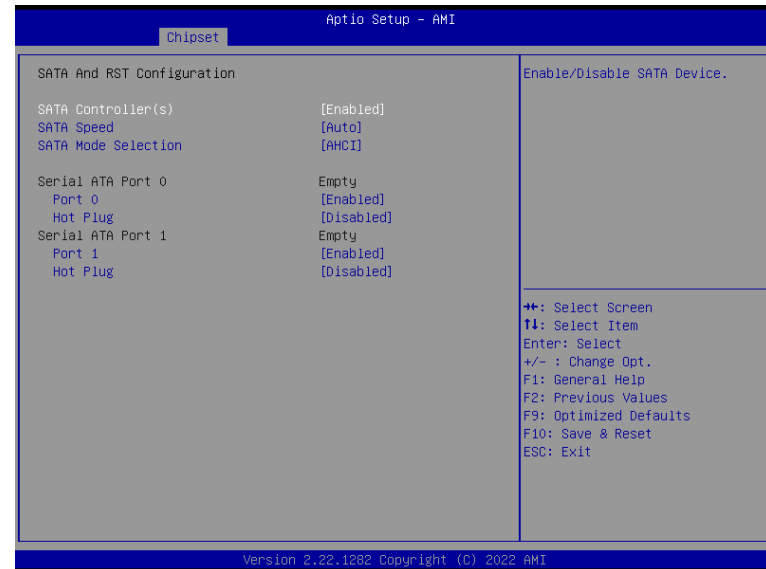
Select one of the PCI Express channels and press enter to configure the following settings.

**PCI Express Root Port 5~9 & Intel i225**

Control the PCI Express Root Port.

► Chipset

PCH-IO Configuration ► SATA And RST Configuration



**SATA Controller(s)**

This field is used to enable or disable the Serial ATA controller.

**SATA Speed**

This field is used to select SATA speed generation limit: Auto, Gen1, Gen2 or Gen3.

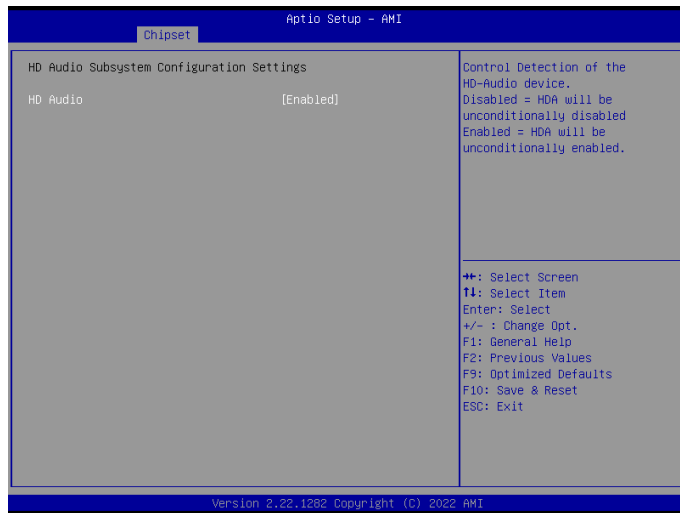
**SATA Mode Selection**

The mode selection determines how the SATA controller(s) operates.

- **AHCI** This option allows the Serial ATA controller(s) to use AHCI (Advanced Host Controller Interface).

► Chipset

PCH-IO Configuration ► HD Audio Configuration

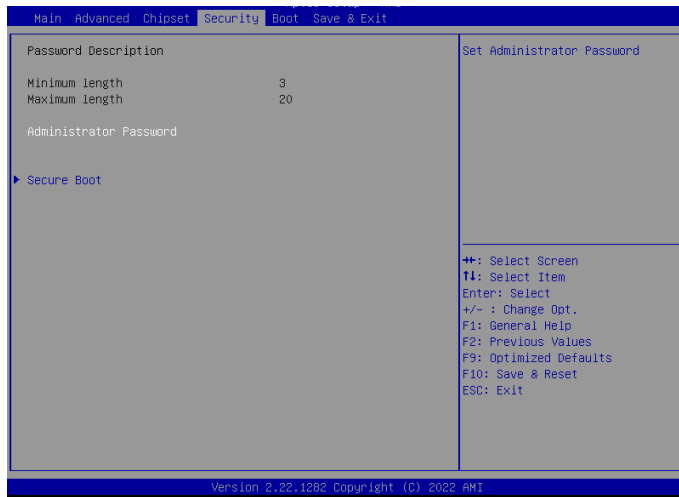


### HD Audio

Control the detection of the HD Audio device.

- **Disabled** HDA will be unconditionally disabled.
- **Enabled** HDA will be unconditionally enabled.

► Security



**Administrator Password**

Set the administrator password. To clear the password, input nothing and press enter when a new password is asked. Administrator Password will be required when entering the BIOS.

**User Password**

Set the user password. To clear the password, input nothing and press enter when a new password is asked. User Password will be required when powering up the system.

► Security



**Secure Boot**

The Secure Boot store a database of certificates in the firmware and only allows the Oses with authorized signatures to boot on the system. To activate Secure Boot, please make sure that "Secure Boot" is "[Enabled]", Platform Key (PK) is enrolled, "System Mode" is "User", and CSM is disabled. After enabling/disabling Secure Boot, please save the configuration and restart the system. When configured and activated correctly, the Secure Boot status will be "Active".

**Secure Boot Customization**

Select the secure boot mode – Standard or Custom. When set to Custom, the following fields will be configurable for the user to manually modify the key database.

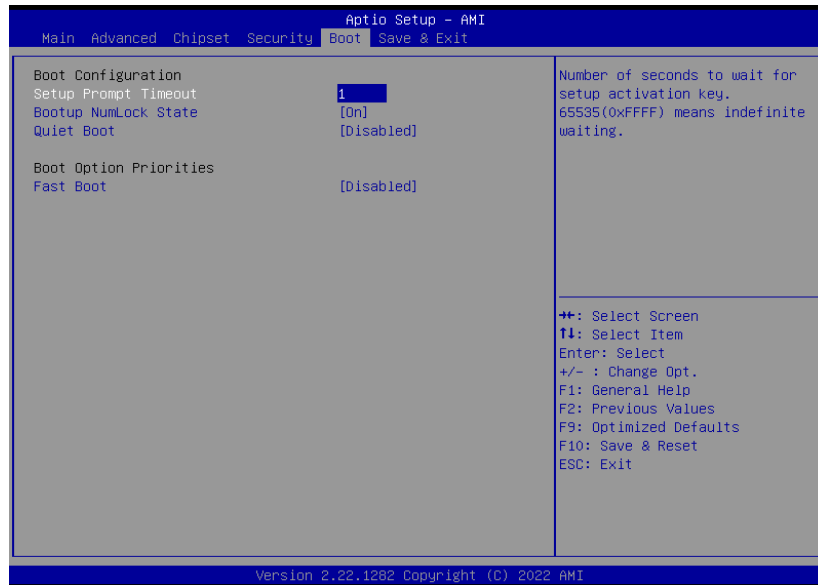
**Restore Factory Keys**

Force system to User Mode. Load OEM-defined factory defaults of keys and databases onto the Secure Boot. Press Enter and a prompt will show up for you to confirm.

**Reset To Setup Mode**

Clear the database from the NVRAM, including all the keys and signatures installed in the Key Management menu. Press Enter and a prompt will show up for you to confirm.

► Boot



**Setup Prompt Timeout**

Set the number of seconds to wait for the setup activation key. 65535 (0xFFFF) denotes indefinite waiting.

**Bootup NumLock State**

Select the keyboard NumLock state: On or Off.

**Quiet Boot**

This section is used to enable or disable quiet boot option.

**Boot Option Priorities**

Rearrange the system boot order of available boot devices.

**Fast Boot**

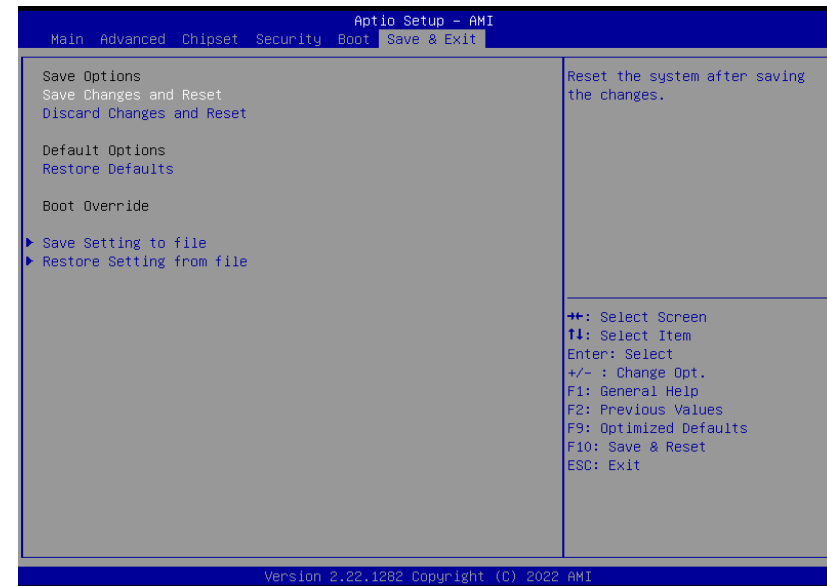
Enables or disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.



**Note:**

If “Boot option filter” of “CSM Configuration” is set to “UEFI and Legacy” or “UEFI only”, and “Quiet Boot” is set to enabled, “BGRT Logo” will show up for configuration. Refer to the Advanced > CSM Configuration submenu for more information.

► Save & Exit



**Save Changes and Reset**

To save the changes, select this field and then press <Enter>. A dialog box will appear. Select Yes to reset the system after saving all changes made.

**Discard Changes and Reset**

To discard the changes, select this field and then press <Enter>. A dialog box will appear. Select Yes to reset the system setup without saving any changes.

**Restore Defaults**

To restore and load the optimized default values, select this field and then press <Enter>. A dialog box will appear. Select Yes to restore the default values of all the setup options.

**Boot Override**

Move the cursor to an available boot device and press Enter, and then the system will immediately boot from the selected boot device. The Boot Override function will only be effective for the current boot. The “Boot Option Priorities” configured in the Boot menu will not be changed.

- **Save Setting to file** Select this option to save BIOS configuration settings to a USB flash device.
- **Restore Setting from file** This field will appear only when a USB flash device is detected. Select this field to restore setting from the USB flash device.