DFI

RK701

Rockchip Processor (Qseven)

User's Manual

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Trademarks

Qseven Specification Reference

Qseven Specification Reference Specification,
please refer to: https://sget.org/standards/qseven/

FCC and DOC Statement on Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio TV technician for help.

Notice:

- The changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.
- Shielded interface cables must be used in order to comply with the emission limits.

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About this Manual

This manual can be downloaded from the website.

The manual is subject to change and update without notice, and may be based on editions that do not resemble your actual products. Please visit our website or contact our sales representatives for the latest editions.

Warranty

- Warranty does not cover damages or failures that occur from misuse of the product, inability to use the product, unauthorized replacement or alteration of components and product specifications.
- The warranty is void if the product has been subjected to physical abuse, improper installation, modification, accidents or unauthorized repair of the product.
- Unless otherwise instructed in this user's manual, the user may not, under any circumstances, attempt to perform service, adjustments or repairs on the product, whether in or out of warranty. It must be returned to the purchase point, factory or authorized service agency for all such work.
- We will not be liable for any indirect, special, incidental or consequential damages to the product that has been modified or altered.

Static Electricity Precautions

It is quite easy to inadvertently damage your PC, system board, components or devices even before installing them in your system unit. Static electrical discharge can damage computer components without causing any signs of physical damage. You must take extra care in handling them to ensure against electrostatic build-up.

- To prevent electrostatic build-up, leave the system board in its anti-static bag until you are ready to install it.
- Wear an antistatic wrist strap.
- Do all preparation work on a static-free surface.
- Hold the device only by its edges. Be careful not to touch any of the components, contacts or connections.
- Avoid touching the pins or contacts on all modules and connectors. Hold modules or connectors by their ends.

Important:
Electrostatic discharge (ESD) can damage your processor, disk drive and other components. Perform the upgrade instruction procedures described at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

Safety Measures

- To avoid damage to the system, use the correct AC input voltage range.
- To reduce the risk of electric shock, unplug the power cord before removing the system chassis cover for installation or servicing. After installation or servicing, cover the system chassis before plugging the power cord.

About the Package

The package contains the following items. If any of these items are missing or damaged, please contact your dealer or sales representative for assistance.

The accessories in the package may not come similar to the information listed below. This may differ in accordance with the sales region or models in which it was sold. For more information about the standard package in your region, please contact your dealer or sales representative.

- RK701 Board
- Heat Sink

Optional Items

The board and accessories in the package may not come similar to the information listed above. This may differ in accordance with the sales region or models in which it was sold. For more information about the standard package in your region, please contact your dealer or sales representative.

- Qseven Carrier Board
- Heat Spreader

Before Using the System Board

Before using the system board, prepare basic system components.
If you are installing the system board in a new system, you will need at least the following internal components.

- Storage devices such as hard disk drive, etc.

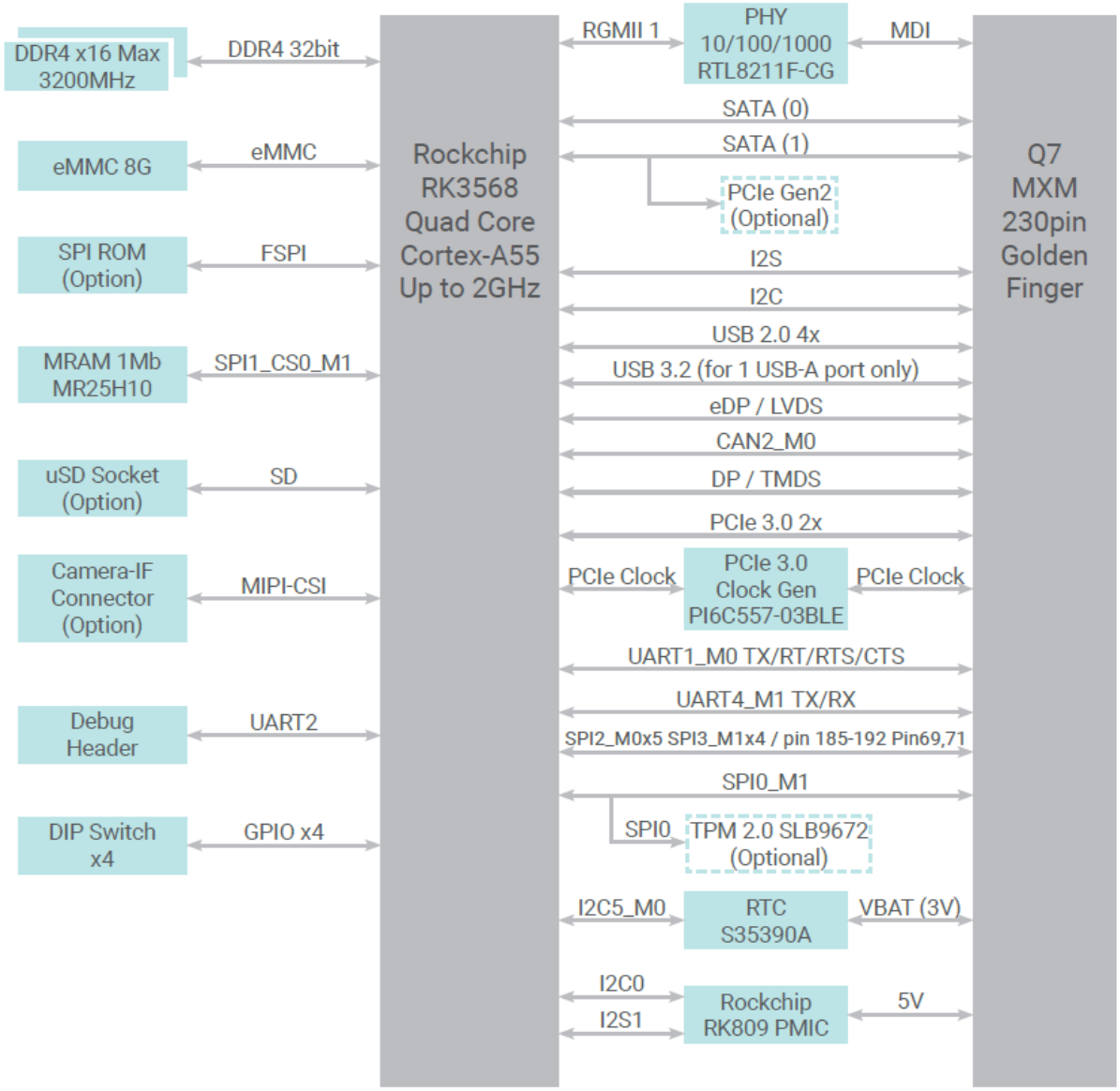
You will also need external system peripherals you intend to use which will normally include at least a keyboard, a mouse and a video display monitor.

Chapter 1 - Introduction

▶ Specification

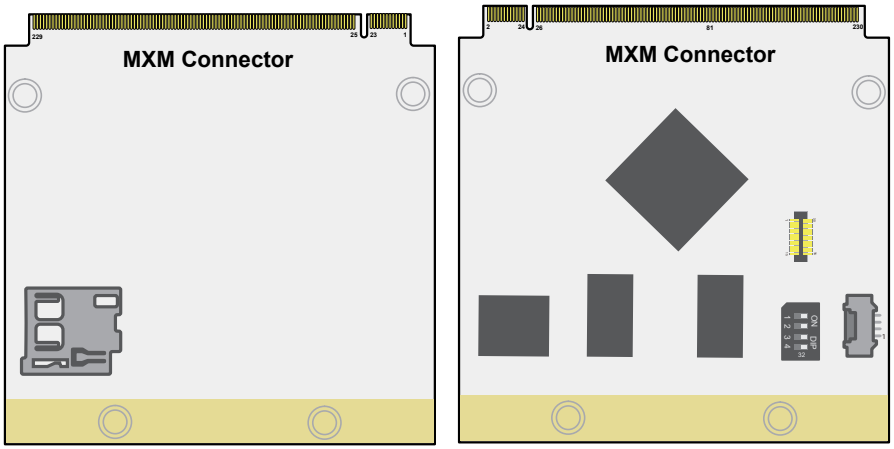
SYSTEM	Processor	Rockchip RK3568 quad-core Cortex-A55 @2.0GHz Rockchip RK3568J quad-core Cortex-A55 @1.8GHz
	Memory	2GB/4GB/8GB DDR4 Memory Down 3200MHZ
GRAPHICS	Controller	G52 2EE
	Feature	OpenGL ES1.1/2.0/3.0/3.1/3.2, Vulkan 1.1, OpenCL 2.0
	Display	1 x eDP/LVDS 1 x DP/TMDS HDMI: resolution up to 4096 x 2160 @30HZ LVDS: resolution up to1024 x 600 @60Hz eDP: resolution up to 3840 x 2160 @60Hz
	Dual Displays	eDP/LVDS + DP/TMDS
EXPANSION	Interface	2 x PCIe x1 (Gen 3) 1 x PCIe x1 (Gen 2) 1 x uSD (available upon request) 1 x I2C 2 x SPI (SPI0 set to TPM 2.0) 1 x CAN bus 2 x UART 1 x MIPI-CSI (available upon request)
AUDIO	Interface	HD Audio
ETHERNET	Controller	1 x RTL8211F-CG
I/O	USB	1 x USB 3.2 4 x USB 2.0
	SATA	2 x SATA 3.0 (up to 6Gb/s, SATA 1 Co-Lay PCIE Gen 2)
	eMMC	Supports up to 128GB eMMC, NC as default eMMC 5.1, BGA-153 Ball 8~128G(MLC mode)
	GPIO	1 x 4-bit GPIO
SECURITY	TPM	TPM 2.0
Power	Type	5V, 5VSB, VCC_RTC
	Consumption	TBD
OS SUPPORT **(UEFI ONLY)**	Linux	Linux
ENVIRONMENT	Temperature	Operating: 0 to 60°C, -40 to 85°C
	Humidity	Operating: 5 to 90% RH Storage: 5 to 90% RH
	MTBF	TBD
MECHANICAL	Dimensions	Qseven Form Factor 70mm (2.76") x 70mm (2.76")
	Compliance	Qseven Specification Revision 2.1
STANDARDS AND CERTIFICATIONS	Certification	CE, FCC Class B, RoHS

▶ Block Diagram



Chapter 2 - Pin Assignment

▶ Board Layout

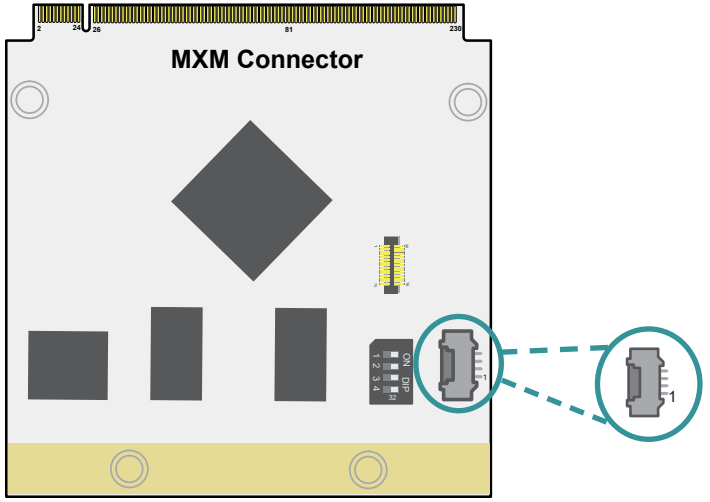


TOP VIEW BOTTOM VIEW

Important:
Boards, and other components. Perform installation procedures at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

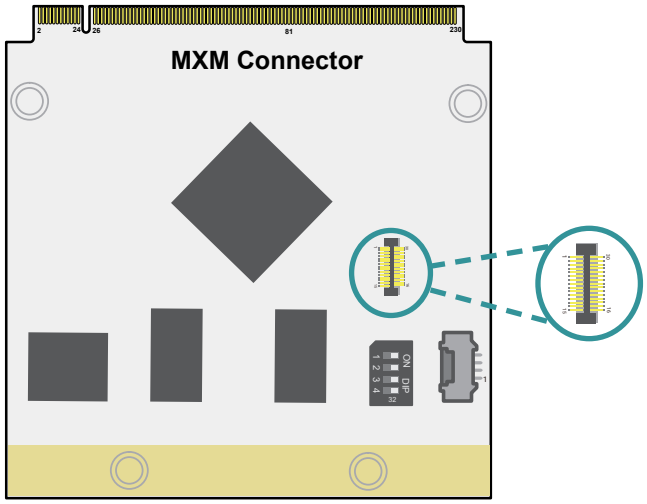
▶ Pin Assignments

UART Debug



Pin	Assignment
1	3V3
2	UART2_RXD
3	UART2_TXD
4	GND

Camera



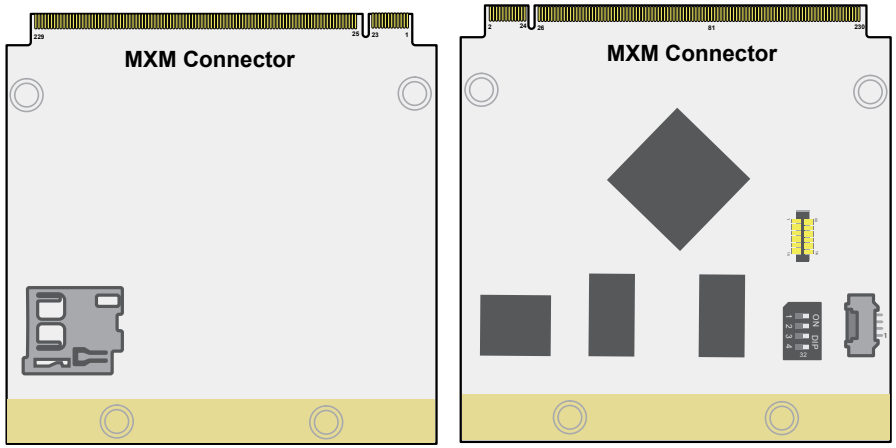
Pin	Assignment	Pin	Assignment
1	GND	30	MIPI_CSI_RX_CLK0N
2	MIPI_CSI_RX_D0P	29	MIPI_CSI_RX_CLK0P
3	MIPI_CSI_RX_D0N	28	GND
4	GND	27	MIPI_CSI_RX_D1P
5	MIPI_CSI_RX_D2P	26	MIPI_CSI_RX_D1N
6	MIPI_CSI_RX_D2N	25	GND
7	GND	24	+1.8V
8	MIPI_CSI_RX_D3P	23	GND
9	MIPI_CSI_RX_D3N	22	+1.2V
10	GND	21	I2C2_SDA
11	CIF_CLKOUT	20	I2C2_SCL
12	MIPI_CSI_RST#	19	GND
13	GND	18	+2.8V
14	MIPI_CAM0_GPIO3_D5	17	+2.8V
15	GND	16	GND

Chapter 3 - Hardware Installation

▶ Connector

The MXM Connector

The MXM connector is used to interface with the carrier board. Insert RK701 to the MXM connector on the carrier board. Refer to the following pages for the pin functions of this connector.



TOP VIEW BOTTOM VIEW

The table below is a comprehensive list of all signal pins supported on the 230-pin MXM connectors.

Pin	Signal	Pin	Signal
1	GND_1	2	GND_2
3	GBE_MDI3-	4	GBE_MDI2-
5	GBE_MDI3+	6	GBE_MDI2+
7	GBE_LINK100#	8	GBE_LINK1000#
9	GBE_MDI1-	10	GBE_MDI0-
11	GBE_MDI1+	12	GBE_MDI0+
13	N/A	14	GBE_ACT#
15	N/A	16	N/A
17	PCIE1_WAKE#	18	N/A
19	GPO0	20	PWRBTN#
21	GPII1	22	GPII0
23	GND_23	24	GND_24
25	GND_25	26	CB_PWROK
27	GPII2	28	RSTBTN#
29	SATA0_TX+	30	SATA1_TX+
31	SATA0_TX-	32	SATA1_TX-
33	SATA_ACT#	34	GND_34
35	SATA0_RX+	36	SATA1_RX+
37	SATA0_RX-	38	SATA1_RX-
39	GND_39	40	GND_40
41	BOOT_ALT#	42	SDIO_CLK#
43	SDIO_CD#	44	N/A
45	SDIO_CMD	46	N/A
47	SDIO_PWREN	48	SDIO_DAT1
49	SDIO_DAT0	50	SDIO_DAT3

Pin	Signal	Pin	Signal
51	SDIO_DAT2	52	UART1_TX
53	UART2_TX	54	UART1_RX
55	UART2_RX	56	N/A
57	GND_57	58	GND_58
59	I2S_LRCK	60	GP1_I2C_CLK
61	I2S_MCLK	62	GP1_I2C_DAT
63	I2S_SCLK	64	GPIO
65	I2S_SDI	66	GP0_I2C_CLK
67	I2S_SDO	68	GP0_I2C_DAT
69	PCIE20_REFCLKP	70	WDTRIG#
71	PCIE20_REFCLKN	72	WDOUT
73	GND_73	74	GND_74
75	USB_SSTX0-	76	USB_SSRX0-
77	USB_SSTX0+	78	USB_SSRX0+
79	N/A	80	N/A
81	N/A	82	N/A
83	N/A	84	N/A
85	N/A	86	N/A
87	USB_P3-	88	USB_P2-
89	USB_P3+	90	USB_P2+
91	USB_VBUS	92	USB3_OTG0ID
93	USB_P1-	94	USB_P0-
95	USB_P1+	96	USB_P0+
97	GND_97	98	GND_98
99	eDP0_TX0+	100	LVDS_B0+
101	eDP0_TX0-	102	LVDS_B0-
103	eDP0_TX1+	104	LVDS_B1+
105	eDP0_TX1-	106	LVDS_B1-
107	eDP0_TX2+	108	LVDS_B2+
109	eDP0_TX2-	110	LVDS_B2-

Pin	Signal	Pin	Signal
111	LVDS_PPEN	112	LVDS_BLEN
113	eDP0_TX3+	114	LVDS_B3+
115	eDP0_TX3-	116	LVDS_B3-
117	GND_117	118	GND_118
119	eDP0_AUX+	120	LVDS_B_CLK+
121	eDP0_AUX-	122	LVDS_B_CLK-
123	BKLTCTL	124	HDMI_CEC_IN
125	N/A	126	LVDS_BLC_DAT
127	N/A	128	LVDS_BLC_CLK
129	CAN0_TX	130	CAN0_RX
131	HDMI_CLK+	132	USB3_OTG0TX-
133	HDMI_CLK-	134	USB3_OTG0TX+
135	GND_135	136	GND_136
137	HDMI_LANE1+	138	N/A
139	HDMI_LANE1-	140	N/A
141	GND_141	142	GND_142
143	HDMI_LANE0+	144	USB3_OTG0RX-
145	HDMI_LANE0-	146	USB3_OTG0RX+
147	GND_147	148	GND_148
149	HDMI_LANE2+	150	HDMI_CTRL_DAT
151	HDMI_LANE2-	152	HDMI_CTRL_CLK
153	HDMI_HPD#	154	N/A
155	PCIE_CLK_REF+	156	PCIE_WAKE#
157	PCIE_CLK_REF-	158	PCIE_RST#
159	GND_159	160	GND_160
161	N/A	162	N/A
163	N/A	164	N/A
165	GND_165	166	GND_166
167	PCIE2_TX+	168	PCIE2_RX+
169	PCIE2_TX-	170	PCIE2_RX-

Pin	Signal	Pin	Signal
171	UART0_TX	172	UART0_RTS#
173	PCIE1_TX+	174	PCIE1_RX+
175	PCIE1_TX-	176	PCIE1_RX-
177	UART0_RX	178	UART0_CTS#
179	PCIE0_TX+	180	PCIE0_RX+
181	PCIE0_TX-	182	PCIE0_RX-
183	GND_183	184	GND_184
185	SPI0_MOSI	186	SPI0_CS0#
187	SPI0_MISO	188	SPI0_CS1#
189	SPI0_CLK	190	GPIO5
191	GPIO6	192	GPIO7
193	VCC_RTC	194	SPK_OUT+
195	SPK_OUT-	196	PWM_OUT1
197	GND_197	198	GND_198
199	SPI2_MOSI	200	SPI2_CS0#
201	SPI2_MISO	202	SPI2_CS1#
203	SPI2_CLK	204	N/A
205	VCC_5V	206	VCC_5V
207	N/A	208	UART3_RX
209	UART3_TX	210	N/A
211	N/A	212	N/A
213	N/A	214	N/A
215	N/A	216	N/A
217	N/A	218	N/A
219	VCC	220	VCC
221	VCC	222	VCC
223	VCC	224	VCC
225	VCC	226	VCC
227	VCC	228	VCC
229	VCC	230	VCC

▶ MXM Connector Signal Description

Pin Types
I Input Pin
O Output Pin
I/O Bi-directional input / output Pin
OD Open drain
PP Push Pull
NC Not Connected

PCI Express Interface Signals Descriptions						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**DFI-RK701**	**Carrier Board**	**Description**
PCIE0_RX+	180	I PCIE	AC coupled off Module		**Device** - Connect AC Coupling cap 0.1uF **Slot** - Connect to PCIE Conn pin	PCI Express channel 0, Receive Input differential pair.
PCIE0_RX-	182					
PCIE0_TX+	179	O PCUE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express channel 0, Transmit Output differential pair.
PCIE0_TX-	181			AC Coupling capacitor		
PCIE_CLK_REF+	155	O PCUE	PCIE		Connect to PCIE device, **PCIe CLK Buffer** or slot	Reference clock output for all PCI Express and PCI Express Graphics lanes.
PCIE_CLK_REF-	157					
PCIE_WAKE#	156	I CMOS	3.3V Suspend/3.3V			PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup.
PCIE_RST#	158	O CMOS	3.3V/3.3V			Reset Signal for external devices.

Express Card Support Pins						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**DFI-RK701**	**Carrier Board**	**Description**
UART_RXD	177	I CMOS	3.3V			UART RXD
UART_TXD	171	O CMOS	3.3V			UART TXD
UART_CTS	178	I CMOS	3.3V			UART CTS
UART_RTS	172	O CMOS	3.3V			UART RTS

Gigabit Ethernet Signals						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**DFI-RK701**	**Carrier Board**	**Description**
GBE_MDI0+	12	I/O Analog	3.3V max Suspend		Connect to Magnetics Module MDI0+/-	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. Some pairs are unused in some modes, per the following: 1000BASE-T 100BASE-TX 10BASE-T MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-
GBE_MDI0-	10					
GBE_MDI1+	11	I/O Analog	3.3V max Suspend		Connect to Magnetics Module MDI1+/-	
GBE_MDI1-	9					
GBE_MDI2+	6	I/O Analog	3.3V max Suspend		Connect to Magnetics Module MDI2+/-	
GBE_MDI2-	4					
GBE_MDI3+	5	I/O Analog	3.3V max Suspend		Connect to Magnetics Module MDI3+/-	
GBE_MDI3-	3					
GBE_LINK#	13	OD CMOS	3.3V Suspend/3.3V		NC	Gigabit Ethernet Controller 0 link indicator, active low.
GBE_LINK100#	7	OD CMOS	3.3V Suspend/3.3V		Connect to LED and **recommend** current limit resistor 150Ω to 3.3VSB	Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.
GBE_LINK1000#	8	OD CMOS	3.3V Suspend/3.3V		Connect to LED and **recommend** current limit resistor 150Ω to 3.3VSB	Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.
GBE_ACT#	14	OD CMOS	3.3V Suspend/3.3V		Connect to LED and **recommend** current limit resistor 150Ω to 3.3VSB	Gigabit Ethernet Controller 0 activity indicator, active low.

Serial ATA Interface Signals						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**DFI-RK701**	**Carrier Board**	**Description**
SATA0_RX+	35	I SATA	AC coupled on Module		Connect to SATA0 Conn RX pin	Serial ATA or SAS Channel 0 receive differential pair.
SATA0_RX-	37		AC coupled on Module			
SATA0_TX+	29	O SATA	AC coupled on Module		Connect to SATA0 Conn TX pin	Serial ATA or SAS Channel 0 transmit differential pair.
SATA0_TX-	31		AC coupled on Module			
SATA_ACT#	33	I/O CMOS	3.3V/3.3V			Serial ATA Led. Open collector output pin driven during SATA command activity.

USB Interface Signals						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**DFI-RK701**	**Carrier Board**	**Description**
USB_P0+3:66+	96	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	Universal Serial Bus Port 0 differential pair.
USB_P0-	94		3.3V Suspend/3.3V			
USB_P1+	95	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	Universal Serial Bus Port 1 differential pair.This port may be optionally used as USB client port.
USB_P1-	93		3.3V Suspend/3.3V			
USB_P2+	90	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	Universal Serial Bus Port 2 differential pair.
USB_P2-	88		3.3V Suspend/3.3V			
USB_P3+	89	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	Universal Serial Bus Port 3 differential pair.
USB_P3-	87		3.3V Suspend/3.3V			
USB_P4+	84	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	Universal Serial Bus Port 4 differential pair.
USB_P4-	82		3.3V Suspend/3.3V			
USB_0_1_OC#	86	I CMOS	3.3V Suspend/3.3V	PU 10k to 3.3VSB	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 0 and 1. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_2_3_OC#	85	I CMOS	3.3V Suspend/3.3V	PU 10k to 3.3VSB	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 0 and 1. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_4_5_OC#	80	I CMOS	3.3V Suspend/3.3V	PU 10k to 3.3VSB	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 0 and 1. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_ID	92	I CMOS	3.3V Suspend/3.3V			USB ID pin.Configures the mode of the USB Port 1. If the signal is detected as being 'high active' the BIOS will automatically configure USB Port 1 as USB Client and enable USB Client support. This signal should be driven as OC signal by external circuitry.
USB_CC	91	I CMOS	3.3V Suspend/3.3V			USB Client Connect pin.If USB Port 1 is configured for client mode then an externally connected USB host should set this signal to high-active in order to properly make the connection with the module's internal USB client controller. If the external USB host is disconnected, this signal should be set to low-active in order to inform the USB client controller that the external host has been disconnected. A level shifter/protection circuitry should be implemented on the carrier board for this signal.

SDIO Interface Signals						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**DFI-FS700 Series**	**Carrier Board**	**Description**
SDIO_CD#	43	I/O CMOS	3.3V/3.3V			SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.
SDIO_CLK	42	O CMOS	3.3V/3.3V			SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48 MHz.
SDIO_CMD	45	I/O OD/PP CMOS	3.3V/3.3V			SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.
SDIO_LED	44	O CMOS	3.3V/3.3V			SDIO LED. Used to drive an external LED to indicate when transfers occur on the bus.
SDIO_WP	46	I/O CMOS	3.3V/3.3V			SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.
SDIO_PWR#	47	O CMOS	3.3V/3.3V			SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.
SDIO_DAT0-7	48-55	I/O PP CMOS	3.3V/3.3V			SDIO Data lines. These signals operate in push-pull mode

High Definition Audio Signals/AC'97						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**DFI-RK701**	**Carrier Board**	**Description**
I2S_CLK	61	O CMOS	3.3V/3.3V			I2S Clock outout
I2S_TXFS	59	O CMOS	3.3V/3.3V			I2S TXFS
I2C_TXC	63	O CMOS	3.3V/3.3V			I2C TXC
I2S_TXD	67	O CMOS	3.3V/3.3V			I2S TXD
I2S_RXD	65	I CMOS	3.3V/3.3V			I2 RXD

LVDS Flat Panel Signals						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**DFI-RK701**	**Carrier Board**	**Description**
LVDS_PPEN	111	O CMOS	3.3V/3.3V		Connect to enable control of LVDS panel power circuit	Controls panel power enable.
LVDS_BLEN	112	O CMOS	3.3V/3.3V		Connect to enable control of LVDS panel backlight power circuit.	Controls panel Backlight enable.
LVDS_BLT_CTRL/GP_PWM_OUT0	123	O CMOS	3.3V/3.3V		Connect to brightness control of LVDS panel backlight power circuit.	Primary functionality is to control the panel backlight brightness via pulse width modulation (PWM). When not in use for this primary purpose it can be used as General Purpose PWM Output.
LVDS_A0+	99	O LVDS	LVDS		Connect to LVDS connector	LVDS Channel A differential pairs Ther LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/-. LVDS_A_CK+/-, LVDS_B_CK+/-) shall have 100Ω terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer on-board
LVDS_A0-	101					
LVDS_A1+	103	O LVDS	LVDS		Connect to LVDS connector	
LVDS_A1-	105					
LVDS_A2+	107	O LVDS	LVDS		Connect to LVDS connector	
LVDS_A2-	109					
LVDS_A3+	113	O LVDS	LVDS		Connect to LVDS connector	
LVDS_A3-	115					
LVDS_A_CLK+	119	O LVDS	LVDS		Connect to LVDS connector	LVDS Channel A differential clock
LVDS_A_CLK-	121					
LVDS_B0+	100	O LVDS	LVDS		Connect to LVDS connector	LVDS Channel B differential pairs Ther LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/-. LVDS_A_CK+/-, LVDS_B_CK+/-) shall have 100Ω terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer on-board
LVDS_B0-	102					
LVDS_B1+	104	O LVDS	LVDS		Connect to LVDS connector	
LVDS_B1-	106					
LVDS_B2+	108	O LVDS	LVDS		Connect to LVDS connector	
LVDS_B2-	110					
LVDS_B3+	114	O LVDS	LVDS		Connect to LVDS connector	
LVDS_B3-	112					
LVDS_B_CLK+	120	O LVDS	LVDS		Connect to LVDS connector	LVDS Channel B differential clock
LVDS_B_CLK-	122					
LVDS_DID_CLK/GP_I2C_CLK	127	I/O OD CMOS	3.3V/3.3V	PU 4.7K to 3.3V	Connect to DDC clock of LVDS panel	Primary functionality is DisplayID DDC clock line used for LVDS flat panel detection. If primary functionality is not used it can be as General Purpose I²C bus clock line.
LVDS_DID_DAT/GP_I2C_DAT	125	I/O OD CMOS	3.3V/3.3V	PU 4.7K to 3.3V	Connect to DDC data of LVDS panel	Primary functionality DisplayID DDC data line used for LVDS flat panel detection. If primary functionality is not used it can be as General Purpose I²C bus data line.
LVDS_BLC_CLK	128	I/O OD CMOS	3.3V/3.3V	PU 4.7K to 3.3V		Control clock signal for external SSC clock chip.
LVDS_BLC_DAT	126	I/O OD CMOS	3.3V/3.3V	PU 4.7K to 3.3V		Control data signal for external SSC clock chip.

SDVO Interface Signals						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**DFI-FS700 Series**	**Carrier Board**	**Description**
SDVO_BCLK-	133	O PCIE	SDVO			
SDVO_BCLK+	131					
SDVO_INT-	134	I PCIE	SDVO			
SDVO_INT+	132					
SDVO_GREEN-	139	O PCIE	SDVO			
SDVO_GREEN+	137					
SDVO_BLUE-	145	O PCIE	SDVO			
SDVO_BLUE+	143					
SDVO_RED-	151	O PCIE	SDVO			
SDVO_RED+	149					
SDVO_FLDSTALL-	140	I PCIE	SDVO			
SDVO_FLDSTALL+	138					
SDVO_TVCLKIN-	146	I PCIE	SDVO			
SDVO_TVCLKIN+	144					
SDVO_CTRL_CLK	152	I/O OD CMOS	3.3V/3.3V			
SDVO_CTRL_DAT	150	I/O OD CMOS	3.3V/3.3V			

HDMI Interface Signals						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**DFI-RK701**	**Carrier Board**	**Description**
TMDS_CLK-	133	O TMDS	TMDS		Connect AC Coupling Capacitors 0.1uF to Device	TMDS differential pair clock lines.
TMDS_CLK+	131				Connect AC Coupling Capacitors 0.1uF to Device	
TMDS_LANE0-	145	O TMDS	TMDS		Connect AC Coupling Capacitors 0.1uF to Device	TMDS differential pair lines lane 0.
TMDS_LANE0+	143				Connect AC Coupling Capacitors 0.1uF to Device	
TMDS_LANE1-	139	O TMDS	TMDS		Connect AC Coupling Capacitors 0.1uF to Device	TMDS differential pair lines lane 1.
TMDS_LANE1+	137				Connect AC Coupling Capacitors 0.1uF to Device	
TMDS_LANE2-	151	O TMDS	TMDS		Connect AC Coupling Capacitors 0.1uF to Device	TMDS differential pair lines lane 2.
TMDS_LANE2+	149				Connect AC Coupling Capacitors 0.1uF to Device	
HDMI_CTRL_CLK (SDVO_CTRL_CLK)	152	I/O OD CMOS	3.3V/3.3V	PU 4.7K to 3.3V		DDC based control signal (clock) for HDMI device. Note: Level shifters must be implemented on the carrier board for this signal in order to be compliant with the HDMI Specification.
HDMI_CTRL_DAT (SDVO_CTRL_DAT)	150	I/O OD CMOS	3.3V/3.3V	PU 4.7K to 3.3V		DDC based control signal (data) for HDMI device. Note: Level shifters must be implemented on the carrier board for this signal in order to be compliant with the HDMI Specification
HDMI_HPD#	153	I CMOS	3.3V/3.3V		PD 1M and Connect to device Hot Plug Detect	Hot plug detection signal that serves as an interrupt request.

SPI Interface Signals						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**DFI-RK701**	**Carrier Board**	**Description**
SPI_MOSI	199	O CMOS	3.3V Suspend/3.3V		Connect a series resistor 33Ω to Carrier Board SPI Device SI pin	Master serial output/Slave serial input signal. SPI serial output data from Qseven module to the SPI device.
SPI_MISO	201	I CMOS	3.3V Suspend/3.3V		Connect a series resistor 33Ω to Carrier Board SPI Device SO pin	Master serial input/Slave serial output signal. SPI serial input data from the SPI device to Qseven module.
SPI_SCK	203	O CMOS	3.3V Suspend/3.3V		Connect a series resistor 33Ω to Carrier Board SPI Device SCK pin	SPI clock output.
SPI_CS0#	200	O CMOS	3.3V Suspend/3.3V		Connect a series resistor 33Ω to Carrier Board SPI Device CS# pin	SPI chip select 0 output.
SPI_CS1#	202	O CMOS	3.3V/3.3V			

CAN Bus Interface Signals						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**DFI-RK701**	**Carrier Board**	**Description**
CAN0_TX	129	O CMOS	3.3V/3.3V			CAN (Controller Area Network) TX output for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven module's CAN bus it is necessary to add transceiver hardware to the carrier board.
CAN0_RX	130	I CMOS	3.3V/3.3V			RX input for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven module's CAN bus it is necessary to add transceiver hardware to the carrier board.

Power Control Signals						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**DFI-RK701**	**Carrier Board**	**Description**
PWGIN	26	I CMOS	5V/5V			High active input for the Qseven® module indicates that all power rails located on the carrier board are ready for use.
PWRBTN#	20	I CMOS	3.3V Standby			Power Button: Low active power button input. This signal is triggered on the falling edge.

Power Management Signals						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**DFI-RK701**	**Carrier Board**	**Description**
RSTBTN#	28	I CMOS	3.3V/3.3V			Reset button input. This input may be driven active low by an external circuitry to reset the Qseven module.
BATLOW#	27	I CMOS	3.3V Suspend/3.3V			Battery low input. This signal may be driven active low by external circuitry to signal that the system battery is low or may be used to signal some other external battery management event.
WAKE#	17	I CMOS	3.3V Suspend/3.3V			External system wake event. This may be driven active low by external circuitry to signal an external wake-up event.
SUS_STAT#	19	O CMOS	3.3V Suspend/3.3V			Suspend Status: indicates that the system will be entering a low power state soon.
SUS_S3#	18	O CMOS	3.3V Suspend/3.3V			S3 State: This signal shuts off power to all runtime system components that are not maintained during S3 (Suspend to Ram), S4 or S5 states. The signal SUS_S3# is necessary in order to support the optional S3 cold power state.
SUS_S5#	16	O CMOS	3.3V Suspend/3.3V			S5 State: This signal indicates S4 or S5 (Soft Off) state.
SLP_BTN#	21	I CMOS	3.3V Suspend/3.3V			Sleep button. Low active signal used by the ACPI operating system to transition the system into sleep state or to wake it up again. This signal is triggered on falling edge.
LID_BTN#	22	I CMOS	3.3V Suspend/3.3V			LID button. Low active signal used by the ACPI operating system to detect a LID switch and to bring system into sleep state or to wake it up again. Open/Close state may be software configurable.

Miscellaneous Signals						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**DFI-RK701**	**Carrier Board**	**Description**
WDTRIG#	70	I CMOS	3.3V/3.3V			Watchdog trigger signal. This signal restarts the watchdog timer of the Qseven module on the falling edge of a low active pulse.
WDOUT	72	O CMOS	3.3V/3.3V			Watchdog event indicator. High active output used for signaling a missing watchdog trigger. Will be deasserted by software, system reset or a system power down.
I2C_CLK	66	I/O OD CMOS	3.3V/3.3V	PU 4.7K to 3.3V		Clock line of I²C bus.
I2C_DAT	68	I/O OD CMOS	3.3V/3.3V	PU 4.7K to 3.3V		Data line of I²C bus.
SMB_CLK	60	I/O OD CMOS	3.3V Suspend/3.3V	PU 4.7K to 3.3V		Clock line of System Management Bus.
SMB_DAT	62	I/O OD CMOS	3.3V Suspend/3.3V	PU 4.7K to 3.3V		Data line of System Management Bus.
SMB_ALERT#	64	O CMOS	3.3V/3.3V			System Management Bus Alert input. This signal may be driven low by SMB devices to signal an event on the SM Bus.
SPKR/GP_PWM_OUT2	194	O CMOS	3.3V/3.3V			Primary functionality is output for audio enunciator, the"speaker" in PC AT systems. When not in use for this primary purpose it can be used as General Purpose PWM Output.
BIOS_DISABLE#/BOOT_ALT#	41	I CMOS	3.3V/3.3V	PU 10K to 3.3V		Module BIOS disable input signal. Pull low to disable module's on-board BIOS. Allows off-module BIOS implementations. This signal can also be used to disable standard boot firmware flash device and enable an alternative boot firmware source, for example a boot loader.
RSVD	56,124,	NC				Do not connect

Manufacturing Signals						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**DFI-RK701**	**Carrier Board**	**Description**
MFG_NC0	207	I CMOS	3.3V/3.3V			This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TCK signal for boundary scan purposes during production or as a vendor specific control signal. When used as a vendor specific control signal the multiplexer must be controlled by the MFG_NC4 signal.
MFG_NC1	209	O CMOS	3.3V/3.3V			This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TDO signal for boundary scan purposes during production. May also be used, via a multiplexer, as a UART_TX signal to connect a simple UART for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.
MFG_NC2	208	I CMOS	3.3V/3.3V			This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TDI signal for boundary scan purposes during production. May also be used, via a multiplexer, as a UART_RX signal to connect a simple UART for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.
MFG_NC3	210	I CMOS	3.3V/3.3V			This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TMS signal for boundary scan purposes during production. May also be used, via a multiplexer, as vendor specific BOOT signal for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.
MFG_NC4	204	I CMOS	3.3V/3.3V			This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TRST# signal for boundary scan purposes during production. May also be used as control signal for a multiplexer circuit on the module enabling secondary function for MFG_NC0..3 (JTAG / UART). When MFG_NC4 is high active it is being used for JTAG purposes. When MFG_NC4 is low active it is being used for UART purposes.

Thermal Management Signals						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**DFI-RK701**	**Carrier Board**	**Description**
THRM#	69	I CMOS	3.3V/3.3V			Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling.
THRMTRIP#	71	O CMOS	3.3V/3.3V			Thermal Trip indicates an overheating condition of the processor. If 'THRMTRIP#' goes active the system immediately transitions to the S5 State (Soft Off).

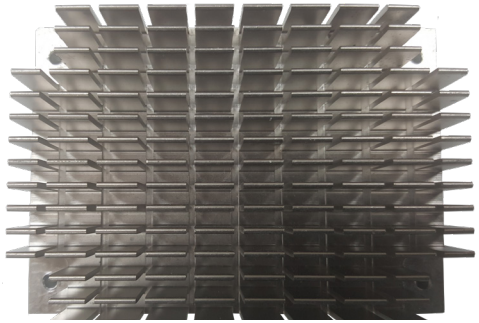
Fan Control Implementation						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**DFI-RK701**	**Carrier Board**	**Description**
FAN_PWMOUT/GP_PWM_OUT1	196	O CMOS	3.3V/3.3V			Primary functionality is fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the Fan's RPM based on the CPU's die temperature. When not in use for this primary purpose it can be used as General Purpose PWM Output.
FAN_TACHOIN/GP_TIMER_IN	195	I CMOS	3.3V/3.3V			Primary functionality is fan tachometer input. When not in use for this primary purpose it can be used as General Purpose Timer Input.

Input Power Pins						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**DFI-RK701**	**Carrier Board**	**Description**
VCC	211-230	Power				Power Supply +5VDC ±5%
VCC_5V_SB	205-206	Power				Standby Power Supply +5VDC ±5%
VCC_RTC	193	Power				3 V backup cell input. VCC_RTC should be connected to a 3V backup cell for RTC operation and storage register non-volatility in the absence of system power. (VCC_RTC = 2.4 - 3.3 V).
GND	1-2, 23-25, 34, 39-40, 57-58, 73-74, 97-98, 117-118, 135-136, 141-142, 147-148, 159-160, 165-166, 183-184, 197-198,	Power Ground				Power Ground.

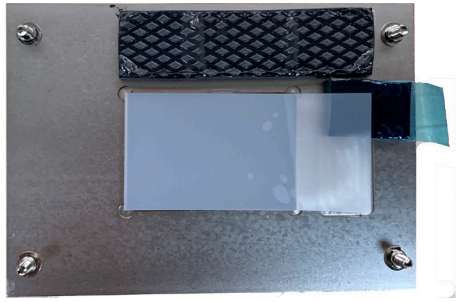
▶ Cooling Option

Heat Sink

The MXM connector is used to interface the RK701 Qseven board to a carrier board. Connect the MXM connector (located on the solder side of the board) to the MXM connector on the carrier board.



Top View of the Heat Sink



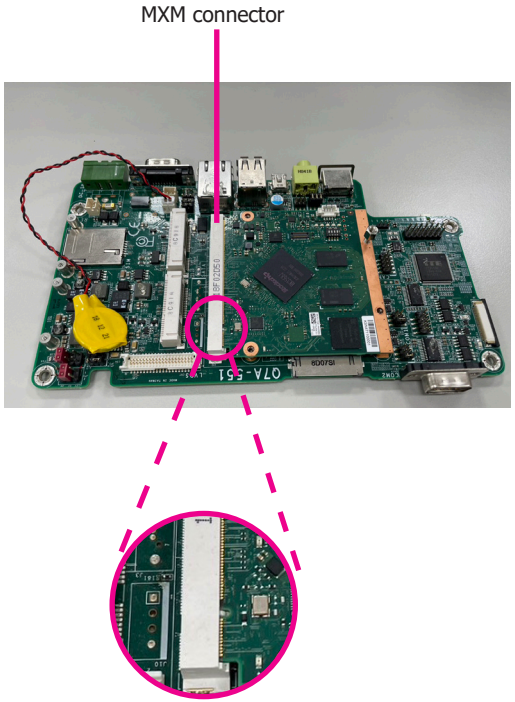
Bottom View of the Heat Sink

Important:
Remove the plastic covering from the thermal pads prior to mounting the heat sink onto board.

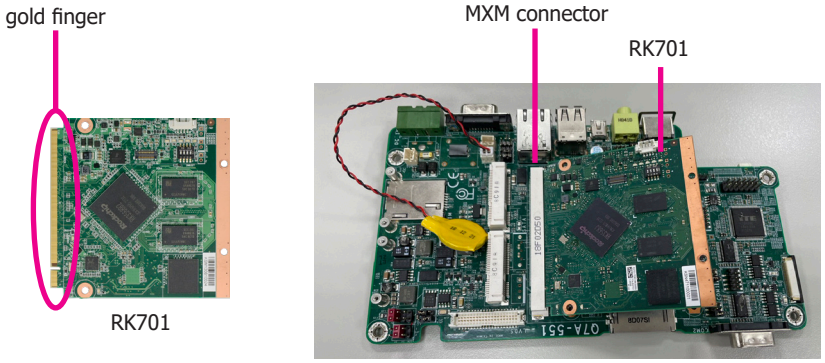
▶ Installing RK701 onto a Carrier Board

Important:
The carrier board used in this section is for reference purpose only and may not resemble your carrier board. These illustrations are mainly to guide you on how to install RK701 onto the carrier board of your choice.

1. Note the key on the MXM connector. The key ensures that RK701 module can be plugged into the connector in one direction only.



2. Grasping the RK701 module by its edges, align it into the MXM connector at an angle of approximately 45 degrees. The RK701 module must be installed into the MXM connector on the carrier board without any gap between the MXM connector and the gold finger.



3. Press the RK701 module down and use the 4 mounting screws provided to secure it to the carrier board in position before you operate the system unit.