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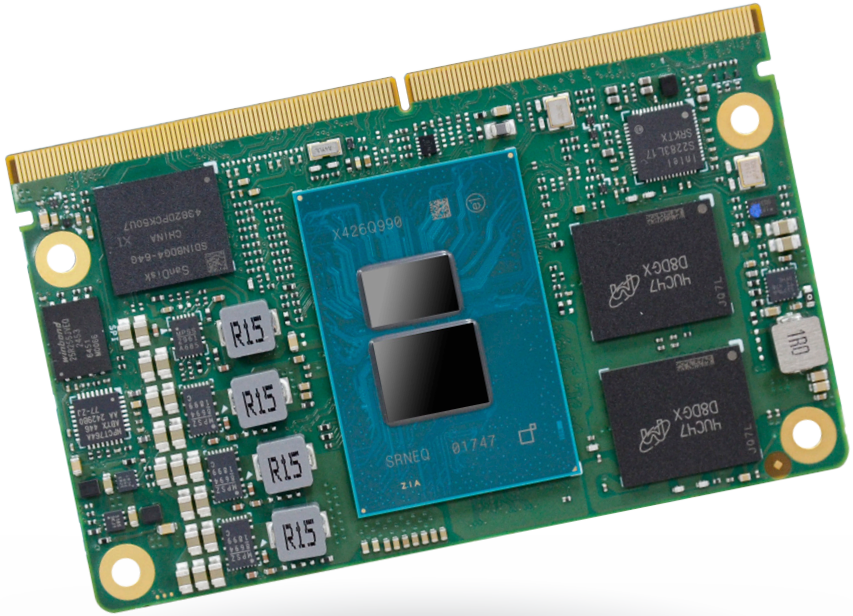


ASL600

SMARC Module
User's Manual

Copyright

Trademarks

SMARC Specification Reference

SMARC Module Specification.
https://sget.org/standards/smarc/

FCC and DOC Statement on Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio TV technician for help.

Notice:

- The changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.
- Shielded interface cables must be used in order to comply with the emission limits.

Table of Contents

About this Manual

This manual can be downloaded from the website.

The manual is subject to change and update without notice, and may be based on editions that do not resemble your actual products. Please visit our website or contact our sales representatives for the latest editions.

Warranty

- Warranty does not cover damages or failures that occur from misuse of the product, inability to use the product, unauthorized replacement or alteration of components and product specifications.
- The warranty is void if the product has been subjected to physical abuse, improper installation, modification, accidents or unauthorized repair of the product.
- Unless otherwise instructed in this user's manual, the user may not, under any circumstances, attempt to perform service, adjustments or repairs on the product, whether in or out of warranty. It must be returned to the purchase point, factory or authorized service agency for all such work.
- We will not be liable for any indirect, special, incidental or consequential damages to the product that has been modified or altered.

Static Electricity Precautions

It is quite easy to inadvertently damage your PC, system board, components or devices even before installing them in your system unit. Static electrical discharge can damage computer components without causing any signs of physical damage. You must take extra care in handling them to ensure against electrostatic build-up.

- To prevent electrostatic build-up, leave the system board in its anti-static bag until you are ready to install it.
- Wear an antistatic wrist strap.
- Do all preparation work on a static-free surface.
- Hold the device only by its edges. Be careful not to touch any of the components, contacts or connections.
- Avoid touching the pins or contacts on all modules and connectors. Hold modules or connectors by their ends.

Important:
Electrostatic discharge (ESD) can damage your processor, disk drive and other components. Perform the upgrade instruction procedures described at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

Safety Measures

- To avoid damage to the system, use the correct AC input voltage range.
- To reduce the risk of electric shock, unplug the power cord before removing the system chassis cover for installation or servicing. After installation or servicing, cover the system chassis before plugging the power cord.

About the Package

The package contains the following items. If any of these items are missing or damaged, please contact your dealer or sales representative for assistance.

The accessories in the package may not come similar to the information listed below. This may differ in accordance with the sales region or models in which it was sold. For more information about the standard package in your region, please contact your dealer or sales representative.

- Heatspreader

Optional Items

The board and accessories in the package may not come similar to the information listed above. This may differ in accordance with the sales region or models in which it was sold. For more information about the standard package in your region, please contact your dealer or sales representative.

- Cooler
- SMX331 Carrier Board Kit

Before Using the System Board

Before using the system board, prepare basic system components.
If you are installing the system board in a new system, you will need at least the following internal components.

- Storage devices such as hard disk drive, etc.

You will also need external system peripherals you intend to use which will normally include at least a keyboard, a mouse and a video display monitor.

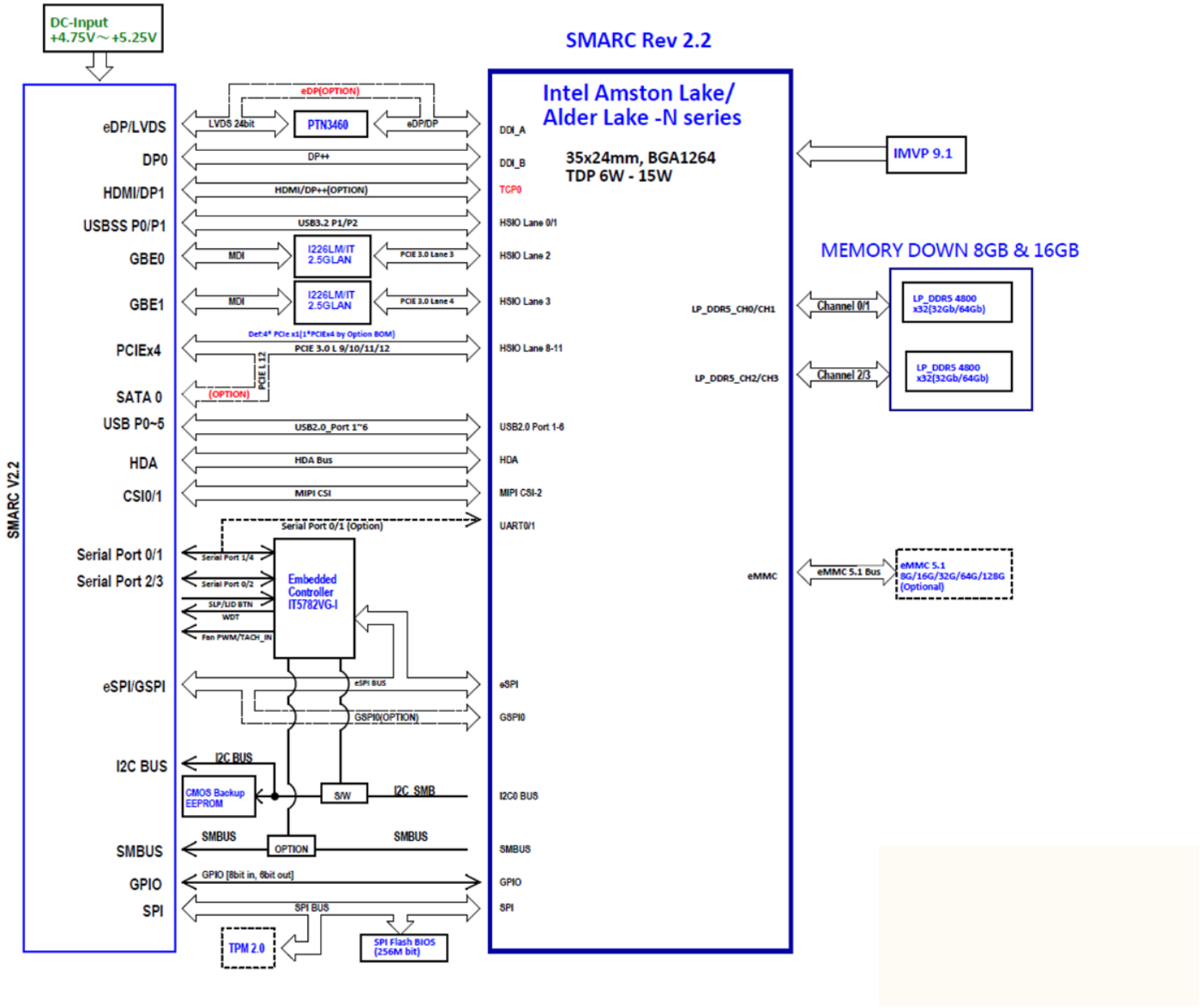
Chapter 1 - Introduction

▶ Specification

SYSTEM	Processor	Intel® Intel® Atom x7000RE series processors (Code Name: Amston Lake) Intel® Atom Processor x7835RE, 8 Cores, 1.3~3.6GHz, 12W Intel® Atom Processor x7433RE, 4 Cores, 1.5~3.4GHz, 9W Intel® Atom Processor x7211RE, 2 Cores, 1.0~3.2GHz, 6W
	Memory	Onboard LPDDR5 4800MHz up to 16GB
	BIOS	AMI SPI 256Mbit
GRAPHICS	Controller	Intel® UHD
	Feature	DX12, Open GL 4.6, Vulkan 1.2 **HW Decode**: 4K60 10b 4:2:0, 4:4:4 HEVC/VP9/SCC, 4K60 10b 4:2:0 AV1 **HW Encode**: 4K60 10b 4:2:0, 4:4:4 HEVC/VP9/SCC
	Display	1 x LVDS/eDP 1 x HDMI/DDI1 1 x DDI **LVDS:** dual channel 1920x1200 @60Hz eDP: 4096x2160 @60Hz **HDMI 1.4b:** 4096x2160 @30Hz **DP:** 4096x2160 @60Hz
	Triple Displays	LVDS/eDP + HDMI + DDI
EXPANSION	Interface	Up to 4x PCIex1 (Gen3) or 1x PCIex4 (available upon request) 2 x I²C 2 x CANBus 1 x SPI, 1 x eSPI/GSPI 2 x 4-wire UART; 2 x 2-wire UART 1 x 4-lane MIPI-CSI; 1 x 2-lane MIPI-CSI
AUDIO	Interface	HD Audio
ETHERNET	Controller	2 x Intel® I226IT (10/100/1000Mbps/2.5Gbps)
I/O	USB	2 x USB 3.2 4 x USB 2.0
	SATA	1 x SATA 3.0 (up to 6Gb/s)
	eMMC	1 x 64GB eMMC 5.1
	GPIO	1 x 14-pin GPIO
WATCHDOG TIMER	Output & Interval	System Reset, Programmable via Software from 1 to 255 Seconds
SECURITY	TPM	TPM 2.0

Power	Type	5Vdc, +/-5%
	Consumption	TBD
OS SUPPORT	Microsoft	Windows: 11/10 IoT Enterprise 64-bit
	Linux	Linux
ENVIRONMENT	Temperature	Operating: -40 to 85°C Storage: -40 to 85°C
	Humidity	Operating: 10 to 90% RH Storage: 10 to 90% RH
	MTBF	TBD
MECHANICAL	Dimensions	SMARC V2.2 82mm (3.22") x 50mm (1.96")
	Compliance	SGET SMARC Specifications 2.2
STANDARDS AND CERTIFICATIONS	Certification	CE, FCC, RoHS

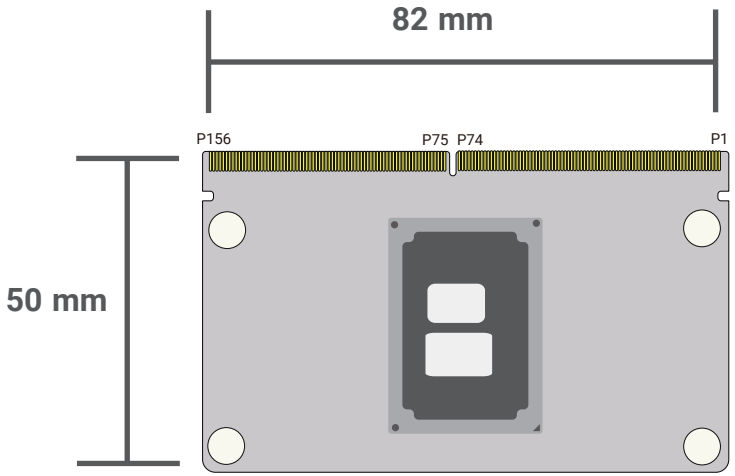
▶ Block Diagram



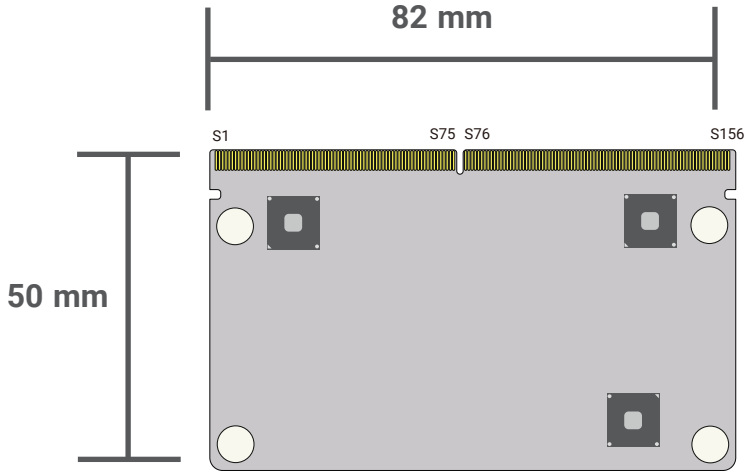
Chapter 2 - Concept

▶ SMARC Module Standards

The figure below shows the dimensions of SMARC modules.
The dimension is 82mm x 50mm.



TOP VIEW



BOTTOM VIEW

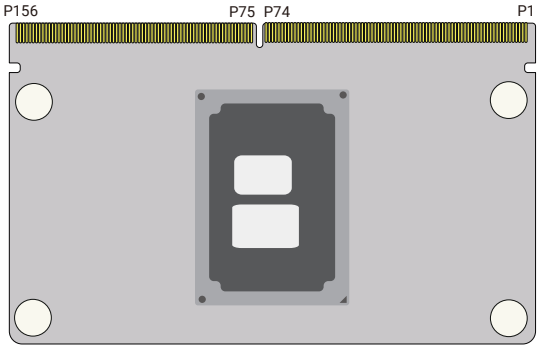
Chapter 2 - Concept

▶ Terminology

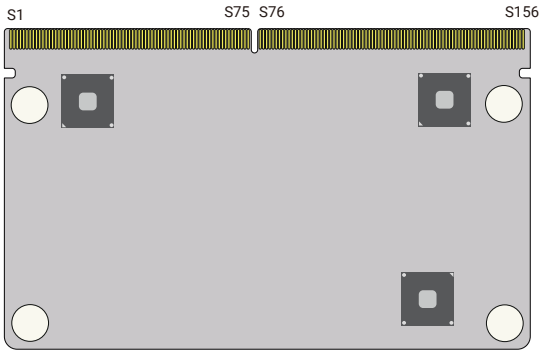
Conventions and Terminology	
ADC	Analog to Digital Converter
CPU	Central Processing Unit
CAN	Controller Area Network
DDC	Digital Video Out
DDI	Digital Display Interface
DP	DisplayPort
DP++	Dual-mode DisplayPort
DSP	Digital Signal Processor
DSI	Display Serial Interface
EEPROM	Electrically Erasable Programmable Read Only Memory
eMMC	Embedded Multi Media Card
ESD	Electrostatic Discharge
GBE	Gigabit Ethernet
GPIO	General Purpose Input / Output
HD Audio	High Definition Audio
HDMI	High Definition Multimedia Interface
I^2C	Inter-Integrated Circuit
I^2S	Inter-Integrated Circuit - Sound
INTx	An interrupt request signal where x stands for interrupts A, B, C, and D
LAN	A local area network (LAN) is a computer network covering a small physical area
LCD	Liquid Crystal Display
LPC	The Low Pin Count (LPC) Interface Specification for legacy I/O has facilitated the industry's transition toward ISA-less systems
LVDS LCD	Low Voltage Differential Signaling: A high speed, low power data transmission standard used for display connections to LCD panels
MIPI	Mobile Industry Processor Interface
NTSC	National Television Standards Committee
PCI	Peripheral Component Interface
PCI-Express	New generation PCI interface with serial interconnection technology
RTC	Real Time Clock
SATA	Serial ATA interface
SMBus	System Management Bus
TMDS	Transition Minimized Differential Signaling
UART	A universal asynchronous receiver/transmitter that translates data between parallel and serial forms.
USB	Universal Serial Bus

Chapter 3 - Hardware Installation

▶ Board Layout



TOP VIEW



BOTTOM VIEW

▶ SMARC Pin Assignments

Pin List of ASL600

The table below is a comprehensive list of all signal pins supported on the SMARC connector as defined for SMARC 2.2 specification.

Pin	Primary (Top) Side	ASL600 Difference	Pin	Primary (Top) Side	ASL600 Difference
P1	SMB_ALERT#		P29	GBE0_MDI0-	
P2	GND		P30	GBE0_MDI0+	
P3	CSI1_CK+		P31	SPI0_CS1#	
P4	CSI1_CK-		P32	GND	
P5	GBE1_SDP		P33	SDIO_WP	NC
P6	GBE0_SDP		P34	SDIO_CMD	NC
P7	CSI1_RX0+		P35	SDIO_CD#	NC
P8	CSI1_RX0-		P36	SDIO_CK	NC
P9	GND		P37	SDIO_PWR_EN	NC
P10	CSI1_RX1+		P38	GND	
P11	CSI1_RX1-		P39	SDIO_D0	NC
P12	GND		P40	SDIO_D1	NC
P13	CSI1_RX2+		P41	SDIO_D2	NC
P14	CSI1_RX2-		P42	SDIO_D3	NC
P15	GND		P43	SPI0_CS0#	
P16	CSI1_RX3+		P44	SPI0_CK	
P17	CSI1_RX3-		P45	SPI0_DIN	
P18	GND		P46	SPI0_DO	
P19	GBE0_MDI3-		P47	GND	
P20	GBE0_MDI3+		P48	SATA_TX+	
P21	GBE0_LINK_MID#	GBE1_LED_1000#	P49	SATA_TX-	
P22	GBE0_LINK_MAX#	GBE1_LED_2500#	P50	GND	
P23	GBE0_MDI2-		P51	SATA_RX+	
P24	GBE0_MDI2+		P52	SATA_RX-	
P25	GBE0_LINK_ACT#		P53	GND	
P26	GBE0_MDI1-		P54	ESPI_CS0#/SPI1_CS0#/QSPI_CS0#	BTB_ESPI_CS0#/GSPI0_CS0#/CB_SPI0_CS0#
P27	GBE0_MDI1+		P55	ESPI_CS1#/SPI1_CS1#/QSPI_CS1#	BTB_ESPI_CS1#/NC/CB_SPI0_CS1#
P28	GBE0_CTREF		P56	ESPI_CK/SPI1_CK/QSPI_CK	BTB_ESPI_CLK/GSPI0_CLK/CB_SPI0_CS0#

Pin	Primary (Top) Side	ASL600 Difference	Pin	Primary (Top) Side	ASL600 Difference
P57	ESPI_IO_1/SPI1_DIN/ QSPI_IO_1	BTB_ESPI_IO_1/GSPI0_ MISO/CB_SPI0_MISO	P85	GND	
P58	ESPI_IO_0/SPI1_DO/ QSPI_IO_0	BTB_ESPI_IO_0/GSPI0_ MOSI/CB_SPI0_MOSI	P86	PCIE_A_RX+	
P59	GND		P87	PCIE_A_RX-	
P60	USB0+		P88	GND	
P61	USB0-		P89	PCIE_A_TX+	
P62	USB0_EN_OC#		P90	PCIE_A_TX-	
P63	USB0_VBUS_DET	NC	P91	GND	
P64	USB0_OTG_ID	NC	P92	HDMI_D2+/DP1_LANE0+	
P65	USB1+		P93	HDMI_D2-/ DP1_LANE0-	
P66	USB1-		P94	GND	
P67	USB1_EN_OC#		P95	HDMI_D1+/DP1_LANE1+	
P68	GND		P96	HDMI_D1-/DP1_LANE1-	
P69	USB2+		P97	GND	
P70	USB2-		P98	HDMI_D0+/DP1_LANE2+	
P71	USB2_EN_OC#		P99	HDMI_D0-/DP1_LANE2-	
P72	RSVD		P100	GND	
P73	RSVD		P101	HDMI_CK+/DP1_LANE3+	
P74	USB3_EN_OC#		P102	HDMI_CK-/DP1_LANE3-	
P75	PCIE_A_RST#		P103	GND	
P76	USB4_EN_OC#		P104	HDMI_HPD/DP1_HPD	
P77	PCIE_B_CKREQ#		P105	HDMI_CTRL_CK/DP1_AUX+	
P78	PCIE_A_CKREQ#		P106	HDMI_CTRL_DAT/ DP1_AUX-	
P79	GND		P107	DP1_AUX_SEL	
P80	PCIE_C_REFCK+		P108	GPIO0/CAM0_PWR#	
P81	PCIE_C_REFCK-		P109	GPIO1/CAM1_PWR#	
P82	GND		P110	GPIO2/CAM0_RST#	
P83	PCIE_A_REFCK+		P111	GPIO3/CAM1_RST#	
P84	PCIE_A_REFCK-		P112	GPIO4/HAD_RST#	

Pin	Primary (Top) Side	ASL600 Difference	Pin	Primary (Top) Side	ASL600 Difference
P113	GPIO5/PWM_OUT		P142	CAN0_TX	
P114	GPIO6/TACHIN		P143	CAN0_RX	
P115	GPIO7		P144	CAN1_TX	
P116	GPIO8		P145	CAN1_RX	
P117	GPIO9		P146	VDD_IN	
P118	GPIO10		P147	VDD_IN	
P119	GPIO11		P148	VDD_IN	
P120	GND		P149	VDD_IN	
P121	I2C_PM_CK		P150	VDD_IN	
P122	I2C_PM_DAT		P151	VDD_IN	
P123	BOOT_SEL0#		P152	VDD_IN	
P124	BOOT_SEL1#		P153	VDD_IN	
P125	BOOT_SEL2#		P154	VDD_IN	
P126	RESET_OUT#		P155	VDD_IN	
P127	RESET_IN#		P156	VDD_IN	
P128	POWER_BTN#				
P129	SER0_TX				
P130	SER0_RX				
P131	SER0_RTS#				
P132	SER0_CTS#				
P133	GND				
P134	SER1_TX				
P135	SER1_RX				
P136	SER2_TX				
P137	SER2_RXSER2_RTS#				
P138	SER2_CTS#				
P139	SER3_TX				
P140	SER3_RX				
P141	GBD				

Pin	Primary (Bottom) Side	ASL600 Difference	Pin	Primary (Bottom) Side	ASL600 Difference
S1	CSI1_TX+/ I2C_CAM1_CK		S30	PCIE_D_TX-/SERDES_0_ TX-	
S2	CSI1_TX-/ I2C_CAM1_DAT		S31	GBE1_LINK_ACT#	
S3	GND		S32	PCIE_D_RX+/ SERDES_0_RX+	
S4	RSVD		S33	PCIE_D_RX-/ SERDES_0_RX-	
S5	CSI0_TX+/ I2C_CAM0_CK		S34	GND	
S6	CAM_MCK		S35	USB4+	
S7	CSI0_TX-/ I2C_CAM0_DAT		S36	USB4-	
S8	CSI0_CK+		S37	USB3_VBUS_DET	NC
S9	CSI0_CK-		S38	AUDIO_MCK	
S10	GND		S39	I2S-LRCK	
S11	CSI1_RX0+		S40	I2S0_SDOUT	
S12	CSI1_RX0-		S41	I2S0_SDIN	
S13	GND		S42	I2S0_CK	
S14	CSI1_RX1+		S43	ESPI_ALERT0#	
S15	CSI1_RX1-		S44	ESPI_ALERT1#	NC
S16	GND		S45	MDIO_CLK	
S17	GBE1_MDI0+		S46	MDIO_DAT	
S18	GBE1_MDI0-		S47	GND	
S19	GBE1_LINK_MID#	GBE2_ LED_1000#	S48	I2C_GP_CK	
S20	GBE1_MDI1+		S49	I2C_GP_DAT	
S21	GBE1_MDI1-		S50	HDA_SYNC/I2S2_LRCK/ SNDW_CLK1	HDA only
S22	GBE1_LINK_MAX#	GBE2_ LED_2500#	S51	HDA_SDO/I2S2_SDOUT/ SNDW_DAT1	HDA only
S23	GBE1_MDI2+		S52	HDA_SDI/I2S2_SDIN/ SNDW_DAT0	HDA only
S24	GBE1_MDI2-		S53	HDA_CK/I2S2_CK/ SNDW_CLK0	HDA only
S25	GND		S54	SATA_ACT#	SATALED#
S26	GBE1_MDI3+		S55	USB5_EN_OC#	
S27	GBE1_MDI3-		S56	ESPI_IO_2/QSPI_IO_2	BTB_ESPI_IO_2/ CB_SPI0_IO2
S28	GBE1_CTREF	NC	S57	ESPI_IO_3/QSPI_IO_3	BTB_ESPI_IO_3/ CB_SPI0_IO3
S29	PCIE_D_TX+/ SERDES_0_TX+		S58	ESPI_RESET#	

Pin	Primary (Bottom) Side	ASL600 Difference	Pin	Primary (Bottom) Side	ASL600 Difference
S59	USB5+		S86	GND	
S60	USB5-		S87	PCIE_B_RX+	
S61	GND		S88	PCIE_B_RX-	
S62	USB3_SSTX+		S89	GND	
S63	USB3_SSTX_-		S90	PCIE_B_TX+	
S64	GND		S91	PCIE_B_TX-	
S65	USB3_SSRX+		S92	GND	
S66	USB3_SSRX-		S93	DP0_LANE0+	
S67	GND		S94	DP0_LANE0-	
S68	USB3+		S95	DP0_AUX_SEL	
S69	USB3-		S96	DP0_LANE1+	
S70	GND		S97	DP0_LANE1-	
S71	USB2_SSTX+		S98	DP0_HPD	
S72	USB2_SSTX-		S99	DP0_LANE2+	
S73	GND		S100	DP0_LANE2-	
S74	USB2_SSRX+		S101	GND	
S75	USB2_SSRX-		S102	DP0_LANE3+	
S76	PCIE_B_RST#		S103	DP0_LANE3-	
S77	PCIE_C_RST#		S104	USB3_OTG_ID	
S78	PCIE_C_RX+/ SERDES_1_RX+		S105	DP0_AUX+	
S79	PCIE_C_RX-/ SERDES_1_RX-		S106	DP0_AUX-	
S80	GND		S107	LCD1_BKLT_EN	
S81	PCIE_C_TX+/ SERDES_1_TX+		S108	LVDS1_CK+/eDP1_AUX+/ DSI1_CLK+	LVDS only
S82	PCIE_C_TX-/ SERDES_1_TX-		S109	LVDS1_CK-/eDP1_AUX-/ DSI1_CLK-	LVDS only
S83	GND		S110	GND	
S84	PCIE_B_REFCK+		S111	LVDS1_0+/eDP1_TX0+/ DSI1_D0+	LVDS only
S85	PCIE_B_REFCK-				

Pin	Primary (Bottom) Side	ASL600 Difference	Pin	Primary (Bottom) Side	ASL600 Difference
S112	LVDS1_0-/eDP1_TX0-/DSI1_D0-	LVDS only	S139	I2C_LCD_CK	
S113	eDP1_HPD/DSI1_TE		S140	I2C_LCD_DAT	
S114	LVDS1_1+/eDP1_TX1+/DSI1_D1+	LVDS only	S141	LCD0_BKLT_PWM	
S115	LVDS1_1-/eDP1_TX1-/DSI1_D1-	LVDS only	S142	GPIO12	
S116	LCD1_VDD_EN		S143	GND	
S117	LVDS1_2+/eDP1_TX2+/DSI1_D2+	LVDS only	S144	eDP0_HPD/DSI0_TE	
S118	LVDS1_2-/eDP1_TX2-/DSI1_D2-	LVDS only	S145	WDT_TIME_OUT#	
S119	GND		S146	PCIE_WAKE#	
S120	LVDS1_3+/eDP1_TX3+/DSI1_D3+	LVDS only	S147	VDD_RTC	
S121	LVDS1_3-/eDP1_TX3-/DSI1_D3-	LVDS only	S148	LID#	
S122	LCD1_BKLT_PWM		S149	SLEEP#	
S123	GPIO13		S150	VIN_PWR_BAD3	
S124	GND		S151	CHARGING#	NC
S125	LVDS0_0+/eDP0_TX0+/DSI0_D0+		S152	CHARGER_PRSNT#	NC
S126	LVDS0_0-/eDP0_TX0-/DSI0_D0-		S153	CARRIER_STBY#	
S127	LCD0_BKLT_PWM		S154	CARRIER_PWR_ON	
S128	LVDS0_1+/eDP0_TX1+/DSI0_D1+		S155	FORCE_RECOV#	
S129	LVDS0_1-/eDP0_TX1-/DSI0_D1-		S156	BATLOW#	
S130	GND		S157	TEST#	
S131	LVDS0_2+/eDP0_TX2+/DSI0_D2+		S158	GND	
S132	LVDS0_2-/eDP0_TX2-/DSI0_D2-				
S133	LCD0_VDD_EN				
S134	LVDS0_CK+/eDP0_AUX+/DSI0_CLK+				
S135	LVDS0_CK-/eDP0_AUX-/DSI0_CLK-				
S136	GND				
S137	LVDS0_3+/eDP0_TX3+/DSI0_D3+				
S138	LVDS0_3-/eDP0_TX3-/DSI0_D3-				

▶ SMARC Connector Signal Description

Pin Types
I : Input to the Module
O : Output from the Module
I/O : Bi-directional input / output signal
OD : Open drain output
RSVD : pins are reserved for future use and should be no connect. Do not tie the RSVD pins together.

PCI Express Lanes Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	ASL600 PU/PD	SMARC Module Specification R2.1 Description	SMARC Carrier Design Guide R2.1 Description
PCIE_A_TX+	P89	O PCIE	AC coupled on Module	AC Coupling capacitor	PCIe Differential Transmit Pair Channel A.	PCIe channel A. Transmit Output differential pair.
PCIE_A_TX-	P90			AC Coupling capacitor		
PCIE_A_RX+	P86	I PCIE			PCIe Differential Receive Pair Channel A.	PCIe channel A. Receive Input differential pair.
PCIE_A_RX-	P87					
PCIE_A_REFCK+	P83	O PCIE	PCIE		PCIe Reference Clock for PCIe lanes.	Connect 0Ω in series to Device - PCIE device REFCLK+, REFCLK-. Slot - PCIE Conn pin A13 REFCLK+, A14 REFCLK-. *Connect to PCIE Clock Buffer input to provide PCIE clocks output for more than one PCIE devices or slots.
PCIE_A_REFCK-	P84					
PCIE_A_RST#	P75	O CMOS		3.3V	Reset output from Module to Carrier Board.	Connect to reset pin of devices except PCI slots or devices.
PCIE_A_CKREQ#	P78	IO OD CMOS		3.3V	PCIe Port A clock request.	Can be used for power saving mode on PCIe - Pulled up or terminated on Module.
PCIE_B_TX+	S90	O PCIE	AC coupled on Module	AC Coupling capacitor	PCIe Differential Transmit Pair Channel B.	PCIe channel B. Transmit Output differential pair.
PCIE_B_TX-	S91			AC Coupling capacitor		
PCIE_B_RX+	S87	I PCIE			PCIe Differential Receive Pair Channel B.	PCIe channel B. Receive Input differential pair.
PCIE_B_RX-	S88					
PCIE_B_REFCK+	S84	O PCIE	PCIE		PCIe Reference Clock for PCIe lanes.	Connect 0Ω in series to Device - PCIE device REFCLK+, REFCLK-. Slot - PCIE Conn pin A13 REFCLK+, A14 REFCLK-. *Connect to PCIE Clock Buffer input to provide PCIE clocks output for more than one PCIE devices or slots.
PCIE_B_REFCK-	S85					
PCIE_B_RST#	S76	O CMOS		3.3V	Reset output from Module to Carrier Board.	Connect to reset pin of devices except PCI slots or devices.
PCIE_B_CKREQ#	P77	IO OD CMOS		3.3V	PCIe Port B clock request.	Can be used for power saving mode on PCIe - Pulled up or terminated on Module.
PCIE_C_TX+	S81	O PCIE	AC coupled on Module	AC Coupling capacitor	PCIe Differential Transmit Pair Channel C.	PCIe channel C. Transmit Output differential pair.
PCIE_C_TX-	S82			AC Coupling capacitor		
PCIE_C_RX+	S78	I PCIE			PCIe Differential Receive Pair Channel C.	PCIe channel C. Receive Input differential pair.
PCIE_C_RX-	S79					
PCIE_C_REFCK+	P80	O PCIE	PCIE		PCIe Reference Clock for PCIe lanes.	Connect 0Ω in series to Device - PCIE device REFCLK+, REFCLK-. Slot - PCIE Conn pin A13 REFCLK+, A14 REFCLK-. *Connect to PCIE Clock Buffer input to provide PCIE clocks output for more than one PCIE devices or slots.
PCIE_C_REFCK-	P81					
PCIE_C_RST#	S77	O CMOS		3.3V	Reset output from Module to Carrier Board.	Connect to reset pin of devices except PCI slots or devices.
PCIE_D_TX+	S29	O PCIE	AC coupled on Module	AC Coupling capacitor	PCIe Differential Transmit Pair Channel D.	PCIe channel D. Transmit Output differential pair.
PCIE_D_TX-	S30			AC Coupling capacitor		
PCIE_D_RX+	S32	I PCIE			PCIe Differential Receive Pair Channel D.	PCIe channel D. Receive Input differential pair.
PCIE_D_RX-	S33					
PCIE_WAKE#	S146	IO OD CMOS		3.3V	PCIe wake up interrupt to host - common to PCIe links A, B, C, D - pulled up or terminated on Module This signal has 10K Ω pull up to 3.3V_DUAL on the module.	Device - Connect to WAKE# pin of PCIE device. Slot - Connect to WAKE# pin B11 of PCIE slot. Express Card - Connect to WAKE# pin 11 of Express Card socket

▶ SMARC Connector Signal Description

SATA Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	ASL600 PU/PD	Module Base Specification R2.2 Description	SMARC Carrier Design Guide R2.2 Description
SATA0_TX+	P48	O SATA	AC coupled on Module	AC Coupling capacitor	Differential SATA 0 transmit data Pair 0402 series coupling caps shall be on Module 10 nF capacitor	Serial ATA channel 0 Transmit output differential pair.
SATA0_TX-	P49	O SATA	AC coupled on Module	AC Coupling capacitor		
SATA0_RX+	P51	I SATA	AC coupled on Module	AC Coupling capacitor	Differential SATA 0 transmit data Pair 0402 series coupling caps shall be on Module 10 nF capacitor	Serial ATA channel 0 Receive input differential pair.
SATA0_RX-	P52	I SATA	AC coupled on Module	AC Coupling capacitor		
SATA_ACT#	S54	I/O CMOS	3.3V / 3.3V	Single buffer	Serial ATA (activity indicator), active low.	Serial ATA activity LED. Open collector output pin driven during SATA command activity.

Gigabit Ethernet Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	ASL600 PU/PD	Module Base Specification R2.2 Description	SMARC Carrier Design Guide R2.2 Description
GBE0_MDI0+	P30	I/O GBE MDI	3.3V max Suspend		Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. Some pairs are unused in some modes, per the following: 1000BASE-T 100BASE-TX 10BASE-T MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	Media Dependent Interface (MDI) differential pair 0.
GBE0_MDI0-	P29		3.3V max Suspend			
GBE0_MDI1+	P27		3.3V max Suspend			Media Dependent Interface (MDI) differential pair 1.
GBE0_MDI1-	P26		3.3V max Suspend			
GBE0_MDI2+	P24		3.3V max Suspend			Media Dependent Interface (MDI) differential pair 2. Only used for 1000Mbit/sec Gigabit Ethernet mode.
GBE0_MDI2-	P23		3.3V max Suspend			
GBE0_MDI3+	P20		3.3V max Suspend			Media Dependent Interface (MDI) differential pair 3. Only used for 1000Mbit/sec Gigabit Ethernet mode.
GBE0_MDI3-	P19		3.3V max Suspend			
GBE0_ACT#	P25	OD CMOS	3.3V Suspend/3.3V		Gigabit Ethernet Controller 0 activity indicator, active low.	Ethernet controller 0 activity indicator, active low.
GBE0_LINK_MID#	P21	OD CMOS	3.3V Suspend/3.3V	LED for link speed with 1Gbps.	A speed lower than the maximum speed supported, active low.	A speed lower than the maximum speed supported, active low.
GBE0_LINK_MAX#	P22	OD CMOS	3.3V Suspend/3.3V	LED for link speed with 2.5Gbps	At the maximum link speed supported by the controller, active low.	At the maximum link speed supported by the controller, active low.
GBE0_CTREF	P28	Analog	GND min, 3.3V max	NC	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be limited to 250 mA or less.	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap.
GBE0_SDP	P6	I/O CMOS	3.3V Suspend/3.3V		Gigabit Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1pps signal.	Reserved measuring points

▶ SMARC Connector Signal Description

Gigabit Ethernet Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	ASL600 PU/PD	Module Base Specification R2.2 Description	SMARC Carrier Design Guide R2.2 Description
GBE1_MDI0+	S17	I/O GBE MDI	3.3V max Suspend		Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. Some pairs are unused in some modes, per the following: 1000BASE-T 100BASE-TX 10BASE-T MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	Media Dependent Interface (MDI) differential pair 0.
GBE1_MDI0-	S18		3.3V max Suspend			
GBE1_MDI1+	S20		3.3V max Suspend			Media Dependent Interface (MDI) differential pair 1.
GBE1_MDI1-	S21		3.3V max Suspend			
GBE1_MDI2+	S23		3.3V max Suspend			Media Dependent Interface (MDI) differential pair 2. Only used for 1000Mbit/sec Gigabit Ethernet mode.
GBE1_MDI2-	S24		3.3V max Suspend			
GBE1_MDI3+	S26		3.3V max Suspend			Media Dependent Interface (MDI) differential pair 3. Only used for 1000Mbit/sec Gigabit Ethernet mode.
GBE1_MDI3-	S27		3.3V max Suspend			
GBE1_ACT#	S31	OD CMOS	3.3V Suspend/3.3V		Gigabit Ethernet Controller 0 activity indicator, active low.	Ethernet controller 0 activity indicator, active low.
GBE1_LINK_MID#	S19	OD CMOS	3.3V Suspend/3.3V	LED for link speed with 1Gbps.	A speed lower than the maximum speed supported, active low.	A speed lower than the maximum speed supported, active low.
GBE1_LINK_MAX#	S22	OD CMOS	3.3V Suspend/3.3V	LED for link speed with 2.5Gbps	At the maximum link speed supported by the controller, active low.	At the maximum link speed supported by the controller, active low.
GBE1_CTREF	S28	Analog	GND min, 3.3V max	NC	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be limited to 250 mA or less.	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap.
GBE1_SDP	P5	I/O CMOS	3.3V Suspend/3.3V		Gigabit Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1pps signal.	Reserved measuring points

HAD/I2S2 Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	ASL600 PU/PD	Module Base Specification R2.2 Description	SMARC Carrier Design Guide R2.2 Description
HDA_RST#/ GPIO4	P112	O CMOS Runtime	1.5V / 1.8V		High Definition Audio Reset Output to Codec, low active.	HDA - Connect 0 Ω in series to HDA CODEC pin RESET#
HDA_SYNC/ I2S2_LRCK	S50	I/O CMOS Runtime	HDA:1.5V / 1.8V I2S2: 1.8V		High Definition Audio Sample synchronization clock to codec	HDA - Connect 0 Ω in series to HDA CODEC pin SYNC
HDA_SDO/ I2S2_SODOUT	S51	O CMOS Runtime	1.5V / 1.8V		High Definition Audio data out to codec	HDA - Connect 0 Ω in series and PD 10KΩ(NL) to HDA CODEC pin SDATA_IN
HDA_SDI/ I2S2/SDIN	S52	I/O CMOS Runtime	1.5V / 1.8V		High Definition Audio data in from codec	HDA - Connect 33-47 Ω in series and PD 10KΩ(NL) to HDA CODEC pin SDATA_OUT
HDA_CK/ I2S2_CK	S53	I/O CMOS Runtime	1.5V / 1.8V		High Definition Audio clock to codec	HDA - Connect 0 Ω in series to HDA CODEC pin BIT_CLK

Note : ASL600 supports HDA only.

▶ SMARC Connector Signal Description

USB Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	ASL600 PU/PD	Module Base Specification R2.2 Description	SMARC Carrier Design Guide R2.2 Description
USB0+	P60	I/O USB	USB Standby		USB differential pairs, channel 0.	USB Port 0, data + or D+
USB0-	P61					USB Port 0, data - or D-
USB1+	P65	I/O USB	USB Standby		USB differential pairs, channel 1.	USB Port 1, data + or D+
USB1-	P66					USB Port 1, data - or D-
USB2+	P69	I/O USB	USB Standby		USB differential pairs, channel 2.	USB Port 2, data + or D+
USB2-	P70					USB Port 2, data - or D-
USB3+	S68	I/O USB	USB Standby		USB differential pairs, channel 3.	USB Port 3, data + or D+
USB3-	S69					USB Port 3, data - or D-
USB4+	S35	I/O USB	USB Standby		USB differential pairs, channel 4.	USB Port 4, data + or D+
USB4-	S36					USB Port 4, data - or D-
USB5+	S59	I/O USB	USB Standby		USB differential pairs, channel 5.	USB Port 5, data + or D+
USB5-	S60					USB Port 5, data - or D-

▶ SMARC Connector Signal Description

USB0_EN_OC#	P62	I/O OD CMOS	3.3V Standby	PU 10KΩ to 3.3V Suspend	USB over-current sense, USB channels 0. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	USB over-current sense, USB ports 0. Do not pull up these lines to 3.3V on the Carrier Board – this shall be done on the Module.
USB1_EN_OC#	P71	I/O OD CMOS	3.3V Standby	PU 10KΩ to 3.3V Suspend	USB over-current sense, USB channels 1. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	USB over-current sense, USB ports 1. Do not pull up these lines to 3.3V on the Carrier Board – this shall be done on the Module.
USB2_EN_OC#	B38	I/O OD CMOS	3.3V Standby	PU 10KΩ to 3.3V Suspend	USB over-current sense, USB channels 2. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	USB over-current sense, USB ports 2. Do not pull up these lines to 3.3V on the Carrier Board – this shall be done on the Module.
USB3_EN_OC#	P74	I/O OD CMOS	3.3V Standby	PU 10KΩ to 3.3V Suspend	USB over-current sense, USB channels 3. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	USB over-current sense, USB ports 3. Do not pull up these lines to 3.3V on the Carrier Board – this shall be done on the Module.
USB4_EN_OC#	P76	I/O OD CMOS	3.3V Standby	PU 10KΩ to 3.3V Suspend	USB over-current sense, USB channels 4. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	USB over-current sense, USB ports 4. Do not pull up these lines to 3.3V on the Carrier Board – this shall be done on the Module.
USB5_EN_OC#	S55	I/O OD CMOS	3.3V Standby	PU 10KΩ to 3.3V Suspend	USB over-current sense, USB channels 5. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	USB over-current sense, USB ports 5. Do not pull up these lines to 3.3V on the Carrier Board – this shall be done on the Module.
USB0_OTG_ID	P64	I CMOS	3.3V Standby		USB OTG ID input, active high. Configures the mode of the USB Port 0. The resistance of this pin measured to ground is used to determine whether USB Port 3 is going to be used as USB Client to enable/ disable USB Client support. Please check the USB-OTG Reference of your chip manufacturer for further details.	Carrier board not support OTG function.
USB3_OTG_ID	S104	I CMOS	3.3V Standby		USB OTG ID input, active high. Configures the mode of the USB Port 3. The resistance of this pin measured to ground is used to determine whether USB Port 3 is going to be used as USB Client to enable/ disable USB Client support. Please check the USB-OTG Reference of your chip manufacturer for further details.	Carrier board not support OTG function.
USB0_VBUS_DET	P63	I USB VBUS	5V Standby		USB host power detection, when this port is used as a device	Carrier board not support OTG function.
USB3_VBUS_DET	S37	I USB VBUS	5V Standby		USB host power detection, when this port is used as a device	Carrier board not support OTG function.

▶ SMARC Connector Signal Description

USB2_SSRX+	S74	I USB SS	USB Standby		Receive signal differential pairs for SuperSpeed USB data Coupling caps for RX pairs are off-Module	USB Port 2, SuperSpeed RX +
USB2_SSRX-	S75					USB Port 2, SuperSpeed RX -
USB2_SSTX+	S71	O USB SS	USB Standby	AC Coupling capacitor	Transmit signal differential pairs for SuperSpeed USB data Coupling caps for TX pairs are on-Module	USB Port 2, SuperSpeed TX +
USB2_SSTX-	S72			AC Coupling capacitor		USB Port 2, SuperSpeed TX -
USB3_SSRX+	S65	I USB SS	USB Standby		Receive signal differential pairs for SuperSpeed USB data Coupling caps for RX pairs are off-Module	USB Port 3, SuperSpeed RX +
USB3_SSRX-	S66					USB Port 3, SuperSpeed RX -
USB3_SSTX+	S62	O USB SS	USB Standby	AC Coupling capacitor	Transmit signal differential pairs for SuperSpeed USB data Coupling caps for TX pairs are on-Module	USB Port 3, SuperSpeed TX +
USB3_SSTX-	S63			AC Coupling capacitor		USB Port 3, SuperSpeed TX -

▶ SMARC Connector Signal Description

LVDS Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	ASL600 PU/PD	Module Base Specification R2.2 Description	SMARC Carrier Design Guide R2.2 Description
LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	S125	O LVDS	LVDS EDP: AC coupled off Module Runtime		LVDS Channel A differential pairs eDP: eDP differential pairs	LVDS channel A differential signal pair 0 eDP lane 0, TX± differential signal pair
LVDS0_0- / eDP0_TX0- / DSI0_D0-	S126					
LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	S128	O LVDS	LVDS EDP: AC coupled off Module Runtime			LVDS channel A differential signal pair 1 eDP lane 1, TX± differential signal pair
LVDS0_1- / eDP0_TX1- / DSI0_D1-	S129					
LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	S131	O LVDS	LVDS EDP: AC coupled off Module Runtime			LVDS channel A differential signal pair 2 eDP lane 2, TX± differential signal pair
LVDS0_2- / eDP0_TX2- / DSI0_D2-	S132					
LVDS0_3+ / eDP0_TX3+ / DSI0_D2+	S137	O LVDS	LVDS EDP: AC coupled off Module Runtime			LVDS channel A differential signal pair 3 eDP lane 3, TX± differential signal pair
LVDS0_3- / eDP0_TX3- / DSI0_D2-	S138					
LVDS0_CK+/eDP0_AUX+/ DSI0_CLK+	S134	O LVDS	LVDS EDP: AC coupled off Module Runtime		LVDS Channel A differential clock eDP: eDP differential pairs	LVDS channel A differential clock pair
LVDS0_CK-/eDP0_AUX-/ DSI0_CLK-	S135					
LCD0_VDD_EN	S133	O CMOS	1.8V Runtime		LVDS panel / eDP power enable Active high	LVDS flat panel power enable. eDP power enable
LCD0_BKLT_EN	S127	O CMOS	1.8V Runtime		LVDS panel / eDP backlight enable Active high	LVDS flat panel backlight enable high active signal eDP backlight enable
LCD0_BKLT_PWM	S141	O CMOS	1.8V Runtime		LVDS panel / eDP backlight brightness control	LVDS flat panel backlight brightness control EDP backlight brightness control
LVDS_I2C_CK	S139	I/O OD CMOS	1.8V Runtime	PU 2.2KΩ to 3.3V	I2C clock – to read LCD display EDID EEPROMs	DDC I2C clock signal used for flat panel detection and control. eDP auxiliary lane +
LVDS_I2C_DAT	S140	I/O OD CMOS	1.8V Runtime	PU 2.2KΩ to 3.3V	I2C data – to read LCD display EDID EEPROMs Be aware of possible EDID PROM address conflicts if multiple displays are implemented	DDC I2C data signal used for flat panel detection and control. eDP auxiliary lane -
eDP0_HPD/DSI0_TE	S144	I CMOS	1.8V Runtime	eDP0: PD 100KΩ to GND	eDP0_HPD:Detection of Hot Plug / Unplug and notification of the link layer Module must tolerate high level in stand-by mode	eDP0_HPD: Detection of Hot Plug / Unplug and notification of the link layer

▶ SMARC Connector Signal Description

LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	S111	O LVDS	LVDS EDP: AC coupled off Module Runtime		LVDS Channel B differential pairs eDP: eDP differential pairs	LVDS channel B differential signal pair 0 eDP lane 0, TX± differential signal pair
LVDS1_0- / eDP1_TX0- / DSI1_D0-	S112					
LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	S114	O LVDS	LVDS EDP: AC coupled off Module Runtime			LVDS channel B differential signal pair 1 eDP lane 1, TX± differential signal pair
LVDS1_1- / eDP1_TX1- / DSI1_D1-	S115					
LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	S117	O LVDS	LVDS EDP: AC coupled off Module Runtime			LVDS channel B differential signal pair 2 eDP lane 2, TX± differential signal pair
LVDS1_2- / eDP1_TX2- / DSI1_D2-	S118					
LVDS1_3+ / eDP1_TX3+ / DSI1_D2+	S120	O LVDS	LVDS EDP: AC coupled off Module Runtime			LVDS channel B differential signal pair 3 eDP lane 3, TX± differential signal pair
LVDS1_3- / eDP1_TX3- / DSI1_D2-	S121					
LVDS0_CK+/eDP0_AUX+/ DSI0_CLK+	S108	O LVDS	LVDS EDP: AC coupled off Module Runtime		LVDS Channel B differential clock eDP: eDP differential pairs	LVDS channel B differential clock pair
LVDS0_CK-/eDP0_AUX-/ DSI0_CLK-	S109					
LCD1_VDD_EN	S116	O CMOS	1.8V Runtime		LVDS panel / eDP power enable Active high	LVDS flat panel power enable. eDP power enable
LCD1_BKLT_EN	S107	O CMOS	1.8V Runtime		LVDS panel / eDP backlight enable Active high	LVDS flat panel backlight enable high active signal eDP backlight enable
LCD1_BKLT_PWM	S112	O CMOS	1.8V Runtime		LVDS panel / eDP backlight brightness control	LVDS flat panel backlight brightness control EDP backlight brightness control
eDP1_HPD/DSI1_TE	S113	I CMOS	1.8V Runtime	eDP1: PD 100KΩ to GND	eDP1_HPD:Detection of Hot Plug / Unplug and notification of the link layer Module must tolerate high level in stand-by mode	eDP1_HPD: Detection of Hot Plug / Unplug and notification of the link layer

Note : ASL600 EDP supports channel A only.

▶ SMARC Connector Signal Description

DDI Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	ASL600 PU/PD	Module Base Specification R2.2 Description	SMARC Carrier Design Guide R2.2 Description
DP0_LANE0+	S93	O DP	AC coupled off Module Runtime		DDI for Display Port: DP0_LANE 0 differential pairs	DP0_LANE0+ for DP
DP0_LANE0-	S94					DP0_LANE0- for DP
DP0_LANE1+	S96	O DP	AC coupled off Module Runtime		DDI for Display Port: DP0_LANE 1 differential pairs	DP0_LANE1+ for DP
DP0_LANE1-	S97					DP0_LANE1- for DP
DP0_LANE2+	S99	O DP	AC coupled off Module Runtime		DDI for Display Port: DP0_LANE 2 differential pairs	DP0_LANE2+ for DP
DP0_LANE2-	S100					DP0_LANE2- for DP
DP0_LANE3+	S102	O DP	AC coupled off Module Runtime		DDI for Display Port: DP0_LANE 3 differential pairs	DP0_LANE3+ for DP
DP0_LANE3-	S103					DP0_LANE3- for DP
DP0_AUX+	S105	I/O DP	3.3V AC coupled on Module Runtime	PD 100KΩ to GND (S/W IC between Rpu/PCH)	AC coupled on Module If DP0_AUX_SEL=0 (DP mode): AC coupled on module, 100k PD. If DP0_AUX_SEL=1 (HDMI mode): DC coupled, CMOS, 100k PU. In case of HDMI over DP++ implementation, stronger pull-up is demanded to the Carrier Board.	DP0_AUX+ for DP
DP0_AUX-	S106	I/O DP	3.3V AC coupled on Module Runtime	PU 100KΩ to 3.3V (S/W IC between Rpu/PCH)	AC coupled on Module If DP0_AUX_SEL=0 (DP mode): AC coupled on module, 100k PU. If DP0_AUX_SEL=1 (HDMI mode): DC coupled, CMOS, 100k PU. In case of HDMI over DP++ implementation, stronger pull-up is demanded to the Carrier Board	DP0_AUX- for DP
DP0_HPD	S98	I CMOS	1.8V Runtime	PD 100KΩ to GND	DDI for Display Port: DP0_HPD (Detection of Hot Plug / Unplug and notification of the link layer) DDI for HDMI/DVI: HDMI0_HPD (HDMI/DVI Hot-Plug Detect)	The carrier shall include a blocking FET on DP0_HPD to prevent back-drive current from damaging the module. Device - Connect to DP device Hot Plug Detect DP Connector - Connect to DP Conn pin 18 Hot Plug Detect
DP0_AUX_SEL	S95	I CMOS	1.8V Runtime	PD 1MΩ to GND	Selects the function of DDI0_CTRLCLK_AUX+ and DDI0_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is unconnected the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals.	Pulled to GND on Carrier for DP operation in Dual Mode (DP++) implementations Module must tolerate high level in stand-by mode. Should be connected to pin 13 of the DisplayPort connector to enable a dual-mode DisplayPort interface.

▶ SMARC Connector Signal Description

DDI Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	ASL600 PU/PD	Module Base Specification R2.2 Description	SMARC Carrier Design Guide R2.2 Description
DP1_LANE0+/ HDMI_D2+	P92	O DP O TMDS HDMI	AC coupled off Module(DP) Runtime		DDI for Display Port: DP0_LANE 0 differential pairs	DP1_LANE0+ for DP
DP1_LANE0-/ HDMI_D2-	P93					DP1_LANE0- for DP
DP1_LANE1+/ HDMI_D1+	P95	O DP O TMDS HDMI	AC coupled off Module(DP) Runtime		DDI for Display Port: DP0_LANE 1 differential pairs	DP1_LANE1+ for DP
DP1_LANE1-/ HDMI_D1-	P96					DP1_LANE1- for DP
DP1_LANE2+/ HDMI_D0+	P98	O DP O TMDS HDMI	AC coupled off Module(DP) Runtime		DDI for Display Port: DP0_LANE 2 differential pairs	DP1_LANE2+ for DP
DP1_LANE2 -/ HDMI_D0-	P99					DP1_LANE2- for DP
DP1_LANE3+/ HDMI_CK+	P101	O DP O TMDS HDMI	AC coupled off Module(DP) Runtime		DDI for Display Port: DP0_LANE 3 differential pairs	DP1_LANE3+ for DP
DP1_LANE3-/ HDMI_CK-	P102					DP1_LANE3- for DP
DP1_AUX+/ HDMI_CTRL_CK	P105	I/O DP I/O OD CMOS HDMI	DP: 3.3V AC coupled on Module Runtime HDMI: 1.8V Runtime	PD 100KΩ to GND **(S/W IC between Rpu/PCH)**	AC coupled on Module If DP1_AUX_SEL=0 (DP mode): AC coupled on module, 100k PD. If DP0_AUX_SEL=1 (HDMI mode): DC coupled, CMOS, 100k PU. In case of HDMI over DP++ implementation, stronger pull-up is demanded to the Carrier Board.	DP1_AUX+ for DP Pull-ups to 1.8V on each of these lines is required on the Carrier. The pull-ups may be part of an integrated HDMI ESD protection and control-line level shift device. If discrete Carrier pull-ups are used, they should be 10K or 100K pull-up to 1.8V. For HDMI Connector, connect to HDMI Conn pin 15 HDMI_CTRL_CK, pin 16 HDMI_CTRL_DAT and ESD protection
DP1_AUX-/ HDMI_CTRL_DAT	P106	I/O DP I/O OD CMOS HDMI	DP: 3.3V AC coupled on Module Runtime HDMI: 1.8V Runtime	PU 100KΩ to 3.3V or 1.8V **(S/W IC between Rpu/PCH)**	AC coupled on Module If DP1_AUX_SEL=0 (DP mode): AC coupled on module, 100k PU. If DP0_AUX_SEL=1 (HDMI mode): DC coupled, CMOS, 100k PU. In case of HDMI over DP++ implementation, stronger pull-up is demanded to the Carrier Board	DP1_AUX- for DP Pull-ups to 1.8V on each of these lines is required on the Carrier. The pull-ups may be part of an integrated HDMI ESD protection and control-line level shift device. If discrete Carrier pull-ups are used, they should be 10K or 100K pull-up to 1.8V. For HDMI Connector, connect to HDMI Conn pin 15 HDMI_CTRL_CK, pin 16 HDMI_CTRL_DAT and ESD protection
DP1_HPD/ HDMI_HPD	P104	I CMOS	1.8V Runtime	PD 100KΩ to GND	DDI for Display Port: DP0_HPD (Detection of Hot Plug / Unplug and notification of the link layer) DDI for HDMI/DVI: HDMI0_HPD (HDMI/DVI Hot-Plug Detect)	The carrier shall include a blocking FET on DP1_HPD to prevent back-drive current from damaging the module. Device - Connect to DP device Hot Plug Detect DP Connector - Connect to DP Conn pin 18 Hot Plug Detect HDMI Connector - HDMI Conn pin 19 Hot Plug Detect
DP1_AUX_SEL	P107	I CMOS	1.8V Runtime	PD 1MΩ to GND	Selects the function of DDI0_CTRLCLK_AUX+ and DDI0_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is unconnected the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals.	Pulled to GND on Carrier for DP operation in Dual Mode (DP++) implementations Module must tolerate high level in stand-by mode. Should be connected to pin 13 of the DisplayPort connector to enable a dual-mode DisplayPort interface.

Note : ASL600 default supports HDMI. DP2 is an option function.

▶ SMARC Connector Signal Description

MIPI CSI0 Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	ASL600 PU/PD	Module Base Specification R2.2 Description	SMARC Carrier Design Guide R2.2 Description
CSI0_RX0+	S11	I D-PHY/ I M-PHY Runtime			CSI0 differential data inputs.	CSI0_RX0+ Connect to Camera0 device pin CSI0_D0+ CSI0_RX0- Connect to Camera0 device pin CSI0_D0-
CSI0_RX0-	S12					
CSI0_RX1+	S14				CSI0 differential data inputs.	CSI0_RX1+ Connect to Camera0 device pin CSI0_D1+. CSI0_RX1- Connect to Camera0 device pin CSI0_D1-.
CSI0_RX1-	S15					
CSI0_CK+	S8	I D-PHY/ Runtime			CSI0 differential clock inputs	CSI0_CK+ Connect to Camera0 device pin CSI0_CK+. CSI0_CK- Connect to Camera0 device pin CSI0_CK-.
CSI0_CK-	S9					
I2C_CAM0_DAT / CSI0_TX-	S7	I/O OD CMOS / O M-PHY Runtime	1.8V	PU 2.2K	I2C data for serial camera data support link or differential data lane MIPI-CSI 2.0 uses I2C_CAM0_DAT which requires PU MIPI-CSI 3.0 uses CSI0_TX-, no PU required.	Connect to Camera0 device pin DAT0.
I2C_CAM0_CK / CSI0_TX+	S5	I/O OD CMOS / O M-PHY Runtime	1.8V	PU 2.2K	I2C clock for serial camera data support link or differential data lane MIPI-CSI 2.0 uses I2C_CAM0_CK which requires PU MIPI-CSI 3.0 uses CSI0_TX+, no PU required.	Connect to Camera0 device pin CK0.
CAM0_PWR#	P108	O CMOS Runtime	1.8V		Camera 0 Power Enable, active low output. Shared with GPIO0	
CAM0_RST#	P110	O CMOS Runtime	1.8V		Camera 0 reset, active low output Shared with GPIO2	

Note : MIPI-CSI is from chipset.

▶ SMARC Connector Signal Description

MIPI CSI1 Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	ASL600 PU/PD	Module Base Specification R2.2 Description	SMARC Carrier Design Guide R2.2 Description
CSI1_RX0+	P7	I D-PHY/ I M-PHY Runtime			CSI1 differential data inputs.	CSI1_RX0+ Connect to Camera0 device pin CSI0_D0+ CSI1_RX0- Connect to Camera0 device pin CSI0_D0-
CSI1_RX0-	P8					
CSI1_RX1+	P10				CSI1 differential data inputs.	CSI1_RX1+ Connect to Camera0 device pin CSI0_D1+. CSI1_RX1- Connect to Camera0 device pin CSI0_D1-.
CSI1_RX1-	P11					
CSI1_RX2+	P13	I D-PHY/ I M-PHY Runtime			CSI1 differential data inputs.	CSI1_RX2+ Connect to Camera0 device pin CSI0_D0+ CSI1_RX2- Connect to Camera0 device pin CSI0_D0-
CSI1_RX2-	P14					
CSI1_RX3+	P16				CSI1 differential data inputs.	CSI1_RX3+ Connect to Camera0 device pin CSI0_D1+. CSI1_RX3- Connect to Camera0 device pin CSI0_D1-.
CSI1_RX3-	P17					
CSI1_CK+	P3	I D-PHY/ Runtime			CSI1 differential clock inputs	CSI1_CK+ Connect to Camera0 device pin CSI0_CK+. CSI1_CK- Connect to Camera0 device pin CSI0_CK-.
CSI1_CK-	P4					
I2C_CAM1_DAT / CSI1_TX-	S2	I/O OD CMOS / O M-PHY Runtime	1.8V	PU 2.2K	I2C data for serial camera data support link or differential data lane MIPI-CSI 2.0 uses I2C_CAM0_DAT which requires PU MIPI-CSI 3.0 uses CSI0_TX-, no PU required.	Connect to Camera1 device pin DAT0.
I2C_CAM1_CK / CSI1_TX+	S1	I/O OD CMOS / O M-PHY Runtime	1.8V	PU 2.2K	I2C clock for serial camera data support link or differential data lane MIPI-CSI 2.0 uses I2C_CAM0_CK which requires PU MIPI-CSI 3.0 uses CSI0_TX+, no PU required.	Connect to Camera 1 device pin CK0.
CAM1_PWR#	P109	O CMOS Runtime	1.8V		Camera 1 Power Enable, active low output. Shared with GPIO0	
CAM1_RST#	P111	O CMOS Runtime	1.8V		Camera 1 reset, active low output Shared with GPIO2	
CAM_MCK	S6	O CMOS Runtime	1.8V		Master clock output	

▶ SMARC Connector Signal Description

CAN BUS Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	ASL600 PU/PD	Module Base Specification R2.2 Description	SMARC Carrier Design Guide R2.2 Description
CAN0_TX	P143	O CMOS / Runtime	1.8V		CAN0 Transmit output	Connect to CAN Bus transceiver transmit data input TXD pin
CAN0_RX	P144	I CMOS / Runtime			CAN0 Transmit input	Connect to CAN Bus transceiver receive data output RXD pin
CAN1_TX	P145	O CMOS / Runtime	1.8V		CAN1 Transmit output	Connect to CAN Bus transceiver transmit data input TXD pin
CAN1_RX	P146	I CMOS / Runtime			CAN1 Transmit input	Connect to CAN Bus transceiver receive data output RXD pin

GPIO Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	ASL600 PU/PD	Module Base Specification R2.2 Description	SMARC Carrier Design Guide R2.2 Description
GPIO0 / CAM0_PWR#	P108	I/O CMOS / Runtime	1.8V	PU 470k (Note)	GPIO Pin 0 Preferred Output	Share with CAM0_PWR# & DIO. by jumper
GPIO1 / CAM1_PWR#	P109	I/O CMOS / Runtime		PU 470k (Note)	GPIO Pin 1 Preferred Output.	Share with CAM1_PWR# & DIO. by jumper
GPIO2 / CAM0_RST#	P110	I/O CMOS / Runtime		PU 470k (Note)	GPIO Pin 2 Preferred Output	Share with CAM0_RST# & DIO. by jumper
GPIO3 / CAM1_RST#	P111	I/O CMOS / Runtime		PU 470k (Note)	GPIO Pin 3 Preferred Output	Share with CAM1_RST# & DIO. by jumper
GPIO4 / HDA_RST#	P112	I/O CMOS / Runtime		PU 470k (Note)	GPIO Pin 4 Preferred Output	Share with HDA_RST# & DIO. by jumper
GPIO5 / PWM_OUT#	P113	I/O CMOS / Runtime		PU 470k (Note)	GPIO Pin 5 Preferred Output	Share with PWM_OUT# & DIO. by jumper
GPIO6 / TACHIN	P114	I/O CMOS / Runtime		PU 470k (Note)	GPIO Pin 6 Preferred Input	Share with TACHIN & DIO. by jumper
GPIO7 / SERDES0_INT#	P115	I/O CMOS / Runtime		PU 470k (Note)	GPIO Pin 7 Preferred Input	Share with DIO. by jumper
GPIO8 / SERDES1_INT#	P116	I/O CMOS / Runtime		PU 470k (Note)	GPIO Pin 8 Preferred Input	Share with DIO by jumper
GPIO9	P117	I/O CMOS / Runtime		PU 470k (Note)	GPIO Pin 9 Preferred Input	Share with DIO by jumper
GPIO10	P118	I/O CMOS / Runtime		PU 470k (Note)	GPIO Pin 10 Preferred Input	Share with DIO by jumper
GPIO11	P119	I/O CMOS / Runtime		PU 470k (Note)	GPIO Pin 11 Preferred Input	Share with DIO by jumper
GPIO12	S142	I/O CMOS / Runtime		PU 470k (Note)	GPIO Pin 12 Preferred Input	Share with DIO by jumper
GPIO13	S123	I/O CMOS / Runtime		PU 470k (Note)	GPIO Pin 13 Preferred Input	Share with DIO by jumper

▶ SMARC Connector Signal Description

FAN Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	ASL600 PU/PD	Module Base Specification R2.2 Description	SMARC Carrier Design Guide R2.2 Description
PWM_OUT/ GPIO5	P113	O CMOS	1.8V Runtime		Primary functionality is fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the Fan's RPM based on the CPU's die temperature.	
TACHIN / GPIO6	P114	I CMOS	1.8V Runtime		Primary functionality is fan tachometer input. When not in use for this primary purpose it can be used as General Purpose Timer Input.	

Miscellaneous Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	ASL600 PU/PD	Module Base Specification R2.2 Description	SMARC Carrier Design Guide R2.2 Description
BATLOW#	S156	I/OD CMOS	1.8V to5V Standby/Sleep	PU 10k	Pulled up on Module.	Carrier to float the line in in-active state. Reserved function by DIP switch.
CARRIER_PWR_ON	S154	O CMOS	1.8V Standby/Sleep		Carrier Board circuits (apart from power management and power path circuits) should not be powered up until the Module asserts the CARRIER_PWR_ON signal. On x86 designs this pin should utilize a standby related power signal i.e. RSM_RST# or SLP_A# signal.	
CARRIER_STBY#	S153	I/O CMOS	1.8V Standby/Sleep		The Module shall drive this signal low when the system is in a standby power state. On x86 designs this pin should utilize the SUS_S3# signal.	
CHARGER_PRSNT#	S152	I OD CMOS	1.8V or 5V / Standby/Sleep	PU 10K Ω	Held low by Carrier if DC input for battery charger is present.	Driven by OD part on Carrier. Reserved function by DIP switch.
CHARGING#	S151	I OD CMOS	1.8V or 5V / Standby/Sleep	PU 10K Ω	Held low by Carrier during battery charging. Carrier to float the line when charge is complete.	Driven by OD part on Carrier. Reserved function by DIP switch.
VIN_PWR_BAD#	S150	I OD CMOS	VDD_IN	PU 10K Ω	Pulled up on Module.	Power bad indication from Carrier board. Driven by OD part on Carrier. (other than Module and Carrier power supervisory circuits) shall not be enabled while this signal is held low by the Carrier.
SLEEP#	S149	I OD CMOS	1.8V or 3.3V	PU 10K Ω	Active low, level sensitive. Should be de-bounced on the Module. Pulled up on Module.	Driven by OD part on Carrier.
LID#	S148	I/ OD CMOS	1.8V or 5V / Standby	PU 10K Ω	Active low, level sensitive. Should be de-bounced on the Module. Pulled up on Module.	Driven by OD part on Carrier.
POWER_BTN#	P128	I OD CMOS	1.8V or 5V / Standby/Sleep	PU 10K Ω	Active low, level sensitive. Should be de-bounced on the Module. Pulled up on Module.	Driven by OD part on Carrier.
RESET_OUT#	P126	O CMOS	1.8V / Standby		General purpose reset output to Carrier Board.	
RESET_IN#	P127	I/ OD CMOS	1.8V or 5V / Standby	PU 10K Ω	Pulled up on Module. Reset input from Carrier Board. Carrier drives low to force a Module reset, floats the line otherwise. This signal Shall be level triggered during bootup to allow to stop booting of the module. After bootup it May act as an edge triggered signal.	Driven by OD part on Carrier.
TEST#	S157	I /OD CMOS	1.8V or 5V / Standby/Sleep	PU vendor specific value	Pulled up on Module. The Module TEST# pin (pin S157) should normally be left not connected. If pulled low, then Module specific test function(s) may be enabled.	Carrier to float the line in in-active state. Driven by OD part on Carrier. Reserved function by DIP switch.
WDT_TIME_OUT#	S145	O CMOS	1.8V / Runtime		Watch-Dog-Timer Output	Connect to Watchdog trigger input

▶ SMARC Connector Signal Description

I2C_GP Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	ASL600 PU/PD	Module Base Specification R2.2 Description	SMARC Carrier Design Guide R2.2 Description
I2C_GP_CK	S48	I/OD CMOS	1.8V Runtime	PU 2.2K Ω	General Purpose I2C Clock output. This signal has 2.2K Ω pull up to 1.8V on the module.	Connect to CLK of I2C device. Reserved for I2C/I2S header, eDP,DP
I2C_GP_DAT	S49	I/OD CMOS	1.8V Runtime	PU 2.2K Ω	General Purpose I2C data I/O line. This signal has 2.2K Ω pull up to 1.8V on the module.	Connect to SDA of I2C device Reserved for I2C/I2S header, eDP,DP

Note: Default from EC, Chipset is option function.

I2C_PM Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	ASL600 PU/PD	Module Base Specification R2.2 Description	SMARC Carrier Design Guide R2.2 Description
I2C_PM_DAT#	P122	I/O OD CMOS	1.8V	PU 2.2K Ω	Power management I2C bus DATA On x86 systems these serve as SMB DATA.	Reserved for SMBUS header, M.2-E, M.2-B.
I2C_PM_CK#	P121	I/O OD CMOS	1.8V	PU 2.2K Ω	Power management I2C bus CLK On x86 systems these serve as SMB CLK	Reserved for SMBUS header, M.2-E, M.2-B.
SMB_ALERT#	P1	I/OD CMOS	1.8V or 5V / Standby/Sleep	PU 2.2K Ω	SMBus Alert# (Interrupt) Signal	Connect to SMBALERT# of SMBus device

Note: I2C_PM is from chipset, EC is option function.

Serial Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	ASL600 PU/PD	Module Base Specification R2.2 Description	SMARC Carrier Design Guide R2.2 Description
SER0_TX	P129	O CMOS	1.8V / Runtime		Asynchronous Serial Data Output Port 0 (Note1)	COM DB-9 port - TxIN of Serial Transceiver and TxOUT to DB-9 pin 3 TXD
SER0_RX	P130	I CMOS	1.8V / Runtime		Asynchronous Serial Data Input Port 0 (Note1)	COM DB-9 port - TxOUT of Serial Transceiver and TxIN to DB-9 pin 2 RXD
SER0_RTS#	P131	O CMOS	1.8V / Runtime		Request to Send Handshake Line for Port 0 (Note1)	COM DB-9 port - TxOUT of Serial Transceiver and TxIN to DB-9 pin 7 RTS#
SER0_CTS#	P132	I CMOS	1.8V / Runtime		Clear to Send Handshake Line for Port 0 (Note1)	COM DB-9 port - TxIN of Serial Transceiver and TxOUT to DB-9 pin 8 CTS#
SER1_TX	P134	O CMOS	1.8V / Runtime		Asynchronous Serial Data Output Port 1 (Note1)	COM DB-9 port - TxIN of Serial Transceiver and TxOUT to DB-9 pin 3 TXD
SER1_RX	P135	I CMOS	1.8V / Runtime		Asynchronous Serial Data Input Port 1 (Note1)	COM DB-9 port - TxOUT of Serial Transceiver and TxIN to DB-9 pin 2 RXD
SER2_TX	P136	O CMOS	1.8V / Runtime		Asynchronous Serial Data Output Port 2 (Note2)	COM DB-9 port - TxIN of Serial Transceiver and TxOUT to DB-9 pin 3 TXD
SER2_RX	P137	I CMOS	1.8V / Runtime		Asynchronous Serial Data Input Port 2 (Note2)	COM DB-9 port - TxOUT of Serial Transceiver and TxIN to DB-9 pin 2 RXD
SER2_RTS#	P138	OCMOS	1.8V / Runtime		Request to Send Handshake Line for Port 2 (Note2)	COM DB-9 port - TxOUT of Serial Transceiver and TxIN to DB-9 pin 7 RTS#
SER2_CTS#	P139	I CMOS	1.8V / Runtime		Clear to Send Handshake Line for Port 2 (Note2)	COM DB-9 port - TxIN of Serial Transceiver and TxOUT to DB-9 pin 8 CTS#
SER3_TX	P140	O CMOS	1.8V / Runtime		Asynchronous Serial Data Output Port 3 (Note2)	COM DB-9 port - TxIN of Serial Transceiver and TxOUT to DB-9 pin 3 TXD
SER3_RX	P141	I CMOS	1.8V / Runtime		Asynchronous Serial Data Input Port 3 (Note2)	COM DB-9 port - TxOUT of Serial Transceiver and TxIN to DB-9 pin 2 RXD

▶ SMARC Connector Signal Description

SPI Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	ASL600 PU/PD	Module Base Specification R2.2 Description	SMARC Carrier Design Guide R2.2 Description
SPI0_CS0#	P43	O CMOS	1.8V / Standby		SPI0 Master Chip Select 0 This signal can be used to select Carrier SPI as boot device.	Connect to SPI_CS0#
SPI0_CS1#	P31	O CMOS	1.8V / Standby		SPI0 Master Chip Select 1	N.C
SPI0_CK	P44	O CMOS	1.8V / Standby		SPI0 Clock	Connect to SPI_CK
SPI0_DIN	P45	I CMOS	1.8V / Standby		SPI0 Master input / Slave output	Connect to SPI_MISO
SPI0_DO	P46	O CMOS	1.8V / Standby		SPI0 Master output / Slave input	Connect to SPI_MOSI
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	ASL600 PU/PD	Module Base Specification R2.2 Description	SMARC Carrier Design Guide R2.2 Description
SPI1_CS0#	P54	O CMOS	1.8V / Standby		SPI1 Master Chip Select 0	Share with ESPI and GSPI_CS0#
SPI1_CS1#	P55	O CMOS	1.8V / Standby		SPI1 Master Chip Select 1	Connect to ESPI_CS1#
SPI1_CK	P56	O CMOS	1.8V / Standby		SPI1 Clock	Share with ESPI and GSPI_CK
SPI1_DIN	P57	I CMOS	1.8V / Standby		SPI1 Master input / Slave output	Share with ESPI and GSPI_ MISO
SPI1_DO	P58	O CMOS	1.8V / Standby		SPI1 Master output / Slave input	Share with ESPI and GSPI_ MOSI

▶ SMARC Connector Signal Description

ESPI Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	ASL600 PU/PD	Module Base Specification R2.2 Description	SMARC Carrier Design Guide R2.2 Description
ESPI_CSO#	P54	O CMOS	1.8V / Standby		ESPI Master Chip Select 0 This signal can be used to select Carrier SPI as boot device.	Connect to ESPI_CS0#
ESPI_CS1#	P55	O CMOS	1.8V / Standby		ESPI Master Chip Select 1	Connect to ESPI_CS0#
ESPI_CK	P56	O CMOS	1.8V / Standby		ESPI Master Clock Output	Connect to ESPI_CK Shall have a 33 Ω series termination
ESPI_RESET#	S58	O CMOS	1.8V / Standby		ESPI Reset	Connect to ESPI_RESET
ESPI_ALERT0#	S43	I OD CMOS	1.8V / Standby		ESPI ALERT0	Connect to ESPI_ALERT0#
ESPI_ALERT1#	S44	I OD CMOS	1.8V / Standby		ESPI ALERT1	Connect to ESPI_ALERT1#
ESPI_IO_0	P58	I/O CMOS	1.8V / Standby		ESPI Master Data Input / Output0	Connect to ESPI_IO_0 Shall have a 33 Ω series termination
ESPI_IO_1	P57	I/O CMOS	1.8V / Standby		ESPI Master Data Input / Output1	Connect to ESPI_IO_1 Shall have a 33 Ω series termination
ESPI_IO_2	S56	I/O CMOS	1.8V / Standby		ESPI Master Data Input / Output2	Connect to ESPI_IO_2 Shall have a 33 Ω series termination
ESPI_IO_3	S57	I/O CMOS	1.8V / Standby		ESPI Master Data Input / Output3	Connect to ESPI_IO_3 Shall have a 33 Ω series termination

▶ SMARC Connector Signal Description

Boot Select Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	ASL600 PU/PD	Module Base Specification R2.2 Description	SMARC Carrier Design Guide R2.2 Description
BOOT_SEL0# BOOT_SEL1# BOOT_SEL2#	P123 P124 P125	I OD CMOS	1.8V / Standby	PU 10K	Input straps determine the Module boot device.	Driven by OD on Carrier. DIP switch retains function.
FORCE_RECOV#	S155	I OD CMOS	1.8V / Standby	PU 10K	Low on this pin allows non-protected segments of Module boot device to be rewritten / restored from an external USB Host on Module USB0. The Module USB0 operates in Client Mode when in the Force Recovery function is invoked. For SOCs that do not implement a USB based Force Recovery functions, then a low on the Module FORCE_RECOV# pin may invoke the SOC native Force Recovery mode – such as over a Serial Port. For x86 systems this signal may be used to load BIOS defaults.	Driven by OD on Carrier. DIP switch retains function.

Note:1. BOOT_SEL0, BOOT_SEL1, BOOT_SEL2 this signal is from EC.
2. FORCE_RECOV signal is from chipset.

Power and GND Signals Descriptions

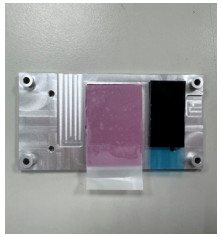
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	ASL600 PU/PD	Module Base Specification R2.2 Description	SMARC Carrier Design Guide R2.2 Description
VDD_IN	P147, P148, P149, P150, P151, P152, P153, P154, P155, P156	Power In	5V		Module power input voltage – 5V only	
GND	P2, P9, P12, P15, P18, P32, P38, P47, P50, P53, P59, P68, P79, P82, P85, P88, P91, P94, P97, P100, P103, P120, P133, P142, S3, S10, S16, S25, S34, S47, S61, S64, S67, S70, S73, S80, S83, S86, S89, S92, S101, S110, S119, S124, S130, S136, S143, S158	GND				
VDD_RTC	S147	Power In Power Out	3V		Low current RTC circuit backup power – 3.0V nominal May be sourced from a Carrier based Lithium cell or Super Cap	Low current RTC circuit backup power – 3.0V nominal May be sourced from a Carrier based Lithium cell or Super Cap.

▶ Cooling Option

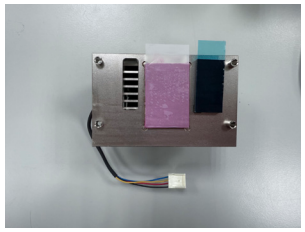
Cooling Solutions

ASL600 SMARC product comes with a heat spreader as standard equipment. An optional cooler can be added for enhanced thermal performance.

a heat spreader



a cooler

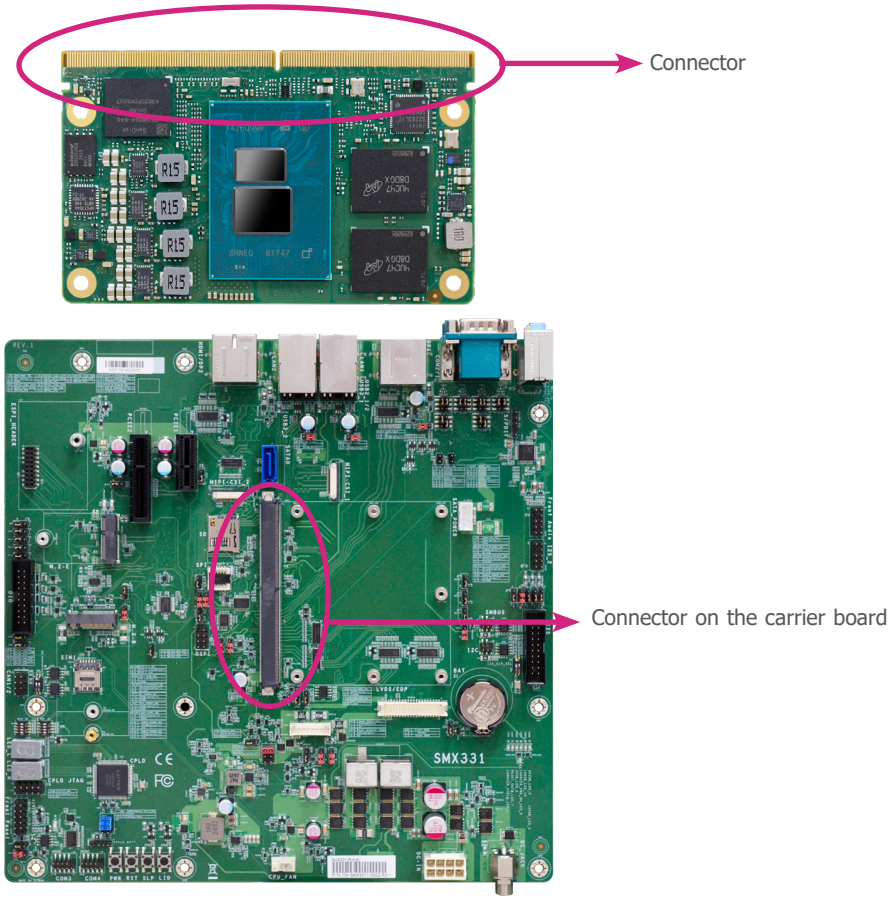


Important:
Remove the plastic covering from the thermal pads prior to mounting the heat sink onto board.

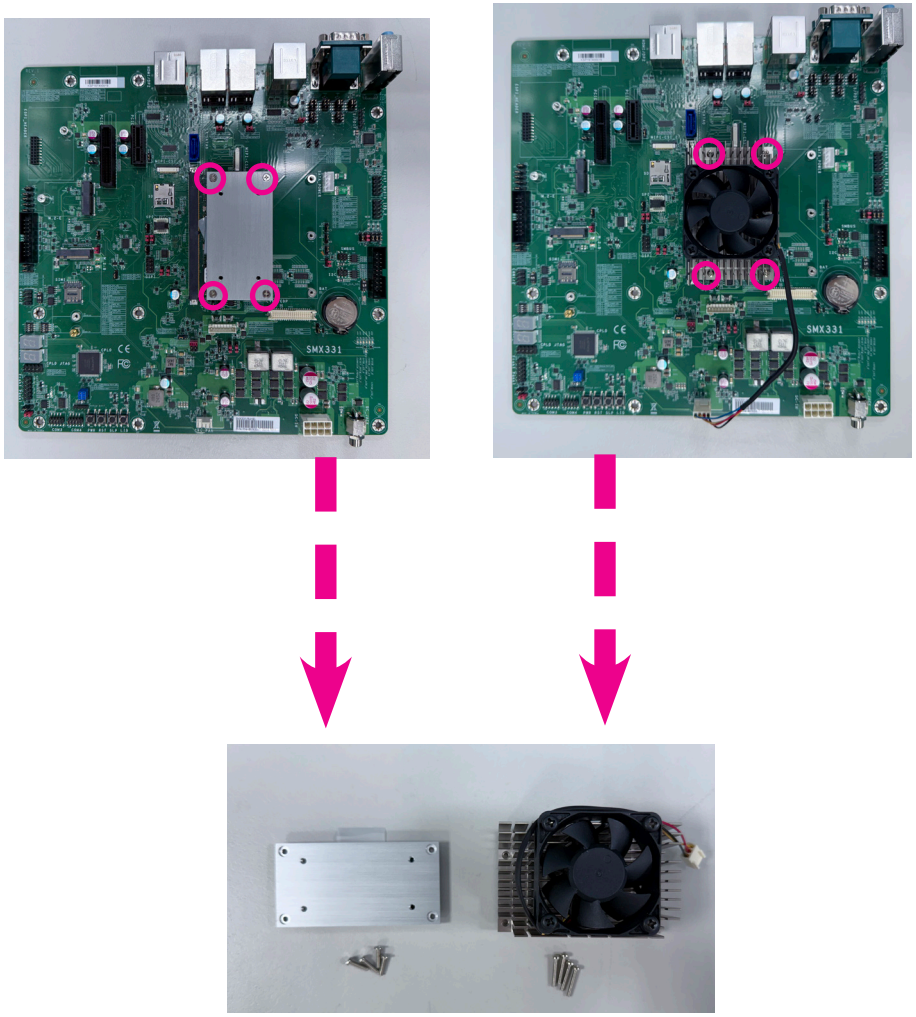
▶ Installing ASL600 onto a Carrier Board

Important:
The carrier board (SMX331) used in this section is for reference purpose only and may not resemble your carrier board. These illustrations are mainly to guide you on how to install ASL600 onto the carrier board of your choice.

1. Grasp ASL600 SMARC by its edges and position it on top of the carrier board. Apply firm even pressure to the side with ASL600 SMARC connector first and insert the entire module. Be careful when pressing the module to avoid damaging it. You will hear a distinctive “click”, indicating the module is correctly locked into position.



2. Align the mounting holes of a heat spreader or a heatsink with the mounting holes of the module. Use the provided mounting screws to install the heat sink onto the module.



Chapter 4 - BIOS Setup

Overview

The BIOS is a program that takes care of the basic level of communication between the CPU and peripherals. It contains codes for various advanced features found in this system board. The BIOS allows you to configure the system and save the configuration in a battery-backed CMOS so that the data retains even when the power is off. In general, the information stored in the CMOS RAM of the EEPROM will stay unchanged unless a configuration change has been made such as a hard drive replaced or a device added.

It is possible that the CMOS battery will fail causing CMOS data loss. If this happens, you need to install a new CMOS battery and reconfigure the BIOS settings.

Note:
The BIOS is constantly updated to improve the performance of the system board; therefore the BIOS screens in this chapter may not appear the same as the actual one. These screens are for reference purpose only.

Default Configuration

Most of the configuration settings are either predefined according to the Load Optimal Defaults settings which are stored in the BIOS or are automatically detected and configured without requiring any actions. There are a few settings that you may need to change depending on your system configuration.

Entering the BIOS Setup Utility

The BIOS Setup Utility can only be operated from the keyboard and all commands are keyboard commands. The commands are available at the right side of each setup screen.
The BIOS Setup Utility does not require an operating system to run. After you power up the system, the BIOS message appears on the screen and the memory count begins. After the memory test, the message “Press DEL to run setup” will appear on the screen. If the message disappears before you respond, restart the system or press the “Reset” button. You may also restart the system by pressing the <Ctrl> <Alt> and <Del> keys simultaneously.

Legends

KEYs	Function
Right and Left Arrows	Moves the highlight left or right to select a menu.
Up and Down Arrows	Moves the highlight up or down between submenus or fields.
<Esc>	Exits to the BIOS setup utility
+ (plus key)	Scrolls forward through the values or options of the hightlighted field.
- (minus key)	Scolls backward through the values or options of the hightlighted field.
<F1>	Displays general help
<F2>	Displays previous values
<F9>	Optimized defaults
<F10>	Saves and reset the setup program.
<Enter>	Press <Enter> to enter the highlighted submenu

Scroll Bar

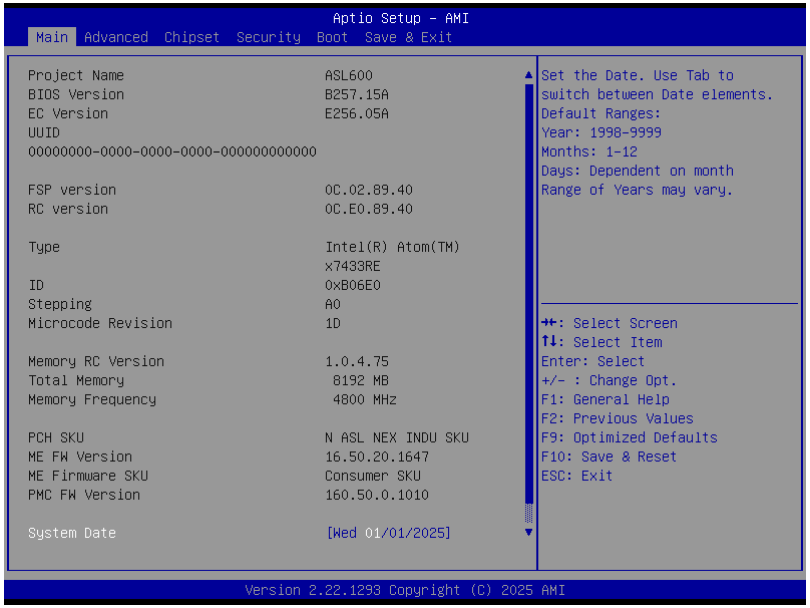
When a scroll bar appears to the right of the setup screen, it indicates that there are more available fields not shown on the screen. Use the up and down arrow keys to scroll through all the available fields.

Submenu

When “▶” appears on the left of a particular field, it indicates that a submenu which contains additional options are available for that field. To display the submenu, move the highlight to that field and press <Enter>.

▶ Main

The Main menu is the first screen that you will see when you enter the BIOS Setup Utility.



System Date

The date format is <month>, <date>, <year>. Press "Tab" to switch to the next field and press "-" or "+" to modify the value.

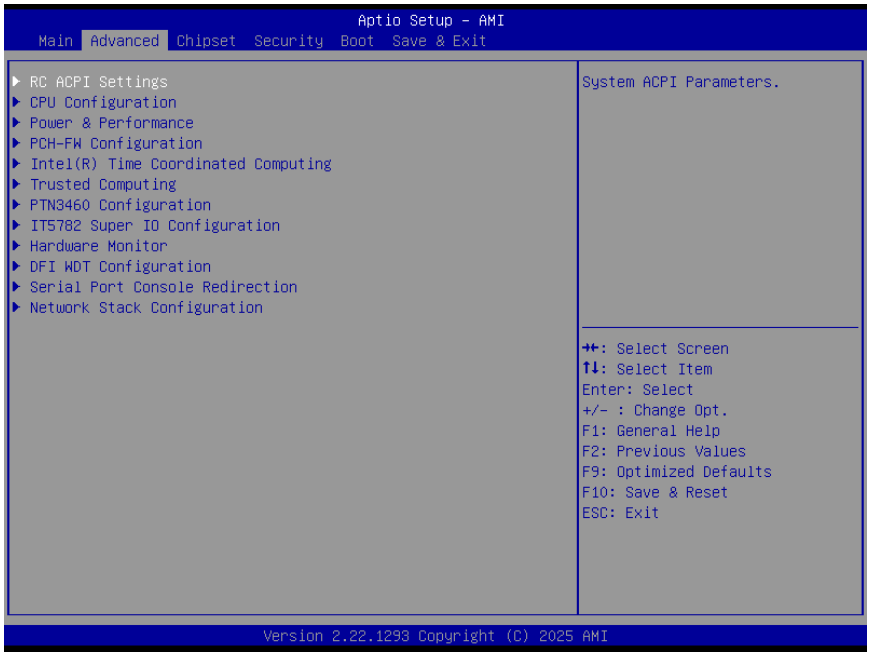
System Time

The time format is <hour>, <minute>, <second>. The time is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Hour displays hours from 00 to 23. Minute displays minutes from 00 to 59. Second displays seconds from 00 to 59.

▶ Advanced

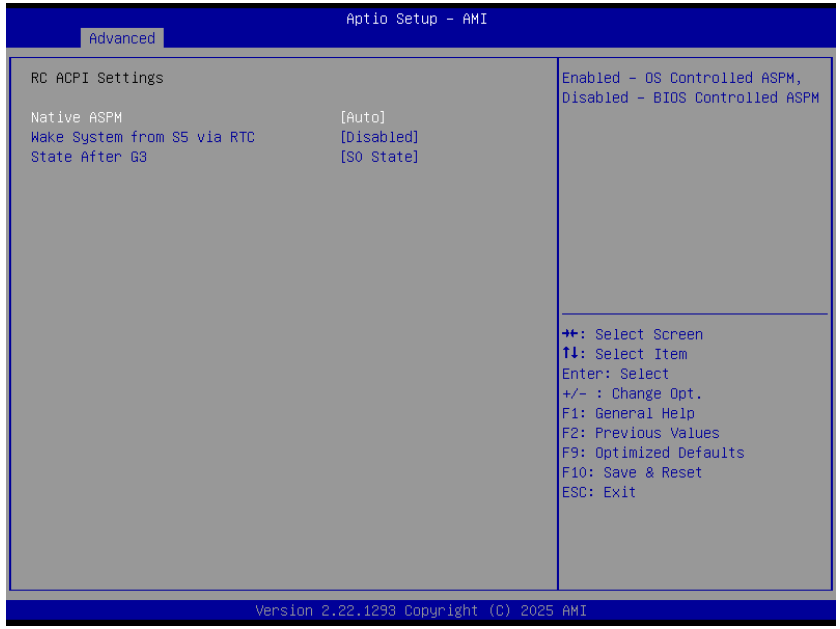
The Advanced menu allows you to configure your system for basic operation. Some entries are defaults required by the system board, while others, if enabled, will improve the performance of your system or let you set some features according to your preference.

Important:
Setting incorrect field values may cause the system to malfunction.



▶ Advanced

RC ACPI Configuration



Native ASPM

Enabled- OS Controlled ASPM.
Disabled - BIOS Controlled ASPM.

Wake system from S5 via RTC

When Enabled, the system will automatically power up at a designated time every day. Once it's switched to [Enabled], please set up the time of day — hour, minute, and second — for the system to wake up.

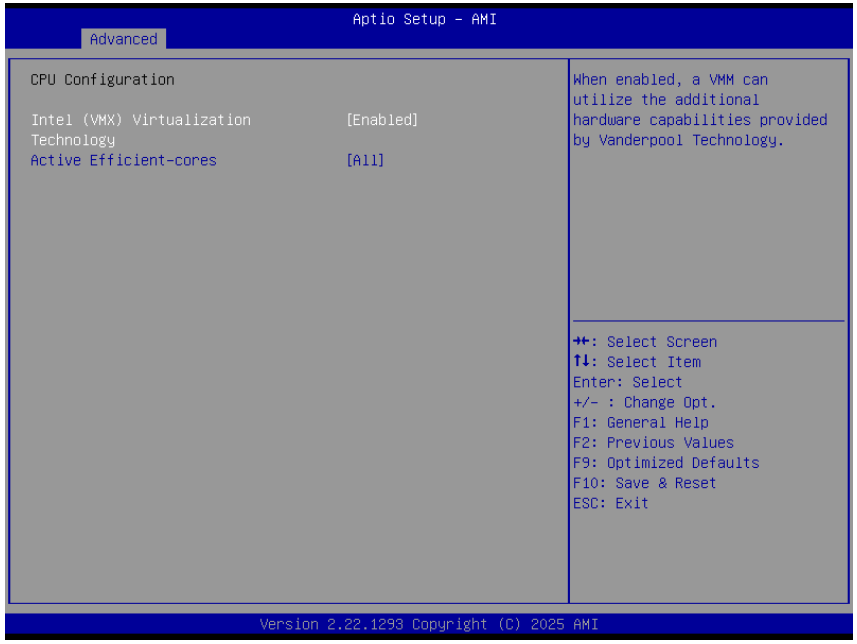
State After G3

Select between S0 State, and S5 State. This field is used to specify what state the system is set to return to when power is re-applied after a power failure (G3 state).

- **S0 State** The system automatically powers on after power failure.
- **S5 State** The system enter soft-off state after power failure. Power-on signal input is required to power up the system.

▶ Advanced

CPU Configuration



Intel (VMX) Virtualization Technology

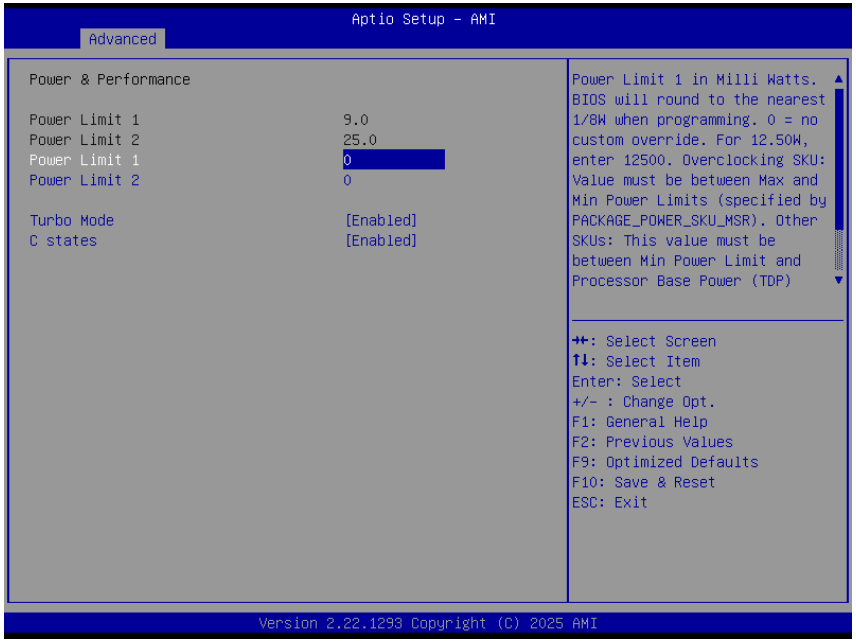
When this field is set to Enabled, the VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

Active Processor Cores

Select number of cores to enable in each processor package.

▶ Advanced

Power & Performance



Turbo Mode

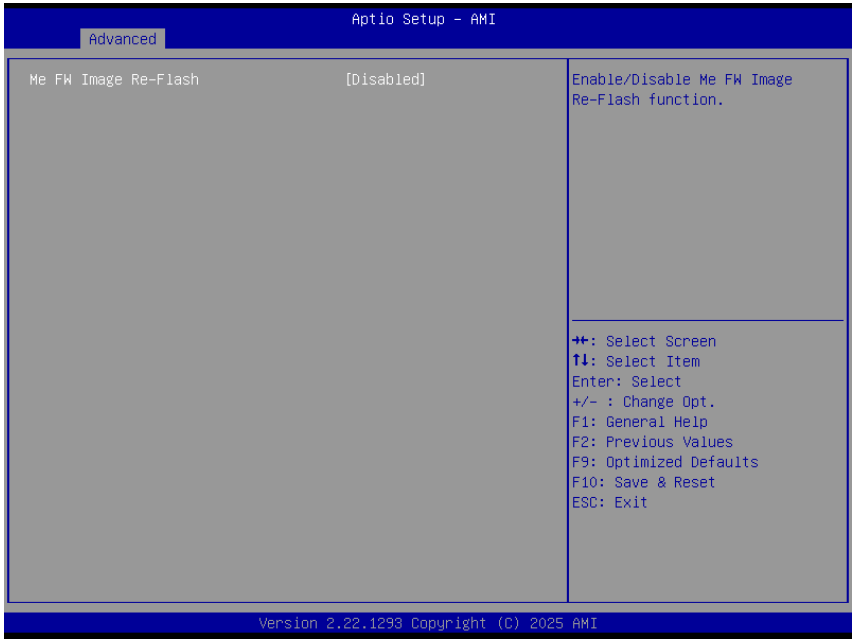
Enable or disable turbo mode of the processor.
This field will only be displayed when EIST is enabled.

C states

Enable or disable CPU Power Management. It allows CPU to enter "C states" when it's idle and nothing is executing.

▶ Advanced

PCH-FW Configuration

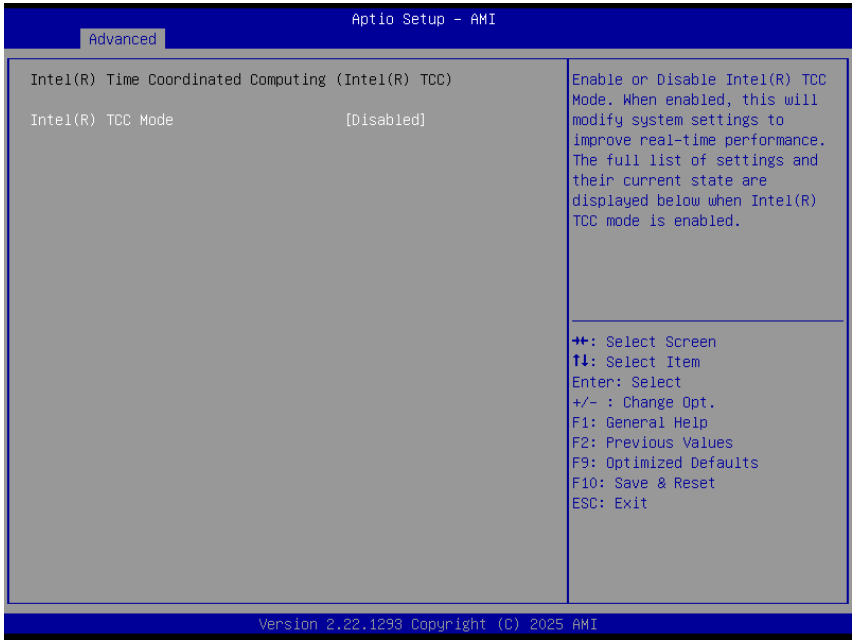


ME FW Image Re-Flash

Enable / Disable Me FW Image Re-Flash function.

▶ Advanced

Intel(R) Time Coordinated Computing



Enable or Disable Intel(R) TCC Mode. When enbaled, this will modify system settings to improve real-time performance.

▶ Advanced

Trusted Computing

Security Device Support

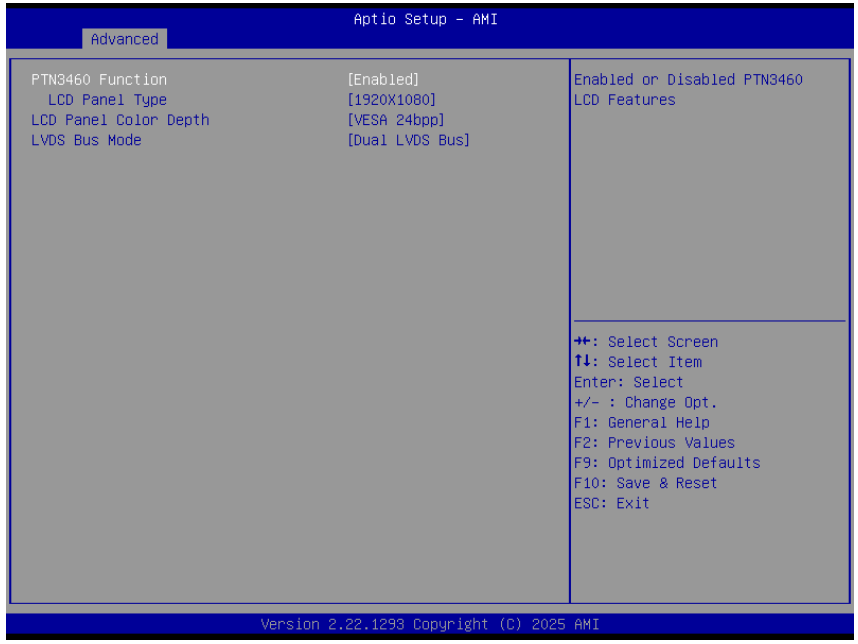
This field is used to enable or disable BIOS support for the security device such as an TPM 2.0 to achieve hardware-level security via cryptographic keys.

Pending operation

To clear the existing TPM encryption, select "TPM Clear" and restart the system. This field is not available when "Security Device Support" is disabled.

▶ Advanced

PTN3460 Configuration



PTN3460 Function

Enable or Disable PTN3460 LCD Features. When this field is disabled, the following fields will remain hidden.

LCD Panel Type

Select the resolution of the LCD Panel — 800X480, 800X600, 1024X768, 1366X768, 1280X1024, 1920X1080, or 1920X1200.

LCD Panel Color Depth

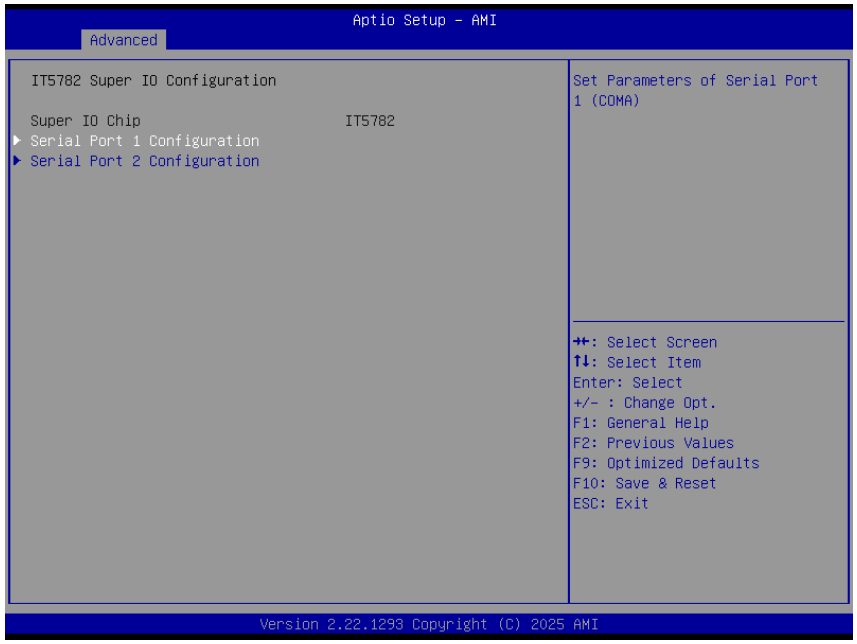
Select the color depth of the LCD Panel — VESA 24bpp, JEIDA 24bpp, VESA and JEIDA 18 bpp.

LVDS Bus Mode

Select PTN3460 LVDS BUS Mode : Single LVDS Bus /Dual LVDS Bus

▶ Advanced

IT5782 Super IO Configuration

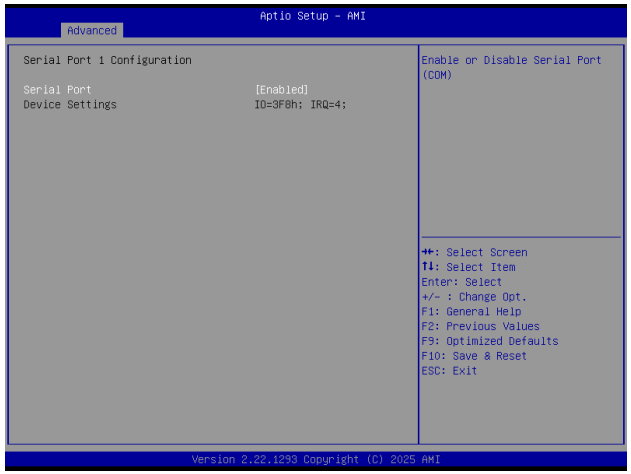


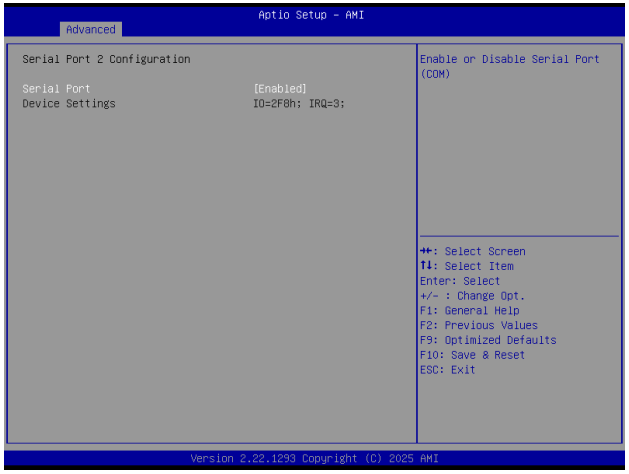
Serial Port Configuration

Set Parameters of Serial Ports. See next page.

▶ Advanced

IT5782 Super IO Configuration ▶ Serial Port 1, 2 Configuration



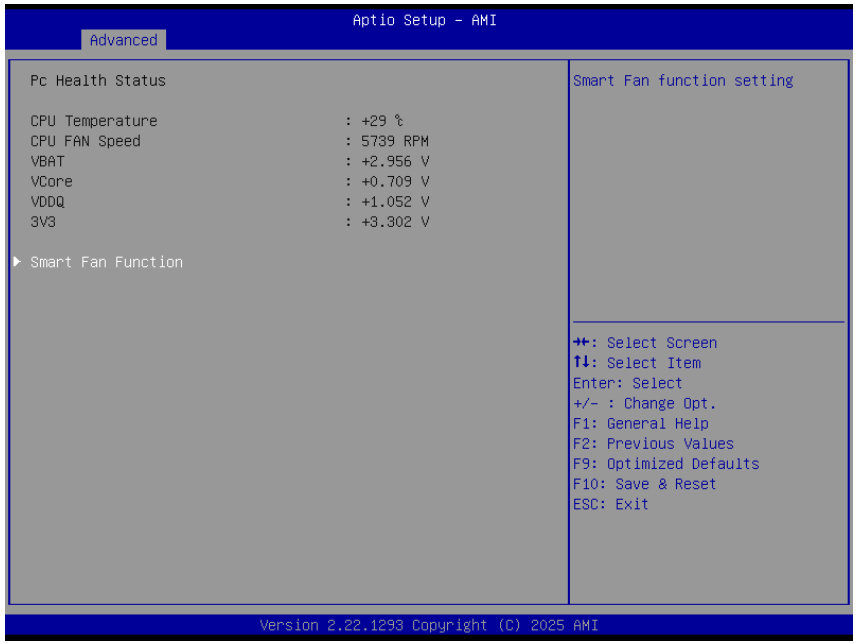


Serial Port

Enable or disable serial port.

▶ Advanced

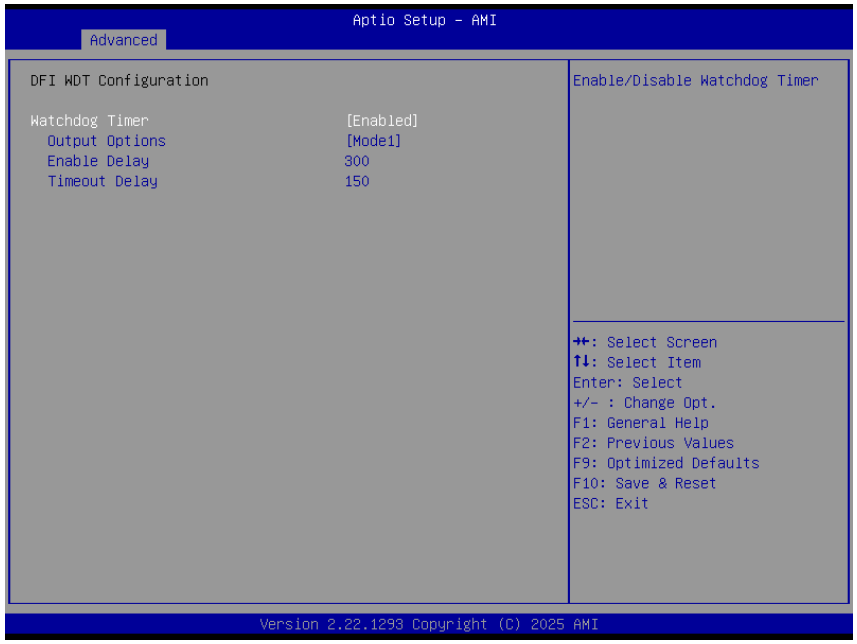
Hardware Monitor



Lists voltage, termperature, and fan speed.

▶ Advanced

DFI WDT Configuration



Watchdog Timer

Enable or disable watchdog timer.

Output Options

Mode1 = A Watchdog timeout causes the system to be reset.
Mode2 = WDT pin goes high upon timeout of the watchdog timer.
Mode3 = Generate NMI upon timeout of the watchdog timer.

Enable Delay

The enable delay allows time for the OS to boot and the application to load and initialize.

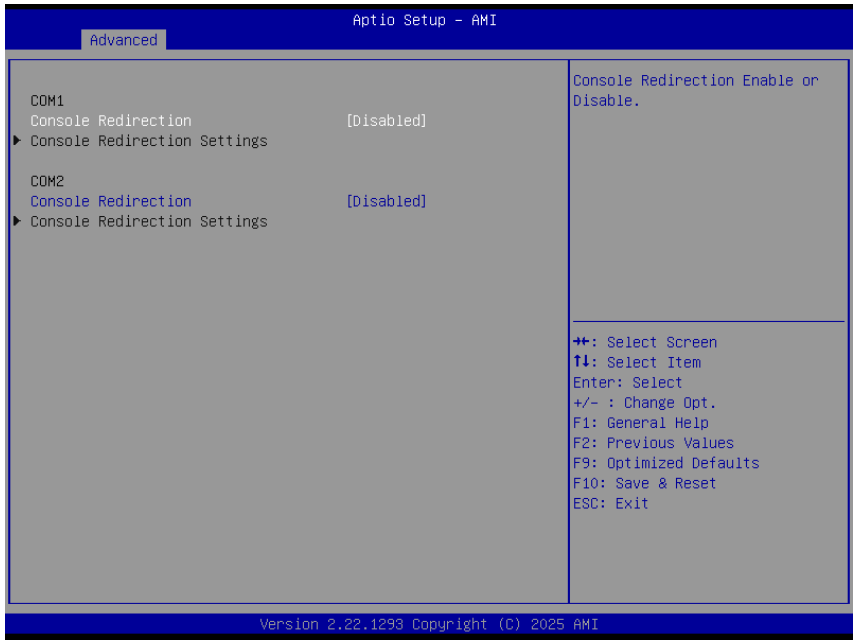
The unit is 1 sec.

Timeout Delay

The timeout delay allows time for period of the watchdog timer. The unit is 0.1 sec.

▶ Advanced

Serial Port Console Redirection



Console Redirection

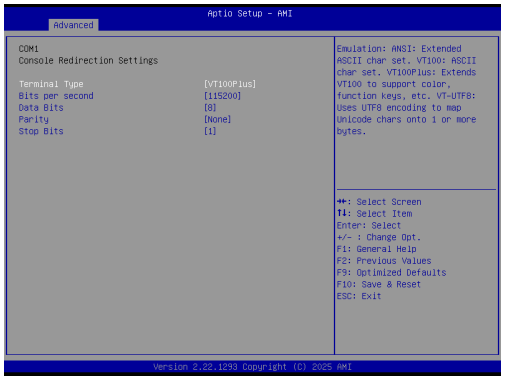
Console Redirection Enable or Disable.

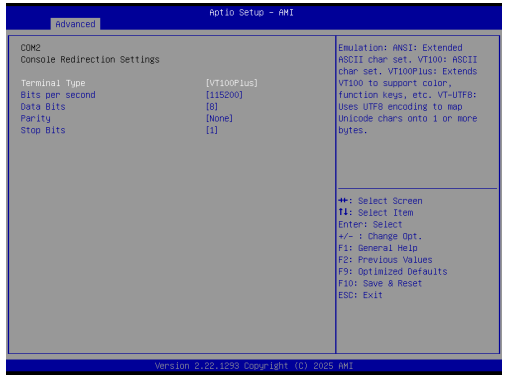
Console Redirection Settings

See following pages.

▶ Advanced

Serial Port Console Redirection ▶ Console Redirection Settings





Configure the serial settings of the current COM port.

Terminal Type

Select terminal type: VT100, VT100+, VT-UTF8 or ANSI.

Bits per second

Select serial port transmission speed: 9600, 19200, 38400, 57600 or 115200.

Data Bits

Select data bits: 7 bits or 8 bits.

Parity

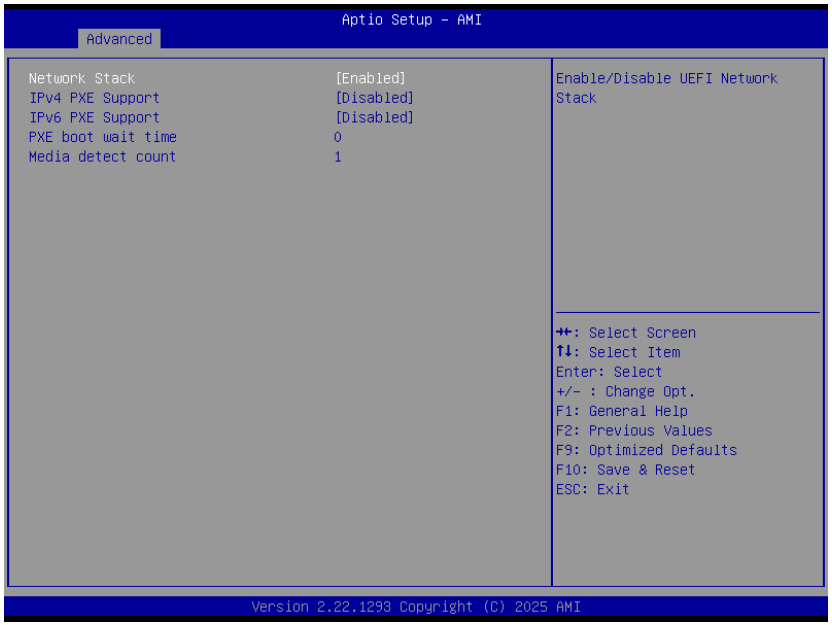
Select parity bits: None, Even, Odd, Mark or Space.

Stop Bits

Select stop bits: 1 bit or 2 bits.

▶ Advanced

Network Stack Configuration



Network Stack

Enable or disable (Default) UEFI network stack. The following fields will appear when this field is enabled.

Ipv4 PXE Support Enable or disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.

Ipv6 PXE Support

Enable or disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.

PXE boot wait time

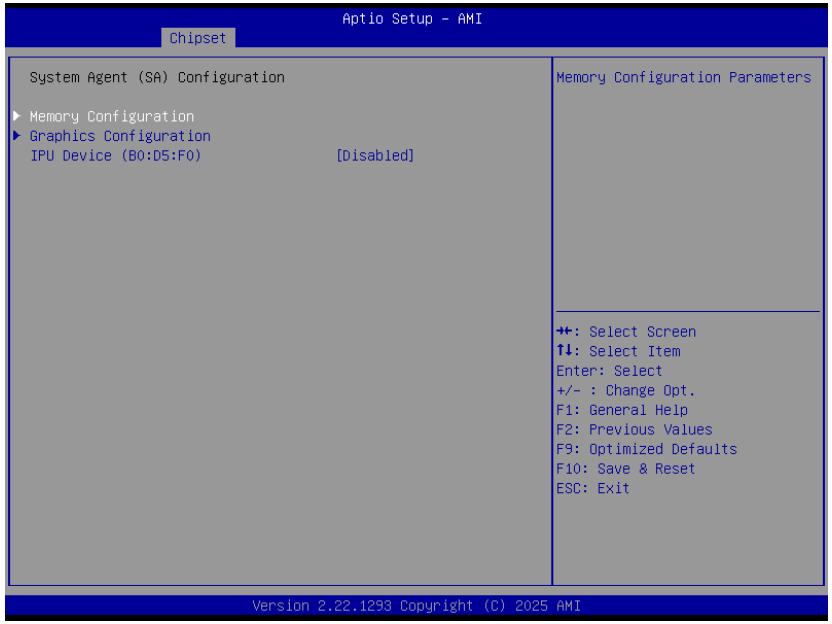
Set the wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.

Media detect count

Set the number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.

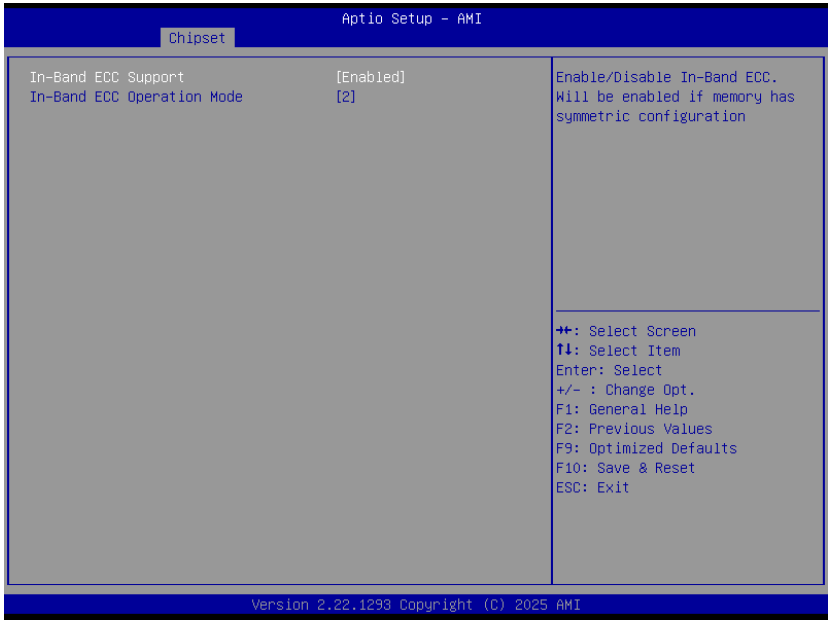
▶ Chipset

System Agent (SA) Configuration



▶ Chipset

System Agent (SA) Configuration ▶ Memory Configuration



In-Band ECC

Enable/Disable (Default) In-Band ECC

In-Band ECC Operation Mode

0: Functional Mode protects requests based on the address range,
1: Makes all requests non protected and ignore range checks,
2: Makes all requests protected and ignore range checks.

▶ Chipset

System Agent (SA) Configuration ▶ Graphics Configuration

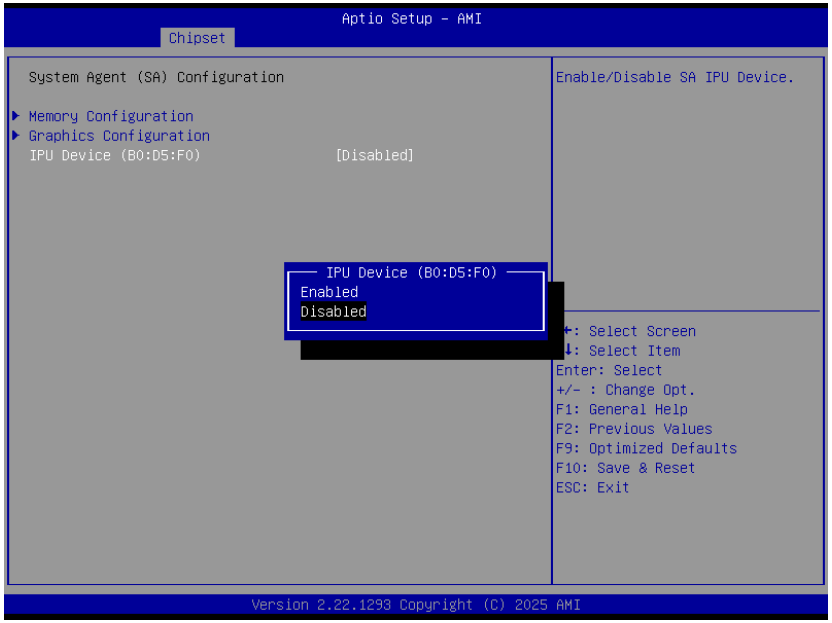
Primary Display

Select which of IGFX/PCI Graphics device to be the primary display.

Internal Graphics

Keep IGFX "Enabled" or "Disabled" based on the setup options, or select "Auto" for auto-detection.

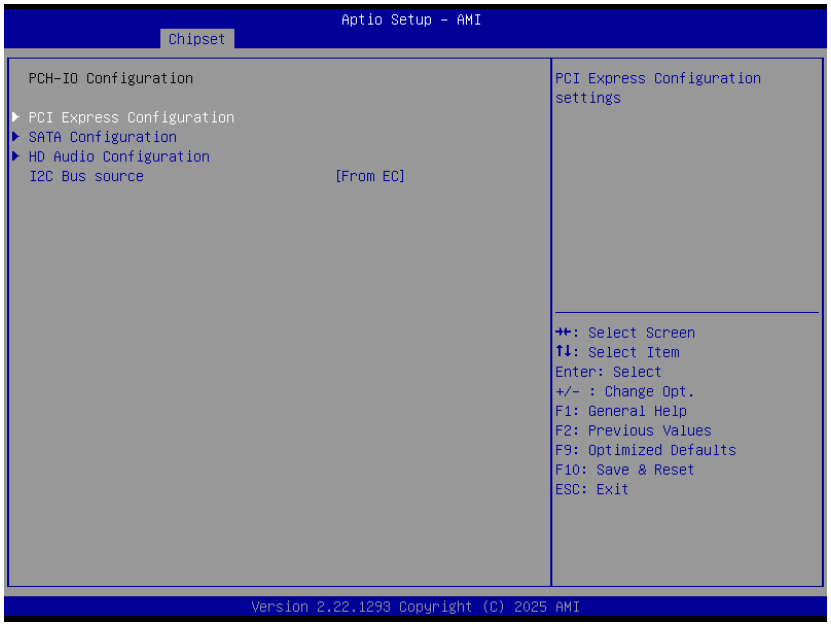
System Agent (SA) Configuration ▶ IPU Device



IPU Device (B0: D5 : F0)

Enable/Disable SA IPU Device

PCH-IO Configuration



Select one of the PCI Express channels and press enter to configure the following settings.

PCI Express Configuration

PCI Express Configuration Settings

SATA And RST Configuration

SATA Device Otpions Settings

HD Audio Configuration

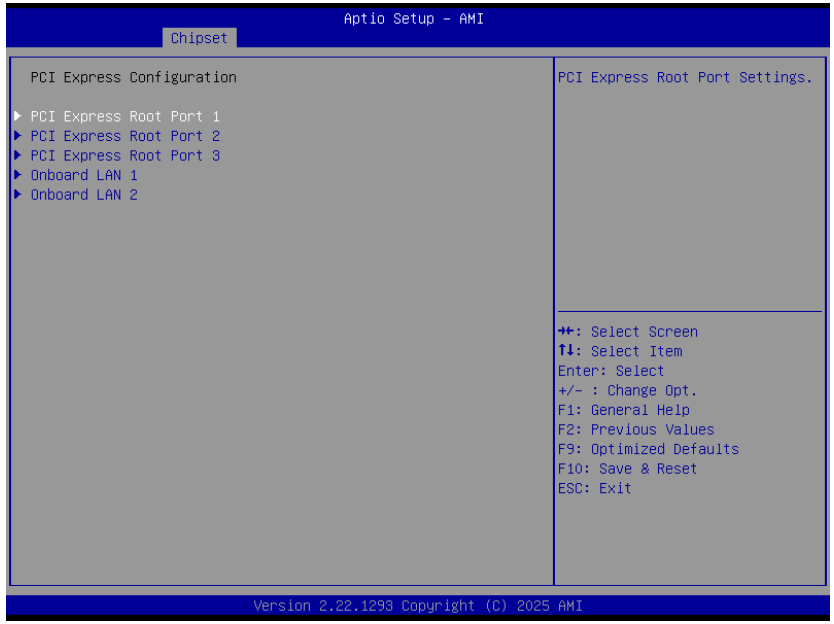
HD Audio Subsystem Configuration Settings

I2C Bus Source

Choose where I2C Bus comes from.

▶ Chipset

PCH-IO Configuration ▶ PCI Express Configuration



Select one of the PCI Express channels and press enter to configure the following settings.

PCIe Express Root Port 1,2,3

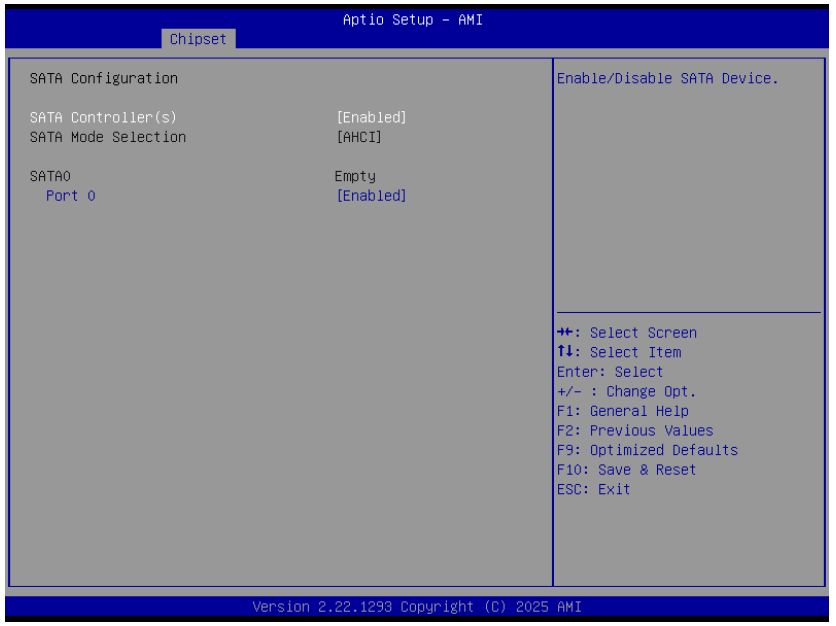
Control the PCI Express Root Port.

Onboard LAN1, 2

Control the PCI Express Root Port.

▶ Chipset

PCH-IO Configuration ▶ SATA Configuration



SATA Controller(s)

This field is used to enable or disable the Serial ATA controller.

SATA Mode Selection

The mode selection determines how the SATA controller(s) operates.

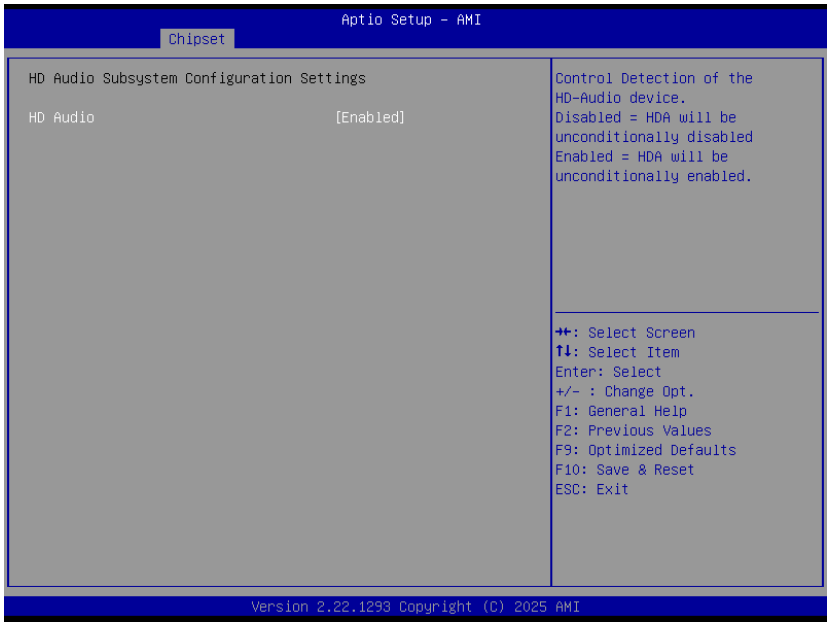
- **AHCI** This option allows the Serial ATA controller(s) to use AHCI (Advanced Host Controller Interface).

Ports

Enable or disable the Serial ATA ports.

▶ Chipset

PCH-IO Configuration ▶ HD Audio Configuration



HD Audio

Control the detection of the HD Audio device.

- **Disabled** HDA will be unconditionally disabled.
- **Enabled** HDA will be unconditionally enabled.

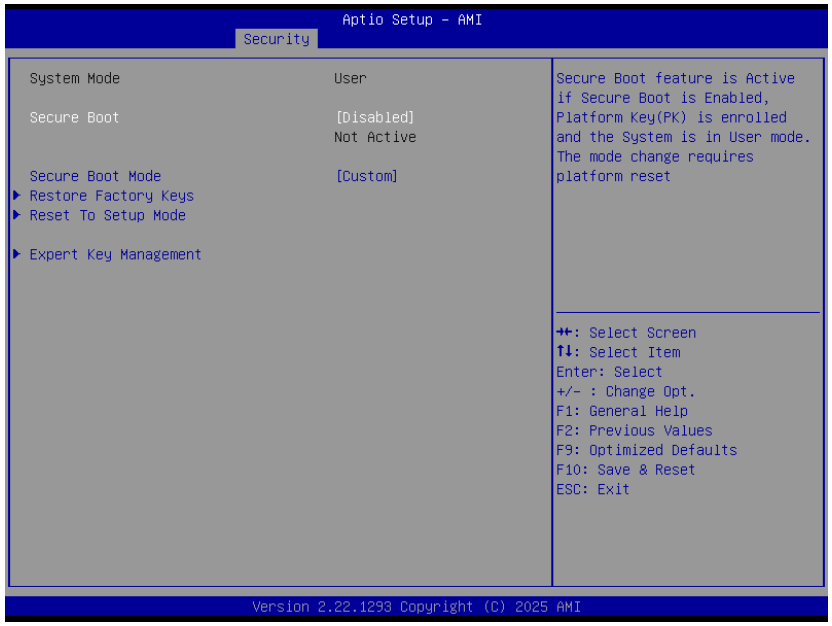
▶ Security

Administrator Password

Set the administrator password. To clear the password, input nothing and press enter when a new password is asked. Administrator Password will be required when entering the BIOS.

▶ Security

Secure Boot



Secure Boot

Secure Boot feature is Active if secure Boot is Enabled, Platform Key (PK) is enrolled and the system is in user mode. The mode change requires platform reset.

Secure Boot Mode

Select the secure boot mode — Standard or Custom. When set to Custom, the following fields will be configurable for the user to manually modify the key database.

Restore Factory Keys

Force system to User Mode. Load OEM-defined factory defaults of keys and databases onto the Secure Boot. Press Enter and a prompt will show up for you to confirm.

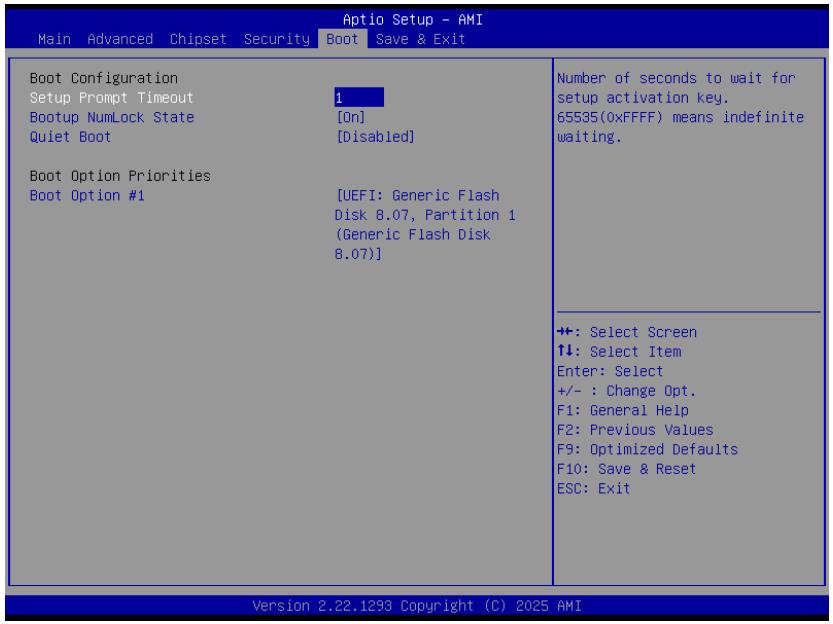
Reset To Setup Mode

Clear the database from the NVRAM, including all the keys and signatures installed in the Key Management menu. Press Enter and a prompt will show up for you to confirm.

Key Management

Enables expert users to modify Secure Boot Policy variables without full authentication.

▶ Boot



Setup Prompt Timeout

Set the number of seconds to wait for the setup activation key. 65535 (0xFFFF) denotes indefinite waiting.

Bootup NumLock State

Select the keyboard NumLock state: On or Off.

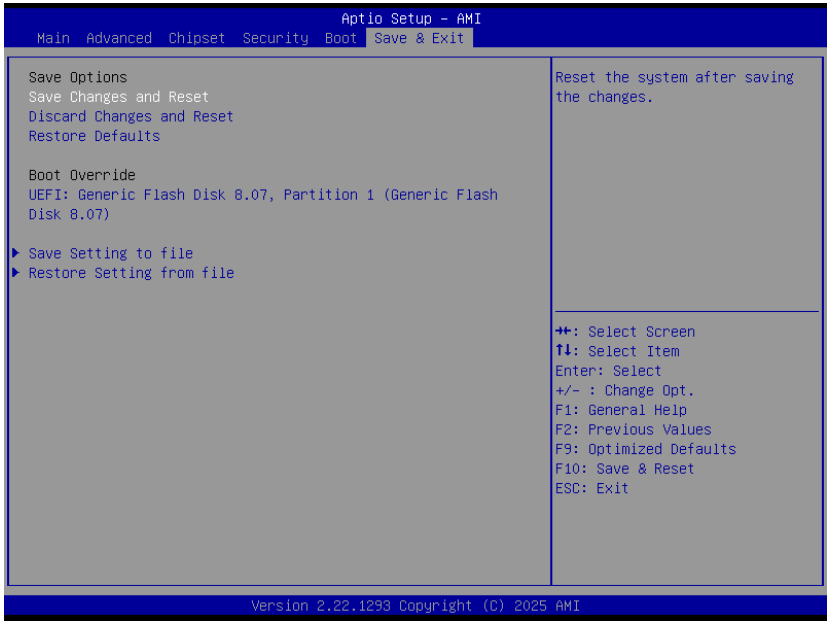
Quiet Boot

This section is used to enable or disable quiet boot option.

Boot Option Priorities

Rearrange the system boot order of available boot devices.

▶ Save & Exit



Save Changes and Reset

To save the changes, select this field and then press <Enter>. A dialog box will appear. Select Yes to reset the system after saving all changes made.

Discard Changes and Reset

To discard the changes, select this field and then press <Enter>. A dialog box will appear. Select Yes to reset the system setup without saving any changes.

Restore Defaults

To restore and load the optimized default values, select this field and then press <Enter>. A dialog box will appear. Select Yes to restore the default values of all the setup options.

Boot Override

Move the cursor to an available boot device and press Enter, and then the system will immediately boot from the selected boot device. The Boot Override function will only be effective for the current boot. The “Boot Option Priorities” configured in the Boot menu will not be changed.

► Save Setting to file

Select this option to save BIOS configuration settings to a USB flash device.

► Restore Setting from file

This field will appear only when a USB flash device is detected. Select this field to restore setting from the USB flash device.

▶ Updating the BIOS

To update the BIOS, you will need the new BIOS file and a flash utility. Please contact technical support or your sales representative for the files and specific instructions about how to update BIOS with the flash utility.

▶ Notice: BIOS SPI ROM

- 1. The Intel® Management Engine has already been integrated into this system board. Due to the safety concerns, the BIOS (SPI ROM) chip cannot be removed from this system board and used on another system board of the same model.
- 2. The BIOS (SPI ROM) on this system board must be the original equipment from the factory and cannot be used to replace one which has been utilized on other system boards.
- 3. If you do not follow the methods above, the Intel® Management Engine will not be updated and will cease to be effective.

Note:

a. You can take advantage of flash tools to update the default configuration of the BIOS (SPI ROM) to the latest version anytime.

b. When the BIOS IC needs to be replaced, you have to populate it properly onto the system board after the EEPROM programmer has been burned and follow the technical person's instructions to confirm that the MAC address should be burned or not.

c. After updating unique MAC Address from manufacturing, NVM will be protected immediately after power cycle.
Users cannot update NVM or MAC address.