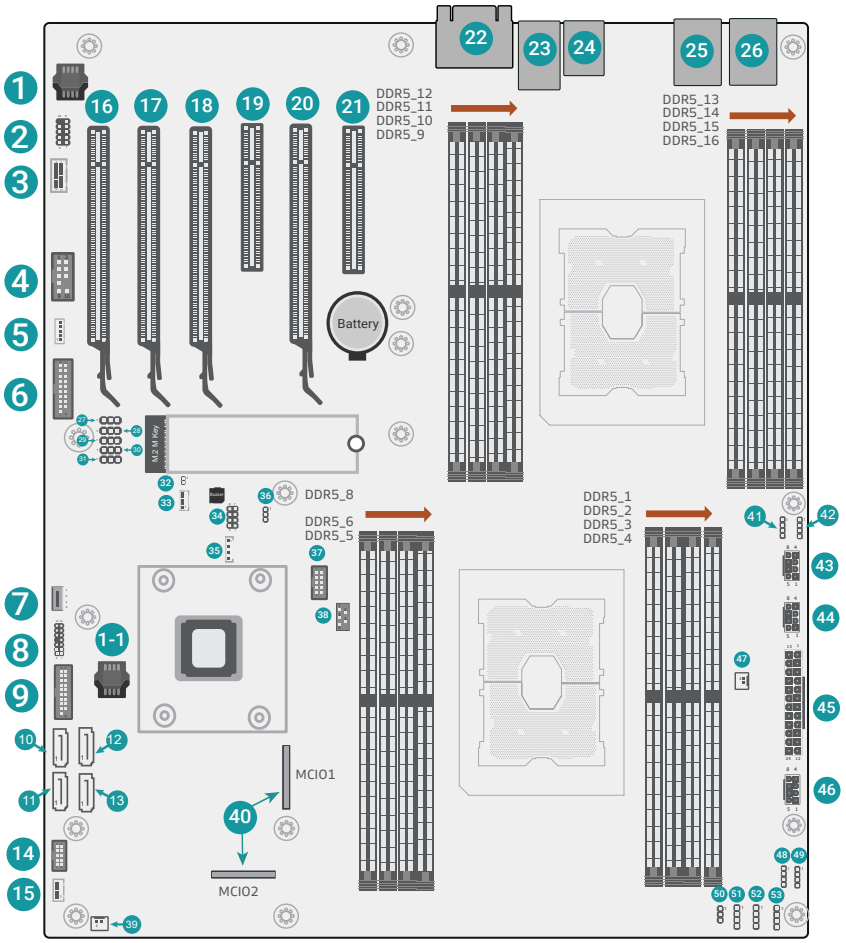
Board Layout

Top View



1. BMC Flash
1-1. BIOS Flash
2. BMC COM
3. Front Panel
4. COM2
5. DIO Power
6. DIO
7. USB 2.0_P9
8. ESPI Header
9. USB 3.0_P5/P6
10. SATA1
11. SATA0
12. SATA2
13. SATA3
14. Front Audio
15. LINE-IN Connector
16. PCIE6
17. PCIE5
18. PCIE4
19. PCIE3
20. PCIE2
21. PCIE1
22. ▲COM1
▼DP
23. ▲LAN3
▼LAN4
24. MGMT Port
25. ▲LAN2
▼USB2_3/4
USB3_3/4
26. ▲LAN1
▼USB2_1/2
USB3_1/2
27. DIO 4-7 Power Select
28. DIO 8-11 Power Select
29. DIO 12-15 Power Select
30. DIO 0-3 Power Select
31. DIO Power
32. Case Open
33. OOB I2C
34. CPLD JTAG
35. IntelR VROC Hardware Key
36. Clear CMOS Data
37. USB2.0_P10/P11
38. PMBUS (Power Management Bus)
39. RTC Battery
40. MCIO

41 CPU Fan2

42 CPU Fan1

43 12V Power Connector

44 12V Power Connector

45 ATX Power Connector

46 12V Power Connector

47 5VSB Header

48 System Fan2

49 System Fan1

50 CPU Power Update

51 System Fan5

52 System Fan4

53 System Fan3

Jumper Settings

36 Clear CMOS Data	JP15
Normal (default)	1-2 On
Clear RTC Registers	2-3 On

31 DIO Power	JP3
5VSB (default)	1-2 On
5V	2-3 On

30 DIO 0-3 Power Select	JP2
DIO PWR (default)	1-2 On
GND	2-3 On

27 DIO 4-7 Power Select	JP4
DIO PWR (default)	1-2 On
GND	2-3 On

28 DIO 8-11 Power Select	JP5
DIO PWR (default)	1-2 On
GND	2-3 On

29 DIO 12-15 Power Select	JP6
3V3 (default)	1-2 On
3V3DU	2-3 On

PIN Assignment

39 ▶ RTC Battery (J2)

Pin	Assignment
1	P3V_BAT
2	GND

32 ▶ Case Open (SOJ1)

Pin	Assignment
1	CASEOPEN#
2	GND

47 ▶ 5VSB Header (J7)

Pin	Assignment
1	5VSB_CONN
2	GND

50 ▶ CPU Power Update (J8000)

Pin	Assignment
1	DEBUG_UART_TX
2	DEBUG_UART_RX
3	GND

42 ▶ CPU Fan1 (J10)

Pin	Assignment
1	GND
2	+12V
3	FAN_TACH_IN_CPU0
4	FAN_PWM_OUT_CPU0

41 ▶ CPU Fan2 (J9)

Pin	Assignment
1	GND
2	+12V
3	FAN_TACH_IN_CPU1
4	FAN_PWM_OUT_CPU1

49 ▶ System Fan1 (J11)

Pin	Assignment
1	GND
2	+12V
3	FAN_TACH_IN_SYS1
4	FAN_PWM_OUT_SYS1

48 ▶ System Fan2 (J13)

Pin	Assignment
1	GND
2	+12V
3	FAN_TACH_IN_SYS2
4	FAN_PWM_OUT_SYS2

53 ▶ System Fan3 (J12)

Pin	Assignment
1	GND
2	12V
3	FAN_TACH_IN_SYS3
4	FAN_PWM_OUT_SYS3

52 ▶ System Fan4 (J14)

Pin	Assignment
1	GND
2	12V
3	FAN_TACH_IN_SYS4
4	FAN_PWM_OUT_SYS4

51 ▶ System Fan5 (J23)

Pin	Assignment
1	GND
2	12V
3	FAN_TACH_IN_SYS5
4	FAN_PWM_OUT_SYS5

5 ▶ DIO Power (J20)

Pin	Assignment
1	12V
2	GND
3	5VSB
4	5V

15 ▶ LINE-IN Connector (AUJ3)

Pin	Assignment
1	LINE1-R
2	LINE1-JD
3	LINE1-L
4	GND

7 ▶ USB 2.0_P9 (UBCN4)

Pin	Assignment
1	V5USB2_P9
2	USB2_VER_USB_P9_R_N
3	USB2_VER_USB_P9_R_P
4	GND

33 ▶ OOB I2C (J5)

Pin	Assignment
1	NC
2	GND
3	SIO_SCL
4	SIO_SDA
5	NC

11 ▶ SATA0 (J16)

Pin	Assignment
1	GND
2	SATA_PCH_TO_CON1_P
3	SATA_PCH_TO_CON1_N
4	GND
5	SATA_CON1_TO_PCH_C_N
6	SATA_CON1_TO_PCH_C_P
7	GND

10 ▶ SATA1 (J17)

Pin	Assignment
1	GND
2	SATA_PCH_TO_CON2_P
3	SATA_PCH_TO_CON2_N
4	GND
5	SATA_CON2_TO_PCH_C_N
6	SATA_CON2_TO_PCH_C_P
7	GND

12 ▶ SATA2 (J18)

Pin	Assignment
1	GND
2	SATA_PCH_TO_CON3_P
3	SATA_PCH_TO_CON3_N
4	GND
5	SATA_CON3_TO_PCH_C_N
6	SATA_CON3_TO_PCH_C_P
7	GND

13 ▶ SATA3 (J19)

Pin	Assignment
1	GND
2	SATA_PCH_TO_CON4_P
3	SATA_PCH_TO_CON4_N
4	GND
5	SATA_CON4_TO_PCH_C_N
6	SATA_CON4_TO_PCH_C_P
7	GND

38 ▶ PMBUS (Power Management Bus) (J22)

Pin	Assignment	Pin	Assignment
1	I2C_8_SCL	2	I2C_8_SDA
3	IRQ_SML1_PMBUS_BMC_ALERT_N	4	GND
5	---		

34 ▶ CPLD JTAG (J3)

Pin	Assignment	Pin	Assignment
1	3V3SB	2	JTAG_PLD_TDO
3	JTAG_PLD_TDI	4	JTAG_PLD_EN_N
5	JTAG_PLD_RST_N	6	JTAG_PLD_TMS
7	GND	8	JTAG_PLD_TCK

4 ▶ COM2 (TSJ1)

Pin	Assignment	Pin	Assignment
1	MDCD2-	2	MSIN2
3	MSO2	4	MDTR2-
5	GND	6	MDSR2-
7	MRTS2-	8	---
9	5V_12V_COM2	10	MCTS2-

2 ▶ BMC COM (J15)

Pin	Assignment	Pin	Assignment
1	MDCD1-	2	MRD1
3	MTD1	4	MDTR1-
5	GND	6	MDSR1-
7	MRTS1-	8	MCTS1-
9	MRI1-	10	----

14 ▶ Front Audio (AUJ2)

Pin	Assignment	Pin	Assignment
1	GND	2	MIC2-L_HEADER
3	NC	4	MIC2-R_HEADER
5	MIC2-JD	6	LINE2-R_HEADER
7	NC	8	AUD_GND_HEADER
9	LINE2-JD	10	LINE2-L_HEADER

37 ▶ USB2.0_P10/P11 (UBJ3)

Pin	Assignment	Pin	Assignment
1	V5USB2_P1011	2	V5USB2_P1011
3	USB2_HR_USB1_P10_R_N	4	USB2_HR_USB2_P11_R_N
5	USB2_HR_USB1_P10_R_P	6	USB2_HR_USB2_P11_R_P
7	GND	8	GND
9	GND	10	GND

3 ▶ Front Panel (J8)

Pin	Assignment	Pin	Assignment
1	NC	2	3V3SB
3	3V3	4	3V3SB
5	LED_PCH_SATA_HDD_N	6	FP_PWR_LED_N
7	GND	8	GND
9	FP_SYSRST_BTN_N	10	FP_PWR_BTN_IN_N
11	NC	12	---

8 ▶ eSPI Header (J6)

Pin	Assignment	Pin	Assignment
1	3V3SB	2	CLK_24M_66M_ESPI_P80
3	RST_ESPI_RESET_N	4	GND
5	ESPI_ALERT1_N_RCIN_N	6	GND
7	ESPI_IO0_LAD0	8	---
9	ESPI_IO0_LAD1	10	ESPI_CS0_N_LFRAME_N
11	ESPI_IO0_LAD2	12	3V3SB
13	ESPI_IO0_LAD3	14	3V3SB

43 44 46 ▶ 12V Power (CN1, CN2, CN6)

Pin	Assignment	Pin	Assignment
1	GND	5	12V
2	GND	6	12V
3	GND	7	12V
4	GND	8	12V

9 ▶ USB 3.0_P5/P6 (UBJ1)

Pin	Assignment	Pin	Assignment
1	V5USB3_P78	11	USB2_P8_R_P
2	USB3_P5_RX_R_N	12	USB2_P8_R_N
3	USB3_P5_RX_R_P	13	USB2_VER_USB_P9_R_P
4	GND	14	GND
5	USB3_P5_TX_C_R_N	15	USB3_P6_TX_C_R_P
6	USB3_P5_TX_C_R_P	16	USB3_P6_TX_C_R_N
7	GND	17	GND
8	USB2_P7_R_N	18	USB3_P6_RX_R_P
9	USB2_P7_R_P	19	USB3_P6_RX_R_N
10	NC	20	V5USB3_P78

6 ▶ DIO (J21)

Pin	Assignment	Pin	Assignment
1	GND	11	D_IOA8_C
2	GND	12	D_IOA9_C
3	D_IOA7_C	13	D_IOA10_C
4	D_IOA6_C	14	D_IOA11_C
5	D_IOA5_C	15	D_IOA12_C
6	D_IOA4_C	16	D_IOA13_C
7	D_IOA3_C	17	D_IOA14_C
8	D_IOA2_C	18	D_IOA15_C
9	D_IOA1_C	19	GND
10	D_IOA0_C	20	---

40 ▶ MCIO1 (MCCON1)

Pin	Assignment	Pin	Assignment
A1	GND	B1	GND
A2	CPU0_PE3_MCIO1_RX_DN<4>	B2	CPU0_PE3_MCIO1_TX_DN<4>
A3	CPU0_PE3_MCIO1_RX_DP<4>	B3	CPU0_PE3_MCIO1_TX_DP<4>
A4	GND	B4	GND
A5	CPU0_PE3_MCIO1_RX_DN<5>	B5	CPU0_PE3_MCIO1_TX_DN<5>
A6	CPU0_PE3_MCIO1_RX_DP<5>	B6	CPU0_PE3_MCIO1_TX_DP<5>
A7	GND	B7	GND
A8	CPU0_PEHP_ALERT_N	B8	CPU0_PE3_MCIO1_SCL
A9	CPU0_PE3_PWR_BRAKE_N	B9	CPU0_PE3_MCIO1_SDA
A10	GND	B10	GND
A11	CLK_100M_CPU0_PE3_MCIO1_NVME1_P	B11	CPLD_MCIO1_PERST_N
A12	CLK_100M_CPU0_PE3_MCIO1_NVME1_N	B12	CPU0_PE3_MCIO1_PRSNT_N
A13	GND	B13	GND
A14	CPU0_PE3_MCIO1_RX_DN<6>	B14	CPU0_PE3_MCIO1_TX_DN<6>
A15	CPU0_PE3_MCIO1_RX_DP<6>	B15	CPU0_PE3_MCIO1_TX_DP<6>
A16	GND	B16	GND
A17	CPU0_PE3_MCIO1_RX_DN<7>	B17	CPU0_PE3_MCIO1_TX_DN<7>
A18	CPU0_PE3_MCIO1_RX_DP<7>	B18	CPU0_PE3_MCIO1_TX_DP<7>
A19	GND	B19	GND
A20	CPU0_PE3_MCIO1_RX_DN<0>	B20	CPU0_PE3_MCIO1_TX_DN<0>
A21	CPU0_PE3_MCIO1_RX_DP<0>	B21	CPU0_PE3_MCIO1_TX_DP<0>
A22	GND	B22	GND
A23	CPU0_PE3_MCIO1_RX_DN<1>	B23	CPU0_PE3_MCIO1_TX_DN<1>
A24	CPU0_PE3_MCIO1_RX_DP<1>	B24	CPU0_PE3_MCIO1_TX_DP<1>
A25	GND	B25	GND
A26	CPU0_PEHP_ALERT_N	B26	CPU0_PE3_MCIO1_1_SCL
A27	SGPIO_SATA0_DATAOUT_R	B27	CPU0_PE3_MCIO1_1_SDA
A28	GND	B28	GND
A29	CLK_100M_CPU0_PE3_MCIO1_NVME0_P	B29	CPLD_MCIO1_1_PERST_N
A30	CLK_100M_CPU0_PE3_MCIO1_NVME0_N	B30	CPU0_PE3_MCIO1_1_PRSNT_N
A31	GND	B31	GND
A32	CPU0_PE3_MCIO1_RX_DN<2>	B32	CPU0_PE3_MCIO1_TX_DN<2>
A33	CPU0_PE3_MCIO1_RX_DP<2>	B33	CPU0_PE3_MCIO1_TX_DP<2>
A34	GND	B34	GND
A35	CPU0_PE3_MCIO1_RX_DN<3>	B35	CPU0_PE3_MCIO1_TX_DN<3>
A36	CPU0_PE3_MCIO1_RX_DP<3>	B36	CPU0_PE3_MCIO1_TX_DP<3>
A37	GND	B37	GND

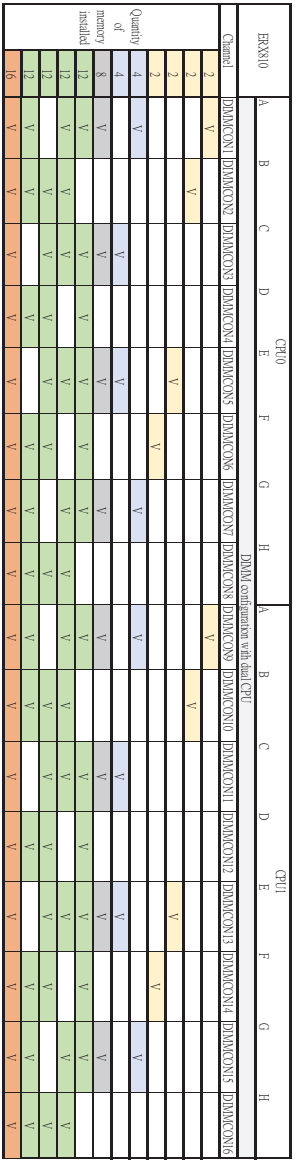
40 ▶ MCIO2 (MCCON2)

Pin	Assignment	Pin	Assignment
A1	GND	B1	GND
A2	CPU0_PE3_MCIO2_RX_DN<4>	B2	CPU0_PE3_MCIO2_TX_DN<4>
A3	CPU0_PE3_MCIO2_RX_DP<4>	B3	CPU0_PE3_MCIO2_TX_DP<4>
A4	GND	B4	GND
A5	CPU0_PE3_MCIO2_RX_DN<5>	B5	CPU0_PE3_MCIO2_TX_DN<5>
A6	CPU0_PE3_MCIO2_RX_DP<5>	B6	CPU0_PE3_MCIO2_TX_DP<5>
A7	GND	B7	GND
A8	CPU0_PEHP_ALERT_N	B8	CPU0_PE3_MCIO2_SCL
A9	SGPIO_SATA0_LOAD_R	B9	CPU0_PE3_MCIO2_SDA
A10	GND	B10	GND
A11	CLK_100M_CPU0_PE3_MCIO2_NVME1_P	B11	CPLD_MCIO2_PERST_N
A12	CLK_100M_CPU0_PE3_MCIO2_NVME1_N	B12	CPU0_PE3_MCIO2_PRSNT_N
A13	GND	B13	GND
A14	CPU0_PE3_MCIO2_RX_DN<6>	B14	CPU0_PE3_MCIO2_TX_DN<6>
A15	CPU0_PE3_MCIO2_RX_DP<6>	B15	CPU0_PE3_MCIO2_TX_DP<6>
A16	GND	B16	GND
A17	CPU0_PE3_MCIO2_RX_DN<7>	B17	CPU0_PE3_MCIO2_TX_DN<7>
A18	CPU0_PE3_MCIO2_RX_DP<7>	B18	CPU0_PE3_MCIO2_TX_DP<7>
A19	GND	B19	GND
A20	CPU0_PE3_MCIO2_RX_DN<0>	B20	CPU0_PE3_MCIO2_TX_DN<0>
A21	CPU0_PE3_MCIO2_RX_DP<0>	B21	CPU0_PE3_MCIO2_TX_DP<0>
A22	GND	B22	GND
A23	CPU0_PE3_MCIO2_RX_DN<1>	B23	CPU0_PE3_MCIO2_TX_DN<1>
A24	CPU0_PE3_MCIO2_RX_DP<1>	B24	CPU0_PE3_MCIO2_TX_DP<1>
A25	GND	B25	GND
A26	CPU0_PEHP_ALERT_N	B26	CPU0_PE3_MCIO2_1_SCL
A27	SGPIO_SATA0_CLOCK_R	B27	CPU0_PE3_MCIO2_1_SDA
A28	GND	B28	GND
A29	CLK_100M_CPU0_PE3_MCIO2_NVME0_P	B29	CPLD_MCIO2_1_PERST_N
A30	CLK_100M_CPU0_PE3_MCIO2_NVME0_N	B30	CPU0_PE3_MCIO2_1_PRSNT_N
A31	GND	B31	GND
A32	CPU0_PE3_MCIO2_RX_DN<2>	B32	CPU0_PE3_MCIO2_TX_DN<2>
A33	CPU0_PE3_MCIO2_RX_DP<2>	B33	CPU0_PE3_MCIO2_TX_DP<2>
A34	GND	B34	GND
A35	CPU0_PE3_MCIO2_RX_DN<3>	B35	CPU0_PE3_MCIO2_TX_DN<3>
A36	CPU0_PE3_MCIO2_RX_DP<3>	B36	CPU0_PE3_MCIO2_TX_DP<3>
A37	GND	B37	GND

45 ▶ ATX Power (CN3)

Pin	Assignment	Pin	Assignment
1	3V3	13	3V3
2	3V3	14	-12V
3	GND	15	GND
4	5V	16	ATX_PCTL_N
5	GND	17	GND
6	5V	18	GND
7	GND	19	GND
8	PWRGD_PS	20	NC
9	5VSB	21	5V
10	12V	22	5V
11	12V	23	5V
12	3V3	24	GND

DIMM Configuration with Dual CPU



ERX810	CPU0								CPU1								Quantity of memory installed	Channel
	A	B	C	D	E	F	G	H	A	B	C	D	E	F	G	H		
	DIMM configuration with dual CPU																	
	DIMMCON1	DIMMCON2	DIMMCON3	DIMMCON4	DIMMCON5	DIMMCON6	DIMMCON7	DIMMCON8	DIMMCON9	DIMMCON10	DIMMCON11	DIMMCON12	DIMMCON13	DIMMCON14	DIMMCON15	DIMMCON16		
2	V								V								2	2
2		V								V							2	2
2					V								V				2	2
2						V								V			2	2
4	V		V				V		V		V				V		4	4
8	V		V	V	V	V	V	V	V	V	V	V	V	V	V	V	8	12
4	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	4	12
8	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	8	12
4	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	4	12
8	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	8	16

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