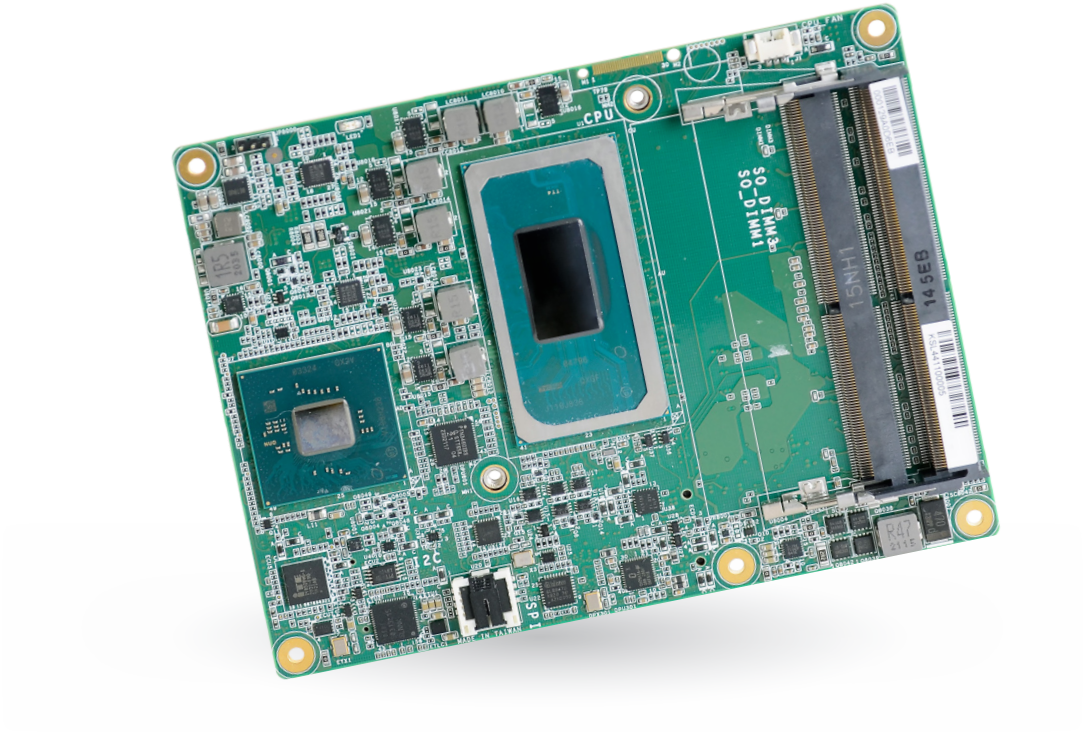
DFI



TGH960

COM Express Basic Module
User's Manual

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Trademarks

COM Express Specification Reference

PICMG® COM Express® Module Base Specification.
http://www.picmg.org/

FCC and DOC Statement on Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio TV technician for help.

Notice:

- The changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.
- Shielded interface cables must be used in order to comply with the emission limits.

Table of Contents

About this Manual

This manual can be downloaded from the website.

The manual is subject to change and update without notice, and may be based on editions that do not resemble your actual products. Please visit our website or contact our sales representatives for the latest editions.

Warranty

- Warranty does not cover damages or failures that occur from misuse of the product, inability to use the product, unauthorized replacement or alteration of components and product specifications.
- The warranty is void if the product has been subjected to physical abuse, improper installation, modification, accidents or unauthorized repair of the product.
- Unless otherwise instructed in this user's manual, the user may not, under any circumstances, attempt to perform service, adjustments or repairs on the product, whether in or out of warranty. It must be returned to the purchase point, factory or authorized service agency for all such work.
- We will not be liable for any indirect, special, incidental or consequential damages to the product that has been modified or altered.

Static Electricity Precautions

It is quite easy to inadvertently damage your PC, system board, components or devices even before installing them in your system unit. Static electrical discharge can damage computer components without causing any signs of physical damage. You must take extra care in handling them to ensure against electrostatic build-up.

- To prevent electrostatic build-up, leave the system board in its anti-static bag until you are ready to install it.
- Wear an antistatic wrist strap.
- Do all preparation work on a static-free surface.
- Hold the device only by its edges. Be careful not to touch any of the components, contacts or connections.
- Avoid touching the pins or contacts on all modules and connectors. Hold modules or connectors by their ends.

Important:
Electrostatic discharge (ESD) can damage your processor, disk drive and other components. Perform the upgrade instruction procedures described at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

Safety Measures

- To avoid damage to the system, use the correct AC input voltage range.
- To reduce the risk of electric shock, unplug the power cord before removing the system chassis cover for installation or servicing. After installation or servicing, cover the system chassis before plugging the power cord.

About the Package

The package contains the following items. If any of these items are missing or damaged, please contact your dealer or sales representative for assistance.

The accessories in the package may not come similar to the information listed below. This may differ in accordance with the sales region or models in which it was sold. For more information about the standard package in your region, please contact your dealer or sales representative.

- One TGH960-RM590E/QM580E/HM570E board

Optional Items

The board and accessories in the package may not come similar to the information listed above. This may differ in accordance with the sales region or models in which it was sold. For more information about the standard package in your region, please contact your dealer or sales representative.

Before Using the System Board

Before using the system board, prepare basic system components.
If you are installing the system board in a new system, you will need at least the following internal components.

- Storage devices such as hard disk drive, etc.

You will also need external system peripherals you intend to use which will normally include at least a keyboard, a mouse and a video display monitor.

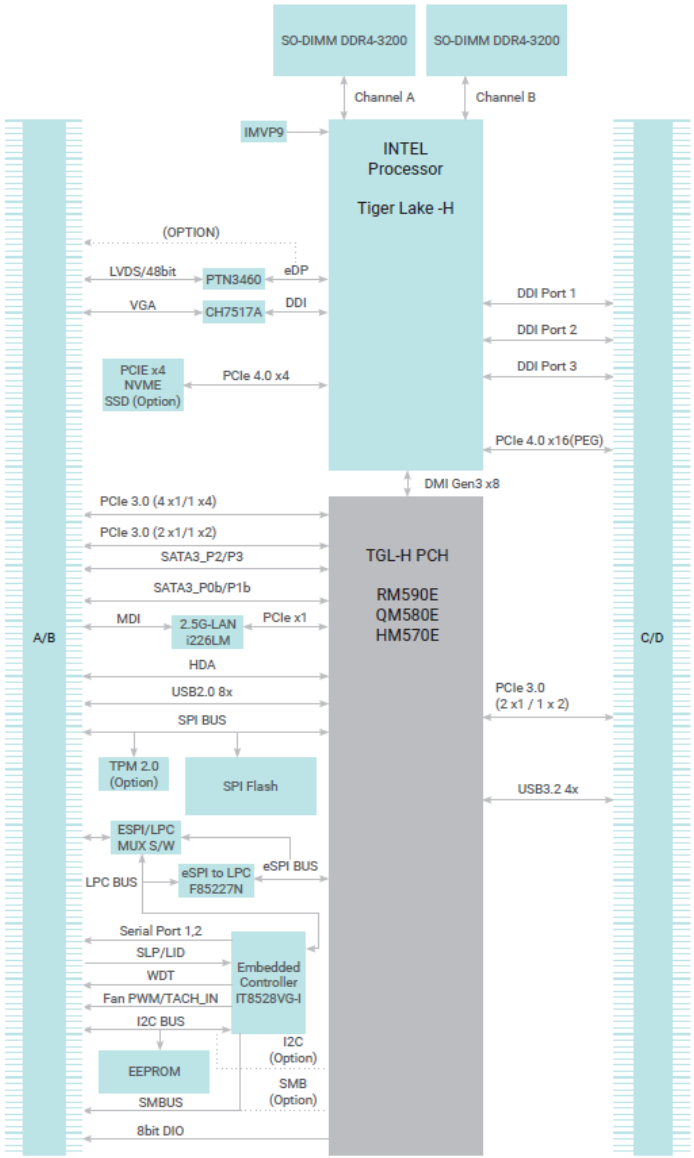
Chapter 1 - Introduction

▶ Specification

SYSTEM	Processor	11th Gen Intel® Core™ Processors, BGA 1787 Intel® Xeon® W-11865MRE, 8 Cores, 24M Cache, 2.6GHz (4.7GHz), 45W (RM590E) Intel® Xeon® W-11865MLE, 8 Cores, 24M Cache, 1.5GHz (4.5GHz), 25W (RM590E) Intel® Core™ i7-11850HE, 8 Cores, 24M Cache, 2.6GHz (4.7GHz), 45W (RM590E/QM580E) Intel® Xeon® W-11555MRE, 6 Cores, 12M Cache, 2.6GHz (4.5GHz), 45W (RM590E) Intel® Xeon® W-11555MLE, 6 Cores, 12M Cache, 1.9GHz (4.4Hz), 25W (RM590E) Intel® Core™ i5-11500HE, 6 Cores, 12M Cache, 2.6GHz (4.5GHz), 45W (RM590E/QM580E) Intel® Xeon® W-11155MRE, 4 Cores, 8M Cache, 2.4GHz (4.4GHz), 45W (RM590E) Intel® Xeon® W-11155MLE, 4 Cores, 8M Cache, 1.8GHz (3.1GHz), 25W (RM590E) Intel® Core™ i3-11100HE, 4 Cores, 8M Cache, 2.4GHz (4.4GHz), 45W (RM590E/QM580E/HM570E) Intel® Celeron® 6600HE, 2 Cores, 8M Cache, 2.6GHz, 35W (RM590E/QM580E/HM570E)
	Chipset	Intel® RM590E/QM580E/HM570E Chipset
	Memory	3pcs DDR4 3200MHz SO-DIMM up to 96GB, 4th DIMM by request. Dual Channel DDR4 3200MHz ECC support (by request)
	BIOS	AMI SPI 256Mbit
GRAPHICS	Controller	Intel® UHD Graphics for 11th Gen Intel® Processors
	Feature	OpenGL 4.5, DirectX 12, OpenCL 2.1 HW Decode: MPEG2, WMV9, AVC/H264, JPEG/MJPEG, HEVC/H265, VP9, AV1 HW Encode: AVC/H264, JPEG, HEVC/H265, VP9
	Display	1 x VGA 1 x LVDS/eDP (eDP available upon request) 3 x DDI (DP/DP++)
	Multi-displays	VGA + LVDS + 2 DDI or VGA + 3 DDI or LVDS + 3 DDI
EXPANSION	Interface	1 x PCIe x16 (Gen 4) 8 x PCIe x1 (Gen 3) 1 x LPC 1 x I2C 1 x SMBus 2 x UART (TX/RX)
AUDIO	Interface	HD Audio
ETHERNET	Phy	1 x Intel® i226 series (10/100/1000Mbps/2.5G)
I/O	USB	4 x USB 3.2 Gen2 8 x USB 2.0
	SATA	4 x SATA 3.0 (up to 6Gb/s) Support RAID 0/1
	DIO	1 x 8-bit DIO (Default 4 inputs and 4 outputs)

WATCHDOG TIMER	Output & Interval	System Reset, Programmable via Software from 1 to 255 Seconds
STORAGE (Optional)	NVMe SSD	PCIe x4 Gen4, 64GB~1TB SSD and 2nd DDR4 SO-DIMM(DIMM2) is alternative function
SECURITY	TPM	TPM2.0 (Available Upon Request)
Power	Type	8.5V~20V, 5VSB, VCC_RTC (ATX mode) 8.5V~20V, VCC_RTC (AT mode)
	Consumption	Typical: 19V @ 2.66A (50.54 Watt) Max.: 19V @ 6.72A (127.68 Watt)
OS SUPPORT	Microsoft	Windows 10 IoT Enterprise 64-bit
	Linux	Ubuntu 20.04
ENVIRONMENT	Temperature	Operating: 0 to 60°C, -40 to 70°C Storage: -40 to 85°C
	Humidity	Operating: 5 to 90% RH Storage: 5 to 90% RH
	MTBF	TBD
MECHANICAL	Dimensions	COM Express® Basic 95mm (3.74") x 125mm (4.9")
	Compliance	PICMG COM Express® R3.0, Type 6

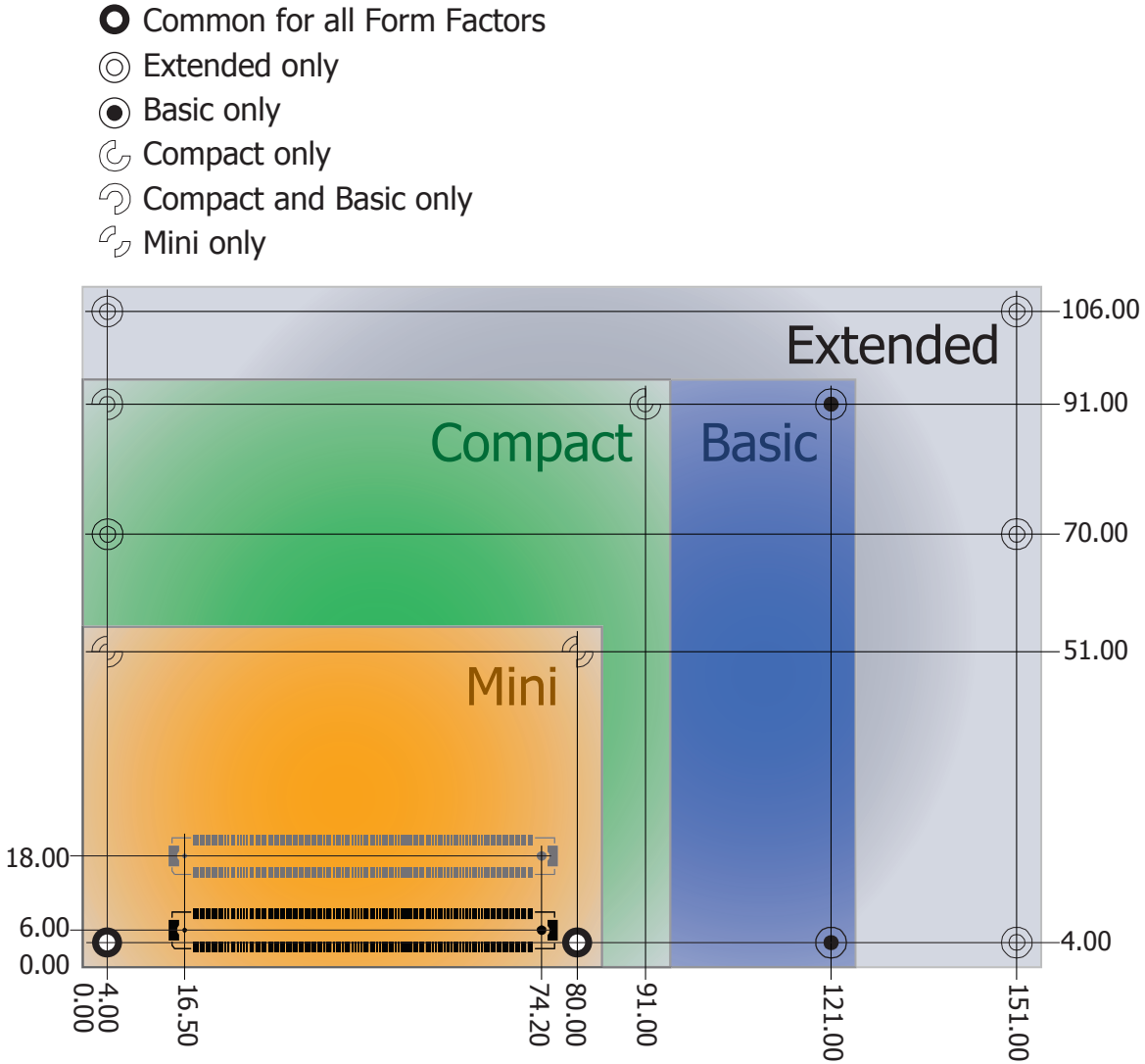
▶ Block Diagram



Chapter 2 - Concept

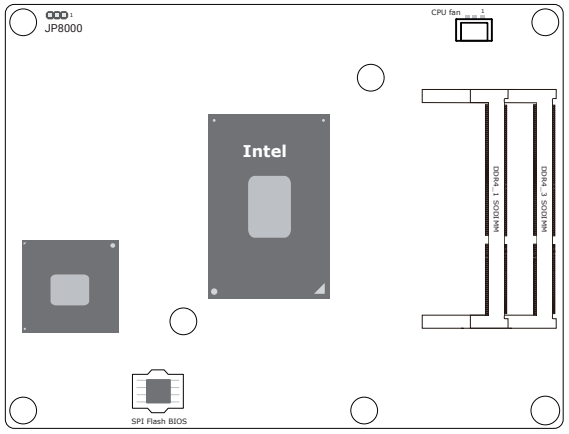
▶ COM Express Module Standards

The figure below shows the dimensions of the different types of COM Express modules.
TGH960 is a COM Express Basic. The dimension is 95mm x 125mm.

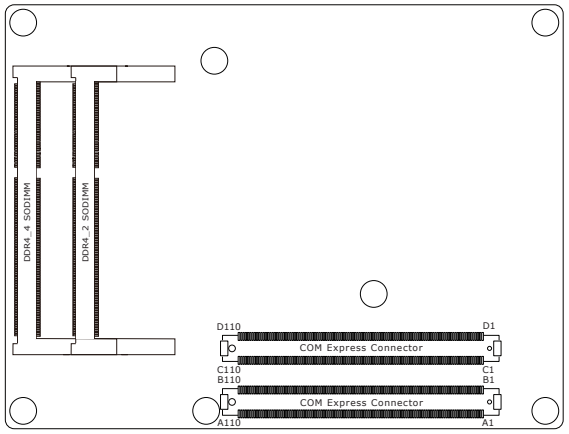


Chapter 3 - Hardware Installation

▶ Board Layout



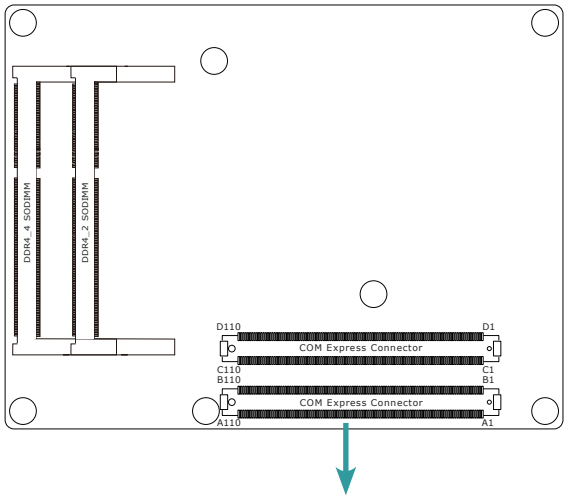
TOP VIEW



BOTTOM VIEW

▶ Connector

The COM Express connector is used to interface the TGH960 COM Express board to a carrier board. Connect the COM Express connector (located on the solder side of the board) to the COM Express connector on the carrier board.Refer to the following pages for the pin functions of the connector.



▶ COM Express Connector

Row A			Row B
A1	GND (FIXED)	B1	GND (FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#
A3	GBE0_MDI3+	B3	LPC_FRAME#/ESPI_CS0#
A4	Note*GBE0_LINK100#	B4	LPC_AD0/ ESPI_IO_0
A5	Note**GBE0_LINK100#	B5	LPC_AD1/ESPI_IO_1
A6	GBE0_MDI2-	B6	LPC_AD2/ESPI_IO_2
A7	GBE0_MDI2+	B7	LPC_AD3/ESPI_IO_3
A8	GBE0_LINK#	B8	LPC_DRQ0#(NA)/ESPI_ALERT0#
A9	GBE0_MDI1-	B9	LPC_DRQ1#(NA)/ESPI_ALERT1#
A10	GBE0_MDI1+	B10	LPC_CLK/ESPI_CK
A11	GND (FIXED)	B11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#
A13	GBE0_MDI0+	B13	SMB_CK
A14	GBE0_CTREF	B14	SMB_DAT
A15	SUS_S3#	B15	SMB_ALERT#
A16	SATA0_TX+	B16	SATA1_TX+
A17	SATA0_TX-	B17	SATA1_TX-
A18	SUS_S4#	B18	SUS_STAT#/ESPI_RESET#
A19	SATA0_RX+	B19	SATA1_RX+
A20	SATA0_RX-	B20	SATA1_RX-
A21	GND (FIXED)	B21	GND (FIXED)
A22	SATA2_TX+	B22	SATA3_TX+
A23	SATA2_TX-	B23	SATA3_TX-
A24	SUS_S5#	B24	PWR_OK
A25	SATA2_RX+	B25	SATA3_RX+
A26	SATA2_RX-	SATA2_RX-	SATA3_RX-
A27	BATLOW#	BATLOW#	WDT

Note:
1. *GBE_LED_100# is active during a 1Gb connection.
2. **GBE_LED_1000# is active during a 2.5Gb connection.

Row A			Row B
A28	(S)ATA_ACT#	B28	NA
A29	AC/HDA_SYNC	B29	HDA_SDI1
A30	AC/HDA _RST#	B30	HDA _SDIN0
A31	GND (FIXED)	B31	GND (FIXED)
A32	HDA _BITCLK	B32	SPKR
A33	HDA _SDOUT	B33	I2C_CK
A34	BIOS_DIS0#/ESPI_SAFS	B34	I2C_DAT
A35	THRMTRIP#	B35	THRM#
A36	USB6-	B36	USB7-
A37	USB6+	B37	USB7+
A38	USB_6_7_OC#	B38	USB_4_5_O#
A39	USB4-	B39	USB5-
A40	USB4+	B40	USB5+
A41	GND (FIXED)	B41	GND (FIXED)
A42	USB2-	B42	USB3-
A43	USB2+	B43	USB3+
A44	USB_2_3_OC#	B44	USB_0_1_O#
A45	USB0-	B45	USB1-
A46	USB0+	B46	USB1+
A47	VCC_RTC	B47	ESPI_EN#
A48	RSVD	B48	USB0_HOST_PRSNT(NA)
A49	GBE0_SDP	B49	SYS_RESET#
A50	LPC_SERIRQ/ ESPI_CS1#	B50	CB_RESET#
A51	GND (FIXED)	B51	GND (FIXED)
A52	PCIE_TX5+	B52	PCIE_TX5+
A53	PCIE_TX5-	B53	PCIE_TX5-
A54	GPI0	B54	GPO1
A55	PCIE_TX4+	B55	PCIE_RX4+

Row A		Row B	
A56	PCIE_TX4-	B56	PCIE_RX4-
A57	GND	B57	GPO2
A58	PCIE_TX3+	B58	PCIE_RX3+
A59	PCIE_TX3-	B59	PCIE_RX3-
A60	GND (FIXED)	B60	GND (FIXED)
A61	PCIE_TX2+	B61	PCIE_RX2+
A62	PCIE_TX2-	B62	PCIE_RX2-
A63	GPI1	B63	GPO3
A64	PCIE_TX1+	B64	PCIE_RX1+
A65	PCIE_TX1-	B65	PCIE_RX1-
A66	GND	B66	WAKE0#
A67	GPI2	B67	WAKE1#
A68	PCIE_TX0+	B68	PCIE_RX0+
A69	PCIE_TX0-	B69	PCIE_RX0-
A70	GND(FIXED)	B70	GND (FIXED)
A71	LVDS_A0+/ eDP_TX2+	B71	LVDS_B0+
A72	LVDS_A0-/ eDP_TX2-	B72	LVDS_B0-
A73	LVDS_A1+/ eDP_TX1+	B73	LVDS_B1+
A74	LVDS_A1-/ eDP_TX1-	B74	LVDS_B1-
A75	LVDS_A2+/ eDP_TX0+	B75	LVDS_B2+
A76	LVDS_A2-/ eDP_TX0-	B76	LVDS_B2-
A77	LVDS_VDD_EN /eDP_VDD_EN	B77	LVDS_B3+
A78	LVDS_A3+	B78	LVDS_B3-
A79	LVDS_A3-	B79	LVDS_BKLT_EN /eDP_BKLT_EN
A80	GND (FIXED)	B80	GND (FIXED)
A81	LVDS_A_CK+/eDP_TX3+	B81	LVDS_B_CK+
A82	LVDS_A_CK-/eDP_TX3-	B82	LVDS_B_CK-

Row A		Row B	
A83	LVDS_I2C_CK/eDP_AUX+	B83	LVDS_BKLT_CTRL/eDP_BKLT_CTRL
A84	LVDS_I2C_DAT /eDP_AUX-	B84	VCC_5V_SBY
A85	GPI3	B85	VCC_5V_SBY
A86	RSVD	B86	VCC_5V_SBY
A87	RSVD/ePD_HPD	B87	VCC_5V_SBY
A88	PCIE0_CK_REF+	B88	BIOS_DIS1#
A89	PCIE0_CK_REF-	B89	VGA_RED
A90	GND (FIXED)	B90	GND (FIXED)
A91	SPI_POWER	B91	VGA_GRN
A92	SPI_MISO	B92	VGA_BLU
A93	GPO0	B93	VGA_HSYNC
A94	SPI_CLK	B94	VGA_VSYNC
A95	SPI_MOSI	B95	VGA_I2C_CK
A96	TPM_PP	B96	VGA_I2C_DAT
A97	Type10# (NC)	B97	SPI_CS#
A98	SER0_TX	B98	RSVD
A99	SER0_RX	B99	RSVD
A100	GND (FIXED)	B100	GND (FIXED)
A101	SER1_TX	B101	FAN_PWMOUT
A102	SER1_RX	B102	FAN_TACHIN
A103	LID#	B103	SLEEP#
A104	VCC_8.5V~ 20V	B104	VCC_8.5V~ 20V
A105	VCC_8.5V~ 20V	B105	VCC_8.5V~ 20V
A106	VCC_8.5V~ 20V	B106	VCC_8.5V~ 20V
A107	VCC_8.5V~ 20V	B107	VCC_8.5V~ 20V
A108	VCC_8.5V~ 20V	B108	VCC_8.5V~ 20V
A109	VCC_8.5V~ 20V	B109	VCC_8.5V~ 20V
A110	GND (FIXED)	B110	GND (FIXED)

Row C		Row D	
C1	GND (FIXED)	D1	GND (FIXED)
C2	GND	D2	GND
C3	USB_SSRX0-	D3	USB_SSTX0-
C4	USB_SSRX0+	D4	USB_SSTX0+
C5	GND	D5	GND
C6	USB_SSRX1-	D6	USB_SSTX1-
C7	USB_SSRX1+	D7	USB_SSTX1+
C8	GND	D8	GND
C9	USB_SSRX2-	D9	USB_SSTX2-
C10	USB_SSRX2+	D10	USB_SSTX2+
C11	GND (FIXED)	D11	GND (FIXED)
C12	USB_SSRX3-	D12	USB_SSTX3-
C13	USB_SSRX3+	D13	USB_SSTX3+
C14	GND	D14	GND
C15	DDI1_PAIR6+ (NA)	D15	DDI1_CTRLCLK_AUX+
C16	DDI1_PAIR6- (NA)	D16	DDI1_CTRLDATA_AUX-
C17	RSVD	D17	RSVD
C18	RSVD	D18	RSVD
C19	PCIE_RX6+	D19	PCIE_TX6+
C20	PCIE_RX6-	D20	PCIE_TX6-
C21	GND (FIXED)	D21	GND (FIXED)
C22	PCIE_RX7+	D22	PCIE_TX7+
C23	PCIE_RX7-	D23	PCIE_TX7-
C24	DDI1_HPD	D24	RSVD
C25	DDI1_PAIR4+ (NA)	D25	RSVD
C26	DDI1_PAIR4- (NA)	D26	DDI1_PAIR0+
C27	RSVD	D27	DDI1_PAIR0-

Row C		Row D	
C28	RSVD	D28	RSVD
C29	DDI1_PAIR5+ (NA)	D29	DDI1_PAIR1+
C30	DDI1_PAIR5- (NA)	D30	DDI1_PAIR1-
C31	GND (FIXED)	D31	GND (FIXED)
C32	DDI2_CTRLDATA_ AUX+	D32	DDI1_PAIR2+
C33	DDI2_CTRLDATA_AUX-	D33	DDI1_PAIR2-
C34	DDI2_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL
C35	RSVD	D35	RSVD
C36	DDI3_CTRLCLK_AUX+	D36	DDI1_PAIR3+
C37	DDI3_CTRLDATA_AUX-	D37	DDI1_PAIR3-
C38	DDI2_DDC_AUX_SEL	D38	RSVD
C39	DDI3_PAIR0+	D39	DDI2_PAIR0+
C40	DDI3_PAIR0-	D40	DDI2_PAIR0-
C41	GND (FIXED)	D41	GND (FIXED)
C42	DDI3_PAIR1+	D42	DDI2_PAIR1+
C43	DDI3_PAIR1-	D43	DDI2_PAIR1-
C44	DDI3_HPD	D44	DDI2_HPD
C45	RSVD	D45	RSVD
C46	DDI3_PAIR2+	D46	DDI2_PAIR2+
C47	DDI3_PAIR2-	D47	DDI2_PAIR2-
C48	RSVD	D48	RSVD
C49	DDI3_PAIR3+	D49	DDI2_PAIR3+
C50	DDI3_PAIR3-	D50	DDI2_PAIR3-
C51	GND (FIXED)	D51	GND (FIXED)
C52	PEG_RX0+	D52	PEG_TX0+
C53	PEG_RX0-	D53	PEG_TX0-
C54	TYPE0# (NC)	D54	PEG_LANE_RV#
C55	PEG_RX1+	D55	PEG_TX1+

Row C		Row D	
C56	PEG_RX1-	D56	PEG_TX1-
C57	TYPE1# (NC)	D57	TYPE2# (GND)
C58	PEG_RX2+	D58	PEG_TX2+
C59	PEG_RX2-	D59	PEG_TX2-
C60	GND (FIXED)	D60	GND (FIXED)
C61	PEG_RX3+	D61	PEG_TX3+
C62	PEG_RX3-	D62	PEG_TX3-
C63	RSVD	D63	RSVD
C64	RSVD	D64	RSVD
C65	PEG_RX4+	D65	PEG_TX4+
C66	PEG_RX4-	D66	PEG_TX4-
C67	RAPID_SHUTDOWN	D67	GND
C68	PEG_RX5+	D68	PEG_TX5+
C69	PEG_RX5-	D69	PEG_TX5-
C70	GND (FIXED)	D70	GND (FIXED)
C71	PEG_RX6+	D71	PEG_TX6+
C72	PEG_RX6-	D72	PEG_TX6-
C73	GND	D73	GND
C74	PEG_RX7+	D74	PEG_TX7+
C75	PEG_RX7-	D75	PEG_TX7-
C76	GND	D76	GND
C77	RSVD	D77	RSVD
C78	PEG_RX8+	D78	PEG_TX8+
C79	PEG_RX8-	D79	PEG_TX8-
C80	GND (FIXED)	D80	GND (FIXED)
C81	PEG_RX9+	D81	PEG_TX9+
C82	PEG_RX9-	D82	PEG_TX9-

Row C		Row D	
C83	RSVD	D83	RSVD
C84	GND	D84	GND
C85	PEG_RX10+	D85	PEG_TX10+
C86	PEG_RX10-	D86	PEG_TX10-
C87	GND	D87	GND
C88	PEG_RX11+	D88	PEG_TX11+
C89	PEG_RX11-	D89	PEG_TX11-
C90	GND (FIXED)	D90	GND (FIXED)
C91	PEG_RX12+	D91	PEG_TX12+
C92	PEG_RX12-	D92	PEG_TX12-
C93	GND	D93	GND
C94	PEG_RX13+	D94	PEG_TX13+
C95	PEG_RX13-	D95	PEG_TX13-
C96	GND	D96	GND
C97	RSVD	D97	RSVD
C98	PEG_RX14+	D98	PEG_TX14+
C99	PEG_RX14-	D99	PEG_TX14-
C100	GND (FIXED)	D100	GND (FIXED)
C101	PEG_RX15+	D101	PEG_TX15+
C102	PEG_RX15-	D102	PEG_TX15-
C103	GND	D103	GND
C104	VCC_8.5V~ 20V	D104	VCC_8.5V~ 20V
C105	VCC_8.5V~ 20V	D105	VCC_8.5V~ 20V
C106	VCC_8.5V~ 20V	D106	VCC_8.5V~ 20V
C107	VCC_8.5V~ 20V	D107	VCC_8.5V~ 20V
C108	VCC_8.5V~ 20V	D108	VCC_8.5V~ 20V
C109	VCC_8.5V~ 20V	D109	VCC_8.5V~ 20V
C110	GND (FIXED)	D110	GND (FIXED)

▶ COM Express Connector Signal Description

Pin Types
I : Input to the Module
O : Output from the Module
I/O : Bi-directional input / output signal
OD : Open drain output
RSVD : pins are reserved for future use and should be no connect. Do not tie the RSVD pins together.

HDA Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGH960 PU/PD	Carrier Board	Description
HAD_RST#	A30	O CMOS	3.3V Suspend/3.3V	series 33Ω resistor/PD 100KΩ	Connect to CODEC pin 11 RESET#	Reset output to CODEC, active low.
HDA_SYNC	A29	O CMOS	3.3V/3.3V	series 33Ω resistor/PD 100KΩ	Connect to CODEC pin 10 SYNC	Sample-synchronization signal to the CODEC(s).
HDA_BITCLK	A32	I/O CMOS	3.3V/3.3V	series 33Ω resistor/PD 100KΩ	Connect to CODEC pin 6 BIT_CLK	Serial data clock generated by the external CODEC(s).
HDA_SDOUT	A33	O CMOS	3.3V/3.3V	series 33Ω resistor/PD 10KΩ	Connect to CODEC pin 5 SDATA_OUT	Serial TDM data output to the CODEC.
HDA_SDIN2	B28	I/O CMOS	3.3V Suspend/3.3V	HDA_SDIN2 NA	NC	Serial TDM data inputs from up to 3 CODECs.
HDA_SDIN1	B29	I/O CMOS	3.3V Suspend/3.3V		Connect 33 Ω in series to CODEC1 pin 8 SDATA_IN	
HDA_SDIN0	B30	I/O CMOS	3.3V Suspend/3.3V		Connect 33 Ω in series to CODEC0 pin 8 SDATA_IN	

Gigabit Ethernet Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGH960 PU/PD	Carrier Board	Description
GBE0_MDI0+	A13	I/O Analog	3.3V max Suspend	i225 2.5GbE signal	Connect to Magnetics Module MDI0+/-	Gigabit Ethernet Controller 0: Media Dependent Interface DifferentialPairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes or in 2.5, 5.0 and 10 Gbps modes. Some pairs are unused in some modes, per the following:
GBE0_MDI0-	A12	I/O Analog	3.3V max Suspend			
GBE0_MDI1+	A10	I/O Analog	3.3V max Suspend		Connect to Magnetics Module MDI1+/-	
GBE0_MDI1-	A9	I/O Analog	3.3V max Suspend			
GBE0_MDI2+	A7	I/O Analog	3.3V max Suspend		Connect to Magnetics Module MDI2+/-	
GBE0_MDI2-	A6	I/O Analog	3.3V max Suspend			
GBE0_MDI3+	A3	I/O Analog	3.3V max Suspend		Connect to Magnetics Module MDI3+/-	
GBE0_MDI3-	A2	I/O Analog	3.3V max Suspend			
GBE0_ACT#	B2	OD CMOS	3.3V Suspend/3.3V		Connect to LED and **recommend** current limit resistor 150Ω to 3.3VSB	Gigabit Ethernet Controller 0 activity indicator, active low.
GBE0_LINK#	A8	OD CMOS	3.3V Suspend/3.3V	LED for link speed with 1Gbps		Gigabit Ethernet Controller 0 link indicator, active low.
GBE0_LINK100#	A4	OD CMOS	3.3V Suspend/3.3V	LED for link speed with 2.5Gbps	Connect to LED and **recommend** current limit resistor 150Ω to 3.3VSB	Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.
GBE0_LINK1000#	A5	OD CMOS	3.3V Suspend/3.3V		Connect to LED and **recommend** current limit resistor 150Ω to 3.3VSB	Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.
GBE0_CTREF	A14	REF	GND min 3.3V max	NC		Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be limited to 250 mA or less.

	1000BASE-T 2.5GBASE-T 5.0GBASE-T 10GBASE-T	100BASE-TX	10BASE-T
MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-
MDI[1]+/-	B1_DB+/-	RX+/-	RX+/-
MDI[2]+/-	B1_DC+/-		
MDI[3]+/-	B1_DD+/-		

SATA Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGH960 PU/PD	Carrier Board	Description
SATA0_TX+	A16	O SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATA0 Conn TX pin	Serial ATA Channel 0 transmit differential pair.
SATA0_TX-	A17	O SATA	AC coupled on Module	AC Coupling capacitor		
SATA0_RX+	A19	I SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATA0 Conn RX pin	Serial ATA Channel 0 receive differential pair.
SATA0_RX-	A20	I SATA	AC coupled on Module	AC Coupling capacitor		
SATA1_TX+	B16	O SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATA1 Conn TX pin	Serial ATA Channel 1 transmit differential pair.
SATA1_TX-	B17	O SATA	AC coupled on Module	AC Coupling capacitor		
SATA1_RX+	B19	I SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATA1 Conn RX pin	Serial ATA Channel 1 receive differential pair.
SATA1_RX-	B20	I SATA	AC coupled on Module	AC Coupling capacitor		
SATA2_TX+	A22	O SATA	AC coupled on Module	AC Coupling capacitor	NA (No support)	Serial ATA Channel 2 transmit differential pair.
SATA2_TX-	A23	O SATA	AC coupled on Module	AC Coupling capacitor		
SATA2_RX+	A25	I SATA	AC coupled on Module	AC Coupling capacitor	NA (No support)	Serial ATA Channel 2 receive differential pair.
SATA2_RX-	A26	I SATA	AC coupled on Module	AC Coupling capacitor		
SATA3_TX+	B22	O SATA	AC coupled on Module	AC Coupling capacitor	NA (No support)	Serial ATA Channel 3 transmit differential pair.
SATA3_TX-	B23	O SATA	AC coupled on Module	AC Coupling capacitor		
SATA3_RX+	B25	I SATA	AC coupled on Module	AC Coupling capacitor	NA (No support)	Serial ATA Channel 3 receive differential pair.
SATA3_RX-	B26	I SATA	AC coupled on Module	AC Coupling capacitor		
ATA_ACT#	A28	I/O CMOS	3.3V / 3.3V		Connect to LED and **recommend** current limit resistor 220Ω to 3.3V	ATA (parallel and serial) activity indicator, active low.

▶ COM Express Connector Signal Description

PCI Express Lanes Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGH960 PU/PD	Carrier Board	Description
PCIE_TX0+	A68	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express differential transmit pairs 0
PCIE_TX0-	A69			AC Coupling capacitor		
PCIE_RX0+	B68	I PCIE	AC coupled off Module		**Device** - Connect AC Coupling cap 0.1uF for Gen1/2 ; 0.22uF for Gne3 **Slot** - Connect to PCIE Conn pin	PCI Express differential receive pairs 0
PCIE_RX0-	B69					
PCIE_TX1+	A64	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express differential transmit pairs 1
PCIE_TX1-	A65			AC Coupling capacitor		
PCIE_RX1+	B64	I PCIE	AC coupled off Module		**Device** - Connect AC Coupling cap 0.1uF for Gen1/2 ; 0.22uF for Gne3 **Slot** - Connect to PCIE Conn pin	PCI Express differential receive pairs 1
PCIE_RX1-	B65					
PCIE_TX2+	A61	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express differential transmit pairs 2
PCIE_TX2-	A62			AC Coupling capacitor		
PCIE_RX2+	B61	I PCIE	AC coupled off Module		**Device** - Connect AC Coupling cap 0.1uF for Gen1/2 ; 0.22uF for Gne3 **Slot** - Connect to PCIE Conn pin	PCI Express differential receive pairs 2
PCIE_RX2-	B62					
PCIE_TX3+	A58	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express differential transmit pairs 3
PCIE_TX3-	A59			AC Coupling capacitor		
PCIE_RX3+	B58	I PCIE	AC coupled off Module		**Device** - Connect AC Coupling cap 0.1uF for Gen1/2 ; 0.22uF for Gne3 **Slot** - Connect to PCIE Conn pin	PCI Express differential receive pairs 3
PCIE_RX3-	B59					
PCIE_TX4+	A55	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express differential transmit pairs 4
PCIE_TX4-	A56			AC Coupling capacitor		
PCIE_RX4+	B55	I PCIE	AC coupled off Module		**Device** - Connect AC Coupling cap 0.1uF for Gen1/2 ; 0.22uF for Gne3 **Slot** - Connect to PCIE Conn pin	PCI Express differential receive pairs 4
PCIE_RX4-	B56					
PCIE_TX5+	A52	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express differential transmit pairs 5
PCIE_TX5-	A53			AC Coupling capacitor		
PCIE_RX5+	B52	I PCIE	AC coupled off Module		**Device** - Connect AC Coupling cap 0.1uF for Gen1/2 ; 0.22uF for Gne3 **Slot** - Connect to PCIE Conn pin	PCI Express differential receive pairs 5 (
PCIE_RX5-	B53					
PCIE_TX6+	D19	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express differential transmit pairs 6
PCIE_TX6-	D20			AC Coupling capacitor		
PCIE_RX6+	C19	I PCIE	AC coupled off Module		**Device** - Connect AC Coupling cap 0.1uF **Slot** - Connect to PCIE Conn pin	PCI Express differential receive pairs 6
PCIE_RX6-	C20					
PCIE_TX7+	D22	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express differential transmit pairs 7
PCIE_TX7-	D23			AC Coupling capacitor		
PCIE_RX7+	C22	I PCIE	AC coupled off Module		**Device** - Connect AC Coupling cap 0.1uF for Gen1/2 ; 0.22uF for Gne3 **Slot** - Connect to PCIE Conn pin	PCI Express differential receive pairs 7
PCIE_RX7-	C23					
PCIE0_CK_REF+	A88	O PCIE	PCIE		Connect to PCIE device, **PCIe CLK Buffer** or slot	Reference clock output for all PCI Express and PCI Express Graphics lanes.
PCIE0_CK_REF-	A89					

PCI Express Lanes Signals Descriptions (PCIE Gen4 on board NVME SSD Only)

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGH960 PU/PD	Carrier Board	Description
PCIE4_TX0+	NA	O PCIE	AC coupled on Module	AC Coupling capacitor	NA (for On board NVME SSD only)	PCI Express differential transmit pairs 0
PCIE4_TX0-	NA			AC Coupling capacitor		
PCIE4_RX0+	NA	I PCIE	AC coupled on Module	AC Coupling capacitor	NA (for On board NVME SSD only)	PCI Express differential receive pairs 0
PCIE4_RX0-	NA			AC Coupling capacitor		
PCIE4_TX1+	NA	O PCIE	AC coupled on Module	AC Coupling capacitor	NA (for On board NVME SSD only)	PCI Express differential transmit pairs 1
PCIE4_TX1-	NA			AC Coupling capacitor		
PCIE4_RX1+	NA	I PCIE	AC coupled on Module	AC Coupling capacitor	NA (for On board NVME SSD only)	PCI Express differential receive pairs 1
PCIE4_RX1-	NA			AC Coupling capacitor		
PCIE4_TX2+	NA	O PCIE	AC coupled on Module	AC Coupling capacitor	NA (for On board NVME SSD only)	PCI Express differential transmit pairs 2
PCIE4_TX2-	NA			AC Coupling capacitor		
PCIE4_RX2+	NA	I PCIE	AC coupled on Module	AC Coupling capacitor	NA (for On board NVME SSD only)	PCI Express differential receive pairs 2
PCIE4_RX2-	NA			AC Coupling capacitor		
PCIE4_TX3+	NA	O PCIE	AC coupled on Module	AC Coupling capacitor	NA (for On board NVME SSD only)	PCI Express differential transmit pairs 3
PCIE4_TX3-	NA			AC Coupling capacitor		
PCIE4_RX3+	NA	I PCIE	AC coupled on Module	AC Coupling capacitor	NA (for On board NVME SSD only)	PCI Express differential receive pairs 3
PCIE4_RX3-	NA			AC Coupling capacitor		

▶ COM Express Connector Signal Description

PEG Signals Descriptions (PCIE Gen4)

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGH960 PU/PD	Carrier Board	Description
PEG_TX0+	D52	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Graphics transmit differential pairs 0
PEG_TX0-	D53			AC Coupling capacitor		
PEG_RX0+	C52	I PCIE	AC coupled off Module		**Device** - Connect AC Coupling cap 0.1uF for Gen1/2 ; 0.22uF for Gne3/4 **Slot** - Connect to PCIE Conn pin	PCI Express Graphics receive differential pairs 0
PEG_RX0-	C53					
PEG_TX1+	D55	O PCIE	AC coupled on Module	AC Coupling capacitor	**Device** - Connect AC Coupling cap 0.1uF for Gen1/2 ; 0.22uF for Gne3/4 **Slot** - Connect to PCIE Conn pin	PCI Express Graphics transmit differential pairs 1
PEG_TX1-	D56			AC Coupling capacitor		
PEG_RX1+	C55	I PCIE	AC coupled off Module		Connect to PCIE device or slot	PCI Express Graphics receive differential pairs 1
PEG_RX1-	C56					
PEG_TX2+	D58	O PCIE	AC coupled on Module	AC Coupling capacitor	**Device** - Connect AC Coupling cap 0.1uF for Gen1/2 ; 0.22uF for Gne3/4 **Slot** - Connect to PCIE Conn pin	PCI Express Graphics transmit differential pairs 2
PEG_TX2-	D59			AC Coupling capacitor		
PEG_RX2+	C58	I PCIE	AC coupled off Module		Connect to PCIE device or slot	PCI Express Graphics receive differential pairs 2
PEG_RX2-	C59					
PEG_TX3+	D61	O PCIE	AC coupled on Module	AC Coupling capacitor	**Device** - Connect AC Coupling cap 0.1uF for Gen1/2 ; 0.22uF for Gne3/4 **Slot** - Connect to PCIE Conn pin	PCI Express Graphics transmit differential pairs 3
PEG_TX3-	D62			AC Coupling capacitor		
PEG_RX3+	C61	I PCIE	AC coupled off Module		Connect to PCIE device or slot	PCI Express Graphics receive differential pairs 3
PEG_RX3-	C62					
PEG_TX4+	D65	O PCIE	AC coupled on Module	AC Coupling capacitor	**Device** - Connect AC Coupling cap 0.1uF for Gen1/2 ; 0.22uF for Gne3/4 **Slot** - Connect to PCIE Conn pin	PCI Express Graphics transmit differential pairs 4
PEG_TX4-	D66			AC Coupling capacitor		
PEG_RX4+	C65	I PCIE	AC coupled off Module		Connect to PCIE device or slot	PCI Express Graphics receive differential pairs 4
PEG_RX4-	C66					
PEG_TX5+	D68	O PCIE	AC coupled on Module	AC Coupling capacitor	**Device** - Connect AC Coupling cap 0.1uF for Gen1/2 ; 0.22uF for Gne3/4 **Slot** - Connect to PCIE Conn pin	PCI Express Graphics transmit differential pairs 5
PEG_TX5-	D69			AC Coupling capacitor		
PEG_RX5+	C68	I PCIE	AC coupled off Module		Connect to PCIE device or slot	PCI Express Graphics receive differential pairs 5
PEG_RX5-	C69					
PEG_TX6+	D71	O PCIE	AC coupled on Module	AC Coupling capacitor	**Device** - Connect AC Coupling cap 0.1uF for Gen1/2 ; 0.22uF for Gne3/4 **Slot** - Connect to PCIE Conn pin	PCI Express Graphics transmit differential pairs 6
PEG_TX6-	D72			AC Coupling capacitor		
PEG_RX6+	C71	I PCIE	AC coupled off Module		Connect to PCIE device or slot	PCI Express Graphics receive differential pairs 6
PEG_RX6-	C72					
PEG_TX7+	D74	O PCIE	AC coupled on Module	AC Coupling capacitor	**Device** - Connect AC Coupling cap 0.1uF for Gen1/2 ; 0.22uF for Gne3/4 **Slot** - Connect to PCIE Conn pin	PCI Express Graphics transmit differential pairs 7
PEG_TX7-	D75			AC Coupling capacitor		
PEG_RX7+	C74	I PCIE	AC coupled off Module		Connect to PCIE device or slot	PCI Express Graphics receive differential pairs 7
PEG_RX7-	C75					
PEG_TX8+	D78	O PCIE	AC coupled on Module	AC Coupling capacitor	**Device** - Connect AC Coupling cap 0.1uF for Gen1/2 ; 0.22uF for Gne3/4 **Slot** - Connect to PCIE Conn pin	PCI Express Graphics transmit differential pairs 8
PEG_TX8-	D79			AC Coupling capacitor		
PEG_RX8+	C78	I PCIE	AC coupled off Module		Connect to PCIE device or slot	PCI Express Graphics receive differential pairs 8
PEG_RX8-	C79					
PEG_TX9+	D81	O PCIE	AC coupled on Module	AC Coupling capacitor	**Device** - Connect AC Coupling cap 0.1uF for Gen1/2 ; 0.22uF for Gne3/4 **Slot** - Connect to PCIE Conn pin	PCI Express Graphics transmit differential pairs 9
PEG_TX9-	D82			AC Coupling capacitor		
PEG_RX9+	C81	I PCIE	AC coupled off Module		Connect to PCIE device or slot	PCI Express Graphics receive differential pairs 9
PEG_RX9-	C82					
PEG_TX10+	D85	O PCIE	AC coupled on Module	AC Coupling capacitor	**Device** - Connect AC Coupling cap 0.1uF for Gen1/2 ; 0.22uF for Gne3/4 **Slot** - Connect to PCIE Conn pin	PCI Express Graphics transmit differential pairs 10
PEG_TX10-	D86			AC Coupling capacitor		
PEG_RX10+	C85	I PCIE	AC coupled off Module		Connect to PCIE device or slot	PCI Express Graphics receive differential pairs 10
PEG_RX10-	C86					
PEG_TX11+	D88	O PCIE	AC coupled on Module	AC Coupling capacitor	**Device** - Connect AC Coupling cap 0.1uF for Gen1/2 ; 0.22uF for Gne3/4 **Slot** - Connect to PCIE Conn pin	PCI Express Graphics transmit differential pairs 11
PEG_TX11-	D89			AC Coupling capacitor		
PEG_RX11+	C88	I PCIE	AC coupled off Module		Connect to PCIE device or slot	PCI Express Graphics receive differential pairs 11
PEG_RX11-	C89					
PEG_TX12+	D91	O PCIE	AC coupled on Module	AC Coupling capacitor	**Device** - Connect AC Coupling cap 0.1uF for Gen1/2 ; 0.22uF for Gne3/4 **Slot** - Connect to PCIE Conn pin	PCI Express Graphics transmit differential pairs 12
PEG_TX12-	D92			AC Coupling capacitor		
PEG_RX12+	C91	I PCIE	AC coupled off Module		Connect to PCIE device or slot	PCI Express Graphics receive differential pairs 12
PEG_RX12-	C92					

▶ COM Express Connector Signal Description

PEG Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGH960 PU/PD	Carrier Board	Description
PEG_TX13+	D94	O PCIE	AC coupled on Module	AC Coupling capacitor	**Device** - Connect AC Coupling cap 0.1uF for Gen1/2 ; 0.22uF for Gne3/4	PCI Express Graphics transmit differential pairs 13
PEG_TX13-	D95			AC Coupling capacitor	**Slot** - Connect to PCIE Conn pin	
PEG_RX13+	C94	I PCIE	AC coupled off Module		Connect to PCIE device or slot	PCI Express Graphics receive differential pairs 13
PEG_RX13-	C95					
PEG_TX14+	D98	O PCIE	AC coupled on Module	AC Coupling capacitor	**Device** - Connect AC Coupling cap 0.1uF for Gen1/2 ; 0.22uF for Gne3/4	PCI Express Graphics transmit differential pairs 14
PEG_TX14-	D99			AC Coupling capacitor	**Slot** - Connect to PCIE Conn pin	
PEG_RX14+	C98	I PCIE	AC coupled off Module		Connect to PCIE device or slot	PCI Express Graphics receive differential pairs 14
PEG_RX14-	C99					
PEG_TX15+	D101	O PCIE	AC coupled on Module	AC Coupling capacitor	**Device** - Connect AC Coupling cap 0.1uF for Gen1/2 ; 0.22uF for Gne3/4	PCI Express Graphics transmit differential pairs 15
PEG_TX15-	D102			AC Coupling capacitor	**Slot** - Connect to PCIE Conn pin	
PEG_RX15+	C101	I PCIE	AC coupled off Module		Connect to PCIE device or slot	PCI Express Graphics receive differential pairs 15
PEG_RX15-	C102					
PEG_LANE_RV#	D54	I CMOS	3.3V / 3.3V	PU 20K to 3.3V		PCI Express Graphics lane reversal input strap. Pull low on the Carrier board to reverse lane order.

DDI Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGH960 PU/PD	Carrier Board	Description
DDI1_PAIR0+	D26	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DP1_LANE0+/- for DP / TMDS1_DATA2+/- for HDMI or DVI
DDI1_PAIR0-	D27				Connect AC Coupling Capacitors 0.1uF to Device	
DDI1_PAIR1+	D29	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DP1_LANE1+/- for DP / TMDS1_DATA1+/- for HDMI or DVI
DDI1_PAIR1-	D30				Connect AC Coupling Capacitors 0.1uF to Device	
DDI1_PAIR2+	D32	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DP1_LANE2+/- for DP / TMDS1_DATA0+/- for HDMI or DVI
DDI1_PAIR2-	D33				Connect AC Coupling Capacitors 0.1uF to Device	
DDI1_PAIR3+	D36	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DP1_LANE3+ for DP / TMDS1_CLK+/-
DDI1_PAIR3-	D37				Connect AC Coupling Capacitors 0.1uF to Device	
DDI1_PAIR4+	C25	I PCIE	AC coupled off Module		NA (No support)	NA (No support)
DDI1_PAIR4-	C26				NA (No support)	NA (No support)
DDI1_PAIR5+	C29	I PCIE	AC coupled off Module		NA (No support)	NA (No support)
DDI1_PAIR5-	C30				NA (No support)	NA (No support)
DDI1_PAIR6+	C15	I PCIE	AC coupled off Module		NA (No support)	NA (No support)
DDI1_PAIR6-	C16				NA (No support)	NA (No support)
DDI1_CTRLCLK_AUX+	D15	I/O PCIE	AC coupled on Module	PD 100K to GND **(S/W IC between Rpu/PCH)**	Connect to DP1 AUX+	DP AUX+ function if DDI1_DDC_AUX_SEL is no connect
		I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V, PD 100K to GND **(S/W IC between Rpu/Rpd resistor)**	Connect to HDMI1/DVI1 I2C CTRLCLK	HDMI/DVI I2C CTRLCLK if DDI1_DDC_AUX_SEL is pulled high
DDI1_CTRLCLK_AUX-	D16	I/O PCIE	AC coupled on Module	PU 100K to 3.3V **(S/W IC between Rpu/PCH)**	Connect to DP1 AUX-	DP AUX- function if DDI1_DDC_AUX_SEL is no connect
		I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V/PU 100K to 3.3V **(S/W IC between 2.2K/100K resistor)**	Connect to HDMI1/DVI1 I2C CTRLDATA	HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high
DDI1_HPD	C24	I CMOS	3.3V / 3.3V		PD 1M and Connect to device Hot Plug Detect	DDI Hot-Plug Detect
DDI1_DDC_AUX_SEL	D34	I CMOS	3.3V / 3.3V	PD 1M to GND	The DDC_AUX_SEL pin should be routed to pin 13 of the DisplayPort connector, to enable Dual-Mode PU 100K to 3.3V for DDC(HDMI/DVI)	Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRLDATA_AUX-. DDI[n]_DDC_AUX_SEL shall be pulled to 3.3V on the Carrier with a 100K Ohm resistor to configure the DDI[n]_AUX pair as the DDC channel. Carrier DDI[n]_DDC_AUX_SEL should be connected to pin 13 of the DisplayPort
DDI2_PAIR0+	D39	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DP2_LANE0+/- for DP / TMDS2_DATA2+/- for HDMI or DVI
DDI2_PAIR0-	D40				Connect AC Coupling Capacitors 0.1uF to Device	
DDI2_PAIR1+	D42	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DP2_LANE1+/- for DP / TMDS2_DATA1+/- for HDMI or DVI
DDI2_PAIR1-	D43				Connect AC Coupling Capacitors 0.1uF to Device	
DDI2_PAIR2+	D46	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DP2_LANE2+/- for DP / TMDS2_DATA0+/- for HDMI or DVI
DDI2_PAIR2-	D47				Connect AC Coupling Capacitors 0.1uF to Device	
DDI2_PAIR3+	D49	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DP2_LANE3+ for DP / TMDS2_CLK+/-
DDI2_PAIR3-	D50				Connect AC Coupling Capacitors 0.1uF to Device	

▶ COM Express Connector Signal Description

DDI Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGH960 PU/PD	Carrier Board	Description
DDI2_CTRLCLK_AUX+	C32	I/O PCIE	AC coupled on Module	PD 100K to GND **(S/W IC between Rpu/PCH)**	Connect to DP2 AUX+	DP AUX+ function if DDI2_DDC_AUX_SEL is no connect
		I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V, PD 100K to GND **(S/W IC between Rpu/Rpd resistor)**	Connect to HDMI2/DVI2 I2C CTRLCLK	HDMI/DVI I2C CTRLCLK if DDI2_DDC_AUX_SEL is pulled high
DDI2_CTRLDATA_AUX-	C33	I/O PCIE	AC coupled on Module	PU 100K to 3.3V **(S/W IC between Rpu/PCH)**	Connect to DP2 AUX-	DP AUX- function if DDI2_DDC_AUX_SEL is no connect
		I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V/PU 100K to 3.3V **(S/W IC between 2.2K/100K resistor)**	Connect to HDMI2/DVI2 I2C CTRLDATA	HDMI/DVI I2C CTRLDATA if DDI2_DDC_AUX_SEL is pulled high
DDI2_HPD	D44	I CMOS	3.3V / 3.3V		PD 1M and Connect to device Hot Plug Detect	DDI Hot-Plug Detect
DDI2_DDC_AUX_SEL	C34	I CMOS	3.3V / 3.3V	PD 1M to GND	The DDC_AUX_SEL pin should be routed to pin 13 of the DisplayPort connector, to enable Dual-Mode PU 100K to 3.3V for DDC(HDMI/DVI)	Selects the function of DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_AUX-. DDI[n]_DDC_AUX_SEL shall be pulled to 3.3V on the Carrier with a 100K Ohmresistor to configure the DDI[n]_AUX pair as the DDC channel. Carrier DDI[n]_DDC_AUX_SEL should be connected to pin 13 of the DisplayPort
DDI3_PAIR0+	C39	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 3 Pair 0 differential pairs/Serial Digital Video B red output differential pair
DDI3_PAIR0-	C40				Connect AC Coupling Capacitors 0.1uF to Device	
DDI3_PAIR1+	C42	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 3 Pair 1 differential pairs/Serial Digital Video B green output differential pair
DDI3_PAIR1-	C43				Connect AC Coupling Capacitors 0.1uF to Device	
DDI3_PAIR2+	C46	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 3 Pair 2 differential pairs/Serial Digital Video B blue output differential pair
DDI3_PAIR2-	C47				Connect AC Coupling Capacitors 0.1uF to Device	
DDI3_PAIR3+	C49	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 3 Pair 3 differential pairs/Serial Digital Video B clock output differential pair
DDI3_PAIR3-	C50				Connect AC Coupling Capacitors 0.1uF to Device	
DDI3_CTRLCLK_AUX+	C36	I/O PCIE	AC coupled on Module	PD 100K to GND (S/W IC between Rpu/PCH)	Connect to DP3 AUX+	DP AUX+ function if DDI3_DDC_AUX_SEL is no connect
		I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V, PD 100K to GND (S/W IC between Rpu/Rpd resistor)	Connect to HDMI3/DVI3 I2C CTRLCLK	HDMI/DVI I2C CTRLCLK if DDI3_DDC_AUX_SEL is pulled high
DDI3_CTRLDATA_AUX-	C37	I/O PCIE	AC coupled on Module	PU 100K to 3.3V (S/W IC between Rpu/PCH)	Connect to D3P AUX-	DP AUX- function if DDI3_DDC_AUX_SEL is no connect
		I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V/PU 100K to 3.3V (S/W IC between 2.2K/100K resistor)	Connect to HDMI3/DVI3 I2C CTRLDATA	HDMI/DVI I2C CTRLDATA if DDI3_DDC_AUX_SEL is pulled high
DDI3_HPD	C44	I CMOS	3.3V / 3.3V		PD 1M and Connect to device Hot Plug Detect	DDI Hot-Plug Detect
DDI3_DDC_AUX_SEL	C38	I CMOS	3.3V / 3.3V	PD 1M to GND	The DDC_AUX_SEL pin should be routed to pin 13 of the DisplayPort connector, to enable Dual-Mode PU 100K to 3.3V for DDC(HDMI/DVI)	Selects the function of DDI3_CTRLCLK_AUX+ and DDI3_CTRLDATA_AUX-. DDI[n]_DDC_AUX_SEL shall be pulled to 3.3V on the Carrier with a 100K Ohm resistor to configure the DDI[n]_AUX pair as the DDC channel. Carrier DDI[n]_DDC_AUX_SEL should be connected to pin 13 of the DisplayPort

USB Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGH960 PU/PD	Carrier Board	Description
USB0+	A46	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 0
USB0-	A45					
USB1+	B46	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 1
USB1-	B45					
USB2+	A43	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 2
USB2-	A42					
USB3+	B43	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 3
USB3-	B42					
USB4+	A40	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 4
USB4-	A39					
USB5+	B40	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 5
USB5-	B39					
USB6+	A37	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 6
USB6-	A36					
USB7+	B37	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 7, USB7 may be configured as a USB client or as a host, or both, at the Module designer's discretion.(CR901-B default set as a host)
USB7-	B36					

▶ COM Express Connector Signal Description

USB Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGH960 PU/PD	Carrier Board	Description
USB_0_1_OC#	B44	I CMOS	3.3V Suspend/3.3V	PU 10k to 3.3VSB	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 0 and 1. A pull-up for this lineshall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_2_3_OC#	A44	I CMOS	3.3V Suspend/3.3V	PU 10k to 3.3VSB	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 2 and 3. A pull-up for this lineshall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_4_5_OC#	B38	I CMOS	3.3V Suspend/3.3V	PU 10k to 3.3VSB	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 4 and 5. A pull-up for this lineshall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_6_7_OC#	A38	I CMOS	3.3V Suspend/3.3V	PU 10k to 3.3VSB	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 6 and 7. A pull-up for this lineshall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_SSTX0+	D4	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect 90Ω@100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSTX0-	D3					
USB_SSRX0+	C4	I PCIE	AC coupled off Module		Connect 90Ω@100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSRX0-	C3					
USB_SSTX1+	D7	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect 90Ω@100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSTX1-	D6					
USB_SSRX1+	C7	I PCIE	AC coupled off Module		Connect 90Ω@100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSRX1-	C6					
USB_SSTX2+	D10	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect 90Ω@100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSTX2-	D9					
USB_SSRX2+	C10	I PCIE	AC coupled off Module		Connect 90Ω@100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSRX2-	C9					
USB_SSTX3+	D13	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect 90Ω@100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSTX3-	D12					
USB_SSRX3+	C13	I PCIE	AC coupled off Module		Connect 90Ω@100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSRX3-	C12					

LVDS Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGH960 PU/PD	Carrier Board	Description
LVDS_A0+	A71	O LVDS	LVDS		Connect to LVDS connector	LVDS Channel A differential pairs Ther LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/-. LVDS_A_CK+/-, LVDS_B_CK+/-) shall have 100Ω terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializeron-board
LVDS_A0-	A72					
LVDS_A1+	A73	O LVDS	LVDS		Connect to LVDS connector	
LVDS_A1-	A74					
LVDS_A2+	A75	O LVDS	LVDS		Connect to LVDS connector	
LVDS_A2-	A76					
LVDS_A3+	A78	O LVDS	LVDS		Connect to LVDS connector	
LVDS_A3-	A79					
LVDS_A_CK+	A81	O LVDS	LVDS		Connect to LVDS connector	LVDS Channel A differential clock
LVDS_A_CK-	A82					
LVDS_B0+	B71	O LVDS	LVDS		Connect to LVDS connector	LVDS Channel B differential pairs Ther LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/-. LVDS_A_CK+/-, LVDS_B_CK+/-) shall have 100Ω terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializeron-board
LVDS_B0-	B72					
LVDS_B1+	B73	O LVDS	LVDS		Connect to LVDS connector	
LVDS_B1-	B74					
LVDS_B2+	B75	O LVDS	LVDS		Connect to LVDS connector	
LVDS_B2-	B76					
LVDS_B3+	B77	O LVDS	LVDS		Connect to LVDS connector	
LVDS_B3-	B78					
LVDS_B_CK+	B81	O LVDS	LVDS		Connect to LVDS connector	LVDS Channel B differential clock
LVDS_B_CK-	B82					
LVDS_VDD_EN	A77	O CMOS	3.3V / 3.3V	PD 100KΩ	Connect to enable control of LVDS panel power circuit	LVDS panel power enable
LVDS_BKLT_EN	B79	O CMOS	3.3V / 3.3V	PD 100KΩ	Connect to enable control of LVDS panel backlight power circuit.	LVDS panel backlight enable
LVDS_BKLT_CTRL	B83	O CMOS	3.3V / 3.3V	PD 100KΩ	Connect to brightness control of LVDS panel backlight power circuit.	LVDS panel backlight brightness control
LVDS_I2C_CK	A83	I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V	Connect to DDC clock of LVDS panel	I2C clock output for LVDS display use
LVDS_I2C_DAT	A84	I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V	Connect to DDC data of LVDS panel	I2C data line for LVDS display use

▶ COM Express Connector Signal Description

eDP Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGH960 PU/PD	Carrier Board	Description
eDP_TX2+	A71	O LV_DIFF	AC coupled off module		Connect to eDP connector	eDP differential pairs
eDP_TX2-	A72					
eDP_TX1+	A73	O LV_DIFF	AC coupled off module		Connect to eDP connector	
eDP_TX1-	A74					
eDP_TX0+	A75	O LV_DIFF	AC coupled off module		Connect to eDP connector	
eDP_TX0-	A76					
eDP_TX3+	A81	O LV_DIFF	AC coupled off module		Connect to eDP connector	
eDP_TX3-	A82					
eDP_VDD_EN	A77	O CMOS	3.3V / 3.3V	PD 100KΩ	Connecto to enable eDP power.	eDP power enable
eDP_BKLT_EN	B79	I/O LV_DIFF	AC couple off module	PD 100KΩ	Connect to enable control of eDP backlight power circuit.	eDP backlight enable
eDP_BKLT_CTRL	B83	O CMOS	3.3V / 3.3V	PD 100KΩ	Connect to brightness control of eDP panel backlight power circuit.	eDP backlight brightness control
eDP_AUX+	A83	I/O LV_DIFF	AC couple off module	PD 100KΩ	eDP AUX+eDP AUX-	I2C clock output for LVDS display use
eDP_AUX-	A84	I/O LV_DIFF		PU 100KΩ to 3.3V		I2C data line for LVDS display use
eDP_HPD	A87	I CMOS	3.3V / 3.3V		eDP connector hot plug detection	Detection of Hot Plug/ Unplug and notification of the link layer

LPC & eSPI Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGH960 PU/PD	Carrier Board	Description
LPC_AD0/ESPI_IO_0	B4	I/O CMOS	3.3V / 3.3V 1.8V Suspend /1.8V	LPC_ADC0 (ESPI to LPC bridge to Mux S/W) SoC ESPI_IO_0 to Mux S/W	Connect to LPC or ESPI device	LPC & eSPI multi-function pin with bridge
LPC_AD1/ESPI_IO_1	B5			LPC_ADC1 (ESPI to LPC bridge to Mux S/W) SoC ESPI_IO_1 to Mux S/W		
LPC_AD2/ESPI_IO_2	B6			LPC_ADC2 (ESPI to LPC bridge to Mux S/W) SoC ESPI_IO_2 to Mux S/W		
LPC_AD3/ESPI_IO_3	B7			LPC_ADC3 (ESPI to LPC bridge to Mux S/W) SoC ESPI_IO_3 to Mux S/W		
LPC_FRAME#/ESPI_CS0#	B3	O CMOS	3.3V / 3.3V 1.8V Suspend /1.8V	LPC_FRAME#(ESPI to LPC bridge to Mux S/W) SoC ESPI_CS1 to Mux S/W		LPC frame indicates the start of an LPC cycle eSPI Master Chip Select Outputs Driving Chip Select0#.
LPC_DRQ0/ESPI_ALERT0#	B8	I CMOS	3.3V / 3.3V 1.8V Suspend /1.8V	PU 10K to 3V3 to Mux S/W SoC ESPI_ALERT1# to Mux S/W		LPC: NA (No support) ESPI : Supported
LPC_DRQ1#/ESPI_ALERT1#	B9			PU 10K to 3V3 to Mux S/W SoC _ESPI_ALERT2# to Mux S/W		
LPC_SERIRQ/ESPI_CS1#	A50	I/O CMOS	3.3V / 3.3V 1.8V Suspend /1.8V	LPC_SERIRQ (ESPI to LPC bridge to Mux S/W) SoC ESPI_CS2# to Mux S/W		LPC serial interrupt eSPI Master Chip Select Outputs Driving Chip Select1#
LPC_CLK/ESPI_CK	B10	O CMOS	3.3V / 3.3V 1.8V Suspend /1.8V	LPC_CLK(ESPI to LPC bridge to Mux S/W) SoC ESPI_CLK to Mux S/W		LPC clock output - 33MHz nominal ESPI: eSPI Master Clock Output

SPI Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGH960 PU/PD	Carrier Board	Description
SPI_CS#	B97	O CMOS	3.3V Suspend/3.3V	Connect to S/W IC to BTB connector	Connect a series resistor 33Ω to Carrier Board SPI Device CS# pin	Chip select for Carrier Board SPI - may be sourced from chipset SPI0 or SPI1
SPI_MISO	A92	I CMOS	3.3V Suspend/3.3V	10Ω series resistor to BTB connector	Connect a series resistor 33Ω to Carrier Board SPI Device SO pin	Data in to Module from Carrier SPI
SPI_MOSI	A95	O CMOS	3.3V Suspend/3.3V	10Ω series resistor to BTB connector With PU 4.7KΩ to 3V3DU	Connect a series resistor 33Ω to Carrier Board SPI Device SI pin	Data out from Module to Carrier SPI
SPI_CLK	A94	O CMOS	3.3V Suspend/3.3V	10Ω series resistor to BTB connector With PD 100KΩ	Connect a series resistor 33Ω to Carrier Board SPI Device SCK pin	Clock from Module to Carrier SPI
SPI_POWER	A91	O	3.3V Suspend/3.3V		Connect to Carrier Board SPI Device VCC pin	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. TheModule shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall onlybe used to power SPI devices on the Carrier
BIOS_DIS0#	A34	I CMOS	NA	PU 10KΩ to 3V3 Suspend		Selection straps to determine the BIOS boot device. The Carrier should only float these or pull them low, please refer table as below
BIOS_DIS1#	B88			PU 10KΩ to 3V3 Suspend		

BIOS DIS1#	BIOS DIS0#	Chipset SPI(CS1# Destination	Chipset SPI(CS0# Destination	Carrier SPI_CS#	SPI Descriptor	Bios Entry	Ref Line
1	1	Module	Module	High	Module	SPI0/SPI1	0
1	0	Module	Module	High	Module	Carrier FWH	1
0	1	Module	Carrier	SPI 0	Carrier	SPI0/SPI1	2
0	0	**Carrier (Default)**	**Module (Default)**	**SPI1 (Default)**	**Module (Default)**	**SPI0/SPI1 (Default)**	**3**

▶ COM Express Connector Signal Description

VGA Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGH960 PU/PD	Carrier Board	Description
VGA_RED	B89	O Analog	Analog	PD 150 to GND	**PD 150R,connect to VGA connector with EMI filter & ESD protect component.**	Red for monitor. Analog output
VGA_GRN	B91	O Analog	Analog	PD 150 to GND	**PD 150R,connect to VGA connector with EMI filter & ESD protect component.**	Green for monitor. Analog output
VGA_BLU	B92	O Analog	Analog	PD 150 to GND	**PD 150R,connect to VGA connector with EMI filter & ESD protect component.**	Blue for monitor. Analog output
VGA_HSYNC	B93	O CMOS	3.3V / 3.3V		**Connect to VGA connector with a3.3V Buffer IC to isolate PCH & Display Device**	Horizontal sync output to VGA monitor
VGA_VSYNC	B94	O CMOS	3.3V / 3.3V		**Connect to VGA connector with a 33V Buffer IC to isolate PCH & Display Device**	Vertical sync output to VGA monitor
VGA_I2C_CK	B95	I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V	**Connect to VGA connector with a 3.3V to 5V Level shift circuit.**	DDC clock line (I2C port dedicated to identify VGA monitor capabilities)
VGA_I2C_DAT	B96	I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V	**Connect to VGA connector with a 3.3V to 5V Level shift circuit.**	DDC data line.

Serial Interface Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGH960 PU/PD	Carrier Board	Description
SER0_TX	A98	O CMOS	5V / 12V		Suggest follow PICMG COM Express Module board specification v3.0 section 5.8.1 for application	General purpose serial port 0 transmitter **(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)**
SER0_RX	A99	I CMOS	5V / 12V	PU 10K to 3.3V	Suggest follow PICMG COM Express Module board specification v3.0 section 5.8.1 for application	General purpose serial port 0 receiver **(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)**
SER1_TX	A101	O CMOS	5V / 12V		Suggest follow PICMG COM Express Module board specification v3.0 section 5.8.1 for application	General purpose serial port 1 transmitter **(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)**
SER1_RX	A102	I CMOS	5V / 12V	PU 10K to 3.3V	Suggest follow PICMG COM Express Module board specification v3.0 section 5.8.1 for application	General purpose serial port 1 receiver **(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)**

Power and System Management Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	TGH960 PU/PD	Carrier Board	Description
PWRBTN#	B12	I CMOS	3.3V Suspend/3.3V	PU 10K to 3V3_DU_EC		A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off andother suspend states, as well as powering the system down.
SYS_RESET#	B49	I CMOS	3.3V Suspend/3.3V	PU 10K to 3V3_DU		Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# isnot able to reestablish control of the system, PWR_OK or a powercycle may be used.
CB_RESET#	B50	O CMOS	3.3V Suspend/3.3V			Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimumspecification, a watchdog timeout, or may be initiated by the Module software.
PWR_OK	B24	I CMOS	3.3V / 3.3V	PU 10K to 5V and PD 20K		Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGAs or other configurable devices time to be programmed.
SUS_STAT#/ESPI_RESET#	B18	O CMOS	3.3V Suspend/3.3V 1.8V Suspend /1.8V	LPC Mode: PU 1K to 3V3DU to MUX S/W ESPI Mode: SoC ESPI_RESET# to Mux S/W		LPC Mode: Indicates imminent suspend operation; used to notify LPC devices. ESPI Mode: eSPI Reset Reset the eSPI interface for both master and slaves. eSPI Reset# is typically driven from eSPI master to eSPI slaves.
SUS_S3#	A15	O CMOS	3.3V Suspend/3.3V	PD 100K to GND		Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board may be used to enable the non-standby power on a typical ATX supply.
SUS_S4#	A18	O CMOS	3.3V Suspend/3.3V	PD 100K to GND		Indicates system is in Suspend to Disk state. Active low output.
SUS_S5#	A24	O CMOS	3.3V Suspend/3.3V	PD 100K to GND		Indicates system is in Soft Off state.
WAKE0#	B66	I CMOS	3.3V Suspend/3.3V	PU 1K to 3V3_DU		PCI Express wake up signal.
WAKE1#	B67	I CMOS	3.3V Suspend/3.3V	PU 10K to 3V3_DU		General purpose wake up signal. May be used to implementwake-upon PS2 keyboard or mouse activity.
BATLOW#	A27	I CMOS	3.3V Suspend/ 3.3V	PU 10K to 3V3_DU		Indicates that external battery is low. This port provides a battery-low signal to the Module for orderlytransitioning to power saving or power cut-off ACPI modes.
LID#	A103	I OD CMOS	3.3V Suspend/12V	PU 47K to 3V3_DU_EC		LID switch. Low active signal used by the ACPI operating system for a LID switch. **(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)**
SLEEP#	B103	I OD CMOS	3.3V Suspend/12V	PU 10K to 3V3_DU_EC		Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again. **(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)**
THRM#	B35	I CMOS	3.3V / 3.3V	PU 10K to 3V3		Input from off-Module temp sensor indicating an over-temp situation.
THRMTRIP#	A35	O CMOS	3.3V / 3.3V	PU 10K to 3.3V		Active low output indicating that the CPU has entered thermal shutdown.
SMB_CK	B13	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3V3_DU_EC		System Management Bus bidirectional clock line.
SYS_RESET#	B49	I CMOS	3.3V Suspend/3.3V	PU 10K to 3V3_DU		Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power.
SMB_DAT	B14	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3V3_DU_EC		System Management Bus bidirectional data line.
SMB_ALERT#	B15	I CMOS	3.3V Suspend/3.3V	PU 2.2K to 3V3_DU_EC		System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.

▶ COM Express Connector Signal Description

GPIO Signals Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	TGH960 PU/PD	Carrier Board	Description
GPO0	A93	O CMOS	3.3V / 3.3V			General purpose output pins. **Upon a hardware reset, these outputs should be low.**
GPO1	B54					
GPO2	B57					
GPO3	B63					
GPI0	A54	I CMOS	3.3V / 3.3V	PU 10K to 3.3V(PCH side)		General purpose input pins. **Pulled high internally on the Module.**
GPI1	A63			PU 10K to 3.3V(PCH side)		
GPI2	A67			PU 10K to 3.3V(PCH side)		
GPI3	A85			PU 10K to 3.3V(PCH side)		

Power and GND Signal Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	TGH960 PU/PD	Carrier Board	Description
VCC_12V	A104~A109 B104~B109C104~C109D104~D109	Power				Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.
VCC_5V_SBY	B84~B87	Power				Standby power input: +5.0V nominal. If VCC5_SBY isused, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected ifthese functions are not used in the system design.
VCC_RTC	A47	Power				Real-time clock circuit-power input. Nominally +3.0V.
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1,B11, B21 ,B31, B41, B51, B60, B70, B80, B90, B100, B110, C1, C2, C5, C8, C11,C14, C21, C31, C41, C51, C60, C70, C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11,D14, D21, D31, D41,D51, D60, D67, D70,D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Power				Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied toCarrierBoard GND plane.

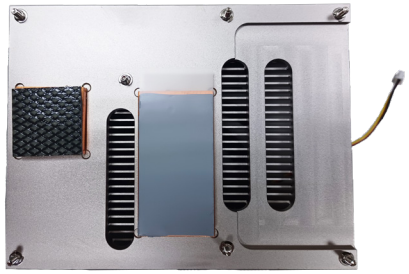
Miscellaneous Signal Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	TGH960 PU/PD	Carrier Board	Description
I2C_CK	B33	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3V3DU		General purpose I2C port clock output
I2C_DAT	B34	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3V3DU		General purpose I2C port data I/O line
SPKR	B32	O CMOS	3.3V / 3.3V	PD 10K		Output for audio enunciator - the "speaker" in PC-AT systems. This port provides the PC beep signal and is mostly intended for debugging purposes.
WDT	B27	O CMOS	3.3V / 3.3V	PD 100K		Output indicating that a watchdog time-out event has occurred.
FAN_PWNOUT	B101	O OD CMOS	3.3V / 3.3V	RSV PD 100K		Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM. **(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)**
FAN_TACHIN	B102	I OD CMOS	3.3V / 3.3V			Fan tachometer input for a fan with a two pulse output. **(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)**
TPM_PP	A96	I CMOS	3.3V / 3.3V	PD 10K		Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has aninternal pull down. This signal is used to indicate Physical Presence to the TPM.

▶ Cooling Option

Heat Sink

The COM Express connector is used to interface the TGH960 COM Express board to a carrier board. Connect the COM Express connector (located on the solder side of the board) to the COM Express connector on the carrier board.

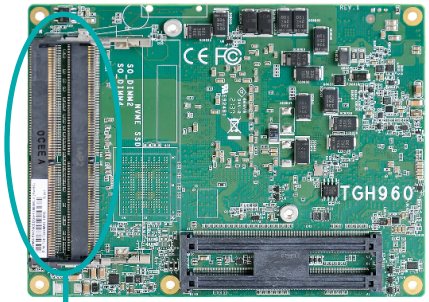
Top View of the Heat Sink



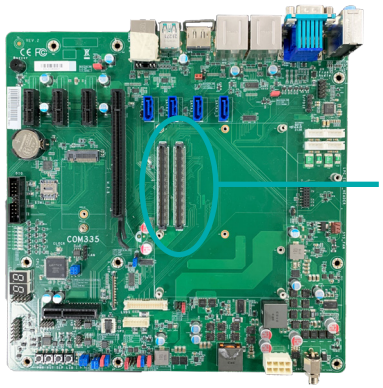
Bottom View of the Heat Sink

Important:
Remove the plastic covering from the thermal pads prior to mounting the heat sink onto board.

Important:
The carrier board (COM335) used in this section is for reference purpose only and may not resemble your carrier board. These illustrations are mainly to guide you on how to install TGH960 onto the carrier board of your choice. .

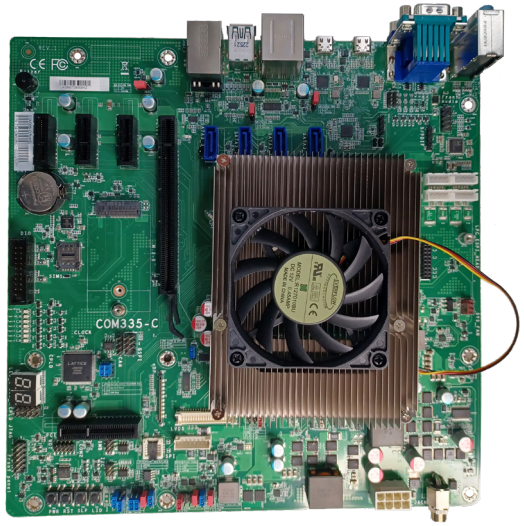


COM Express connector on TGH960



COM Express connector on the carrier board

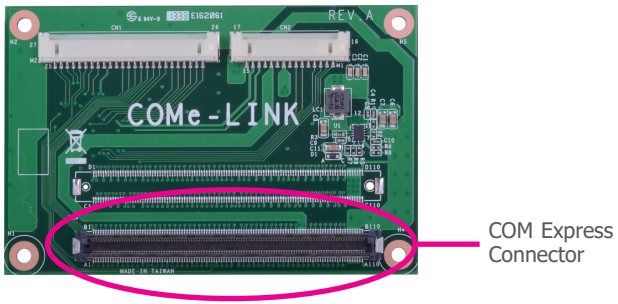
2. Align the mounting holes of the heatsink with the mounting holes of the module. Use the provided mounting screws to install the heat sink onto the module.

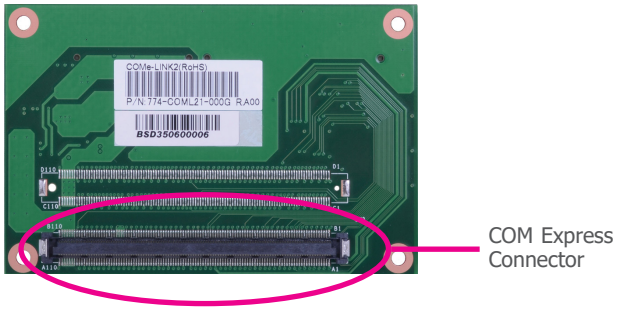


▶ Installing the COM Express Debug Card

Note:
The system board used in the following illustrations may not resemble the actual board. These illustrations are for reference only.

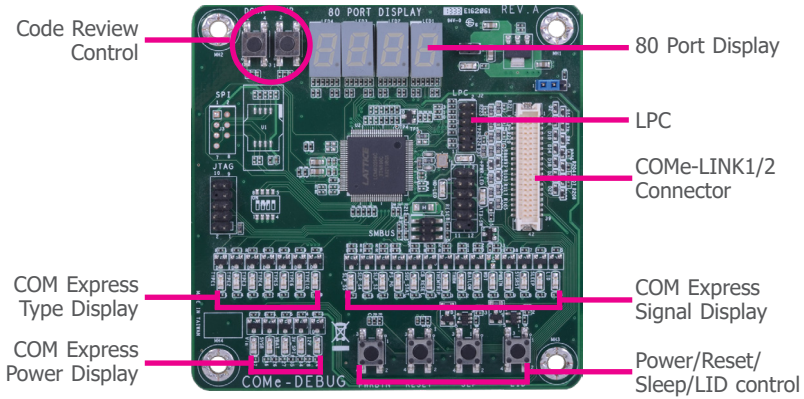
1. COMe-LINK2 is the COM Express debug platform installed into COM Express Mini modules for the application of debugging and displaying signals and codes.



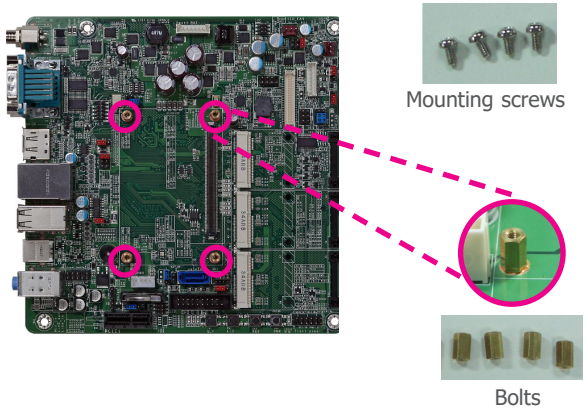


2. Connect the COMe-DEBUG card to COMe-LINK2 via a cable.

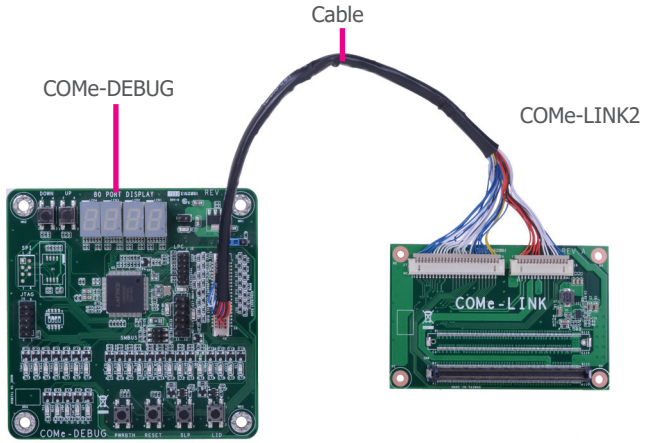
COMe-DEBUG

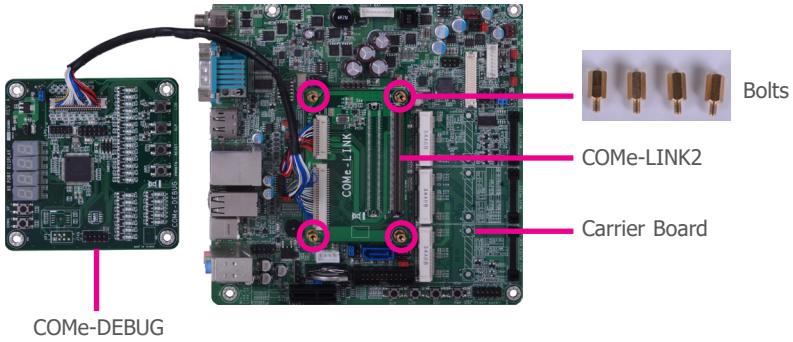


3. Fasten bolts with mounting screws through mounting holes to be fixed in place.

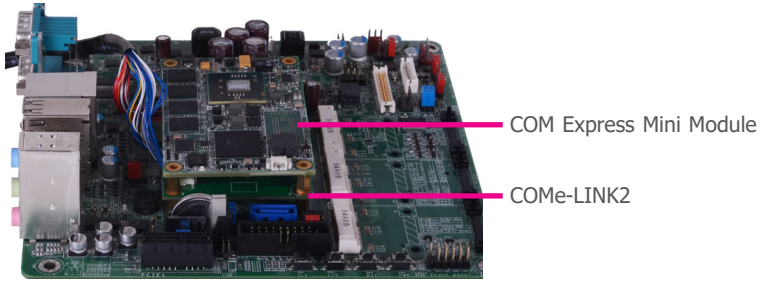


4. Use the provided bolts to fix the COMe-LINK2 debug card onto the carrier board.

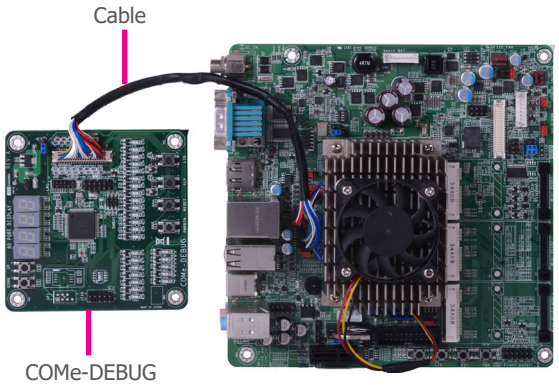




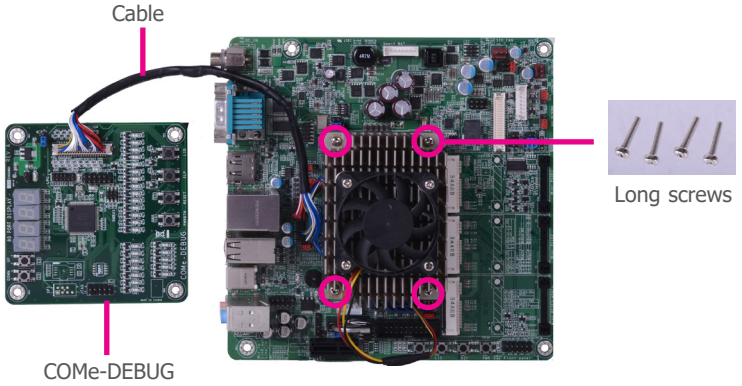
5. Grasp the COM Express Mini module by its edges to press it down on the top of the COMe-LINK2 debug card.

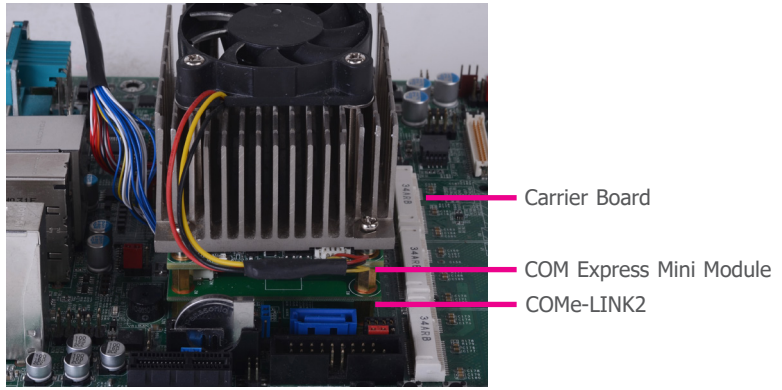


6. Then, grasp the heat sink by its edges and position it down firmly on the top of the COM Express Mini module.



7. Use the long mounting screws to secure the heat sink on the top of the COM Express Mini module and the COMe-LINK2 debug card and connect the cooling fan's cable to the fan connector on the COM Express Mini module. The photo below shows the locations of long mounting screws.





Side View of the Module, Debug Card and Carrier Board

Chapter 4 - BIOS Setup

Overview

The BIOS is a program that takes care of the basic level of communication between the CPU and peripherals. It contains codes for various advanced features found in this system board. The BIOS allows you to configure the system and save the configuration in a battery-backed CMOS so that the data retains even when the power is off. In general, the information stored in the CMOS RAM of the EEPROM will stay unchanged unless a configuration change has been made such as a hard drive replaced or a device added.

It is possible that the CMOS battery will fail causing CMOS data loss. If this happens, you need to install a new CMOS battery and reconfigure the BIOS settings.

Note:
The BIOS is constantly updated to improve the performance of the system board; therefore the BIOS screens in this chapter may not appear the same as the actual one. These screens are for reference purpose only.

Default Configuration

Most of the configuration settings are either predefined according to the Load Optimal Defaults settings which are stored in the BIOS or are automatically detected and configured without requiring any actions. There are a few settings that you may need to change depending on your system configuration.

Entering the BIOS Setup Utility

The BIOS Setup Utility can only be operated from the keyboard and all commands are keyboard commands. The commands are available at the right side of each setup screen.
The BIOS Setup Utility does not require an operating system to run. After you power up the system, the BIOS message appears on the screen and the memory count begins. After the memory test, the message “Press DEL to run setup” will appear on the screen. If the message disappears before you respond, restart the system or press the “Reset” button. You may also restart the system by pressing the <Ctrl> <Alt> and <Del> keys simultaneously.

Legends

KEYs	Function
Right and Left Arrows	Moves the highlight left or right to select a menu.
Up and Down Arrows	Moves the highlight up or down between submenus or fields.
<Esc>	Exits to the BIOS setup utility
+ (plus key)	Scrolls forward through the values or options of the hightlighted field.
- (minus key)	Scolls backward through the values or options of the hightlighted field.
<F1>	Displays general help
<F2>	Displays previous values
<F9>	Optimized defaults
<F10>	Saves and reset the setup program.
<Enter>	Press <Enter> to enter the highlighted submenu

Scroll Bar

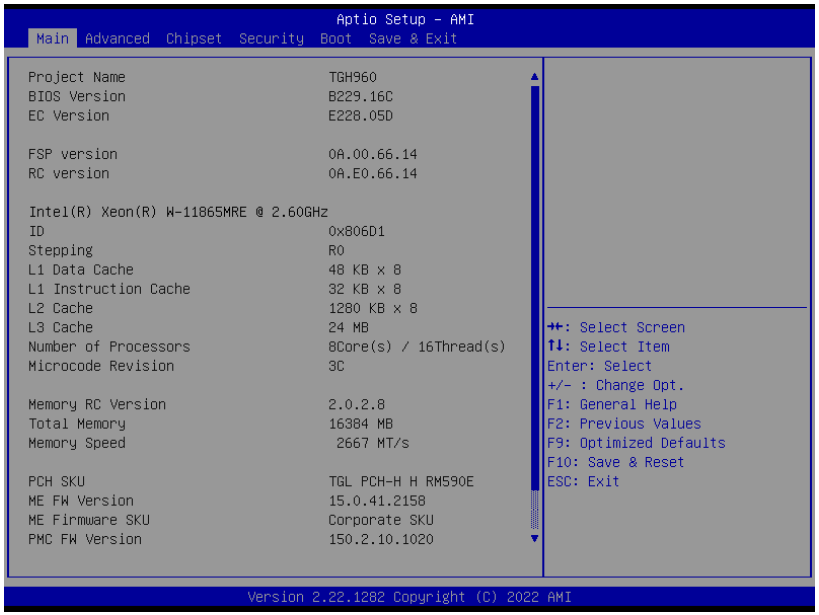
When a scroll bar appears to the right of the setup screen, it indicates that there are more available fields not shown on the screen. Use the up and down arrow keys to scroll through all the available fields.

Submenu

When “▶” appears on the left of a particular field, it indicates that a submenu which contains additional options are available for that field. To display the submenu, move the highlight to that field and press <Enter>.

▶ Main

The Main menu is the first screen that you will see when you enter the BIOS Setup Utility.



System Date

The date format is <month>, <date>, <year>. Press "Tab" to switch to the next field and press "-" or "+" to modify the value.

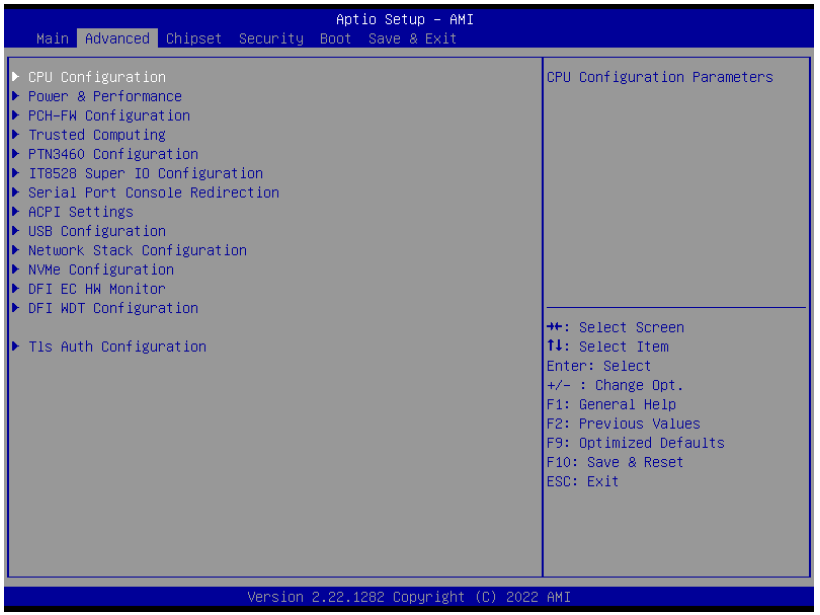
System Time

The time format is <hour>, <minute>, <second>. The time is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Hour displays hours from 00 to 23. Minute displays minutes from 00 to 59. Second displays seconds from 00 to 59.

▶ Advanced

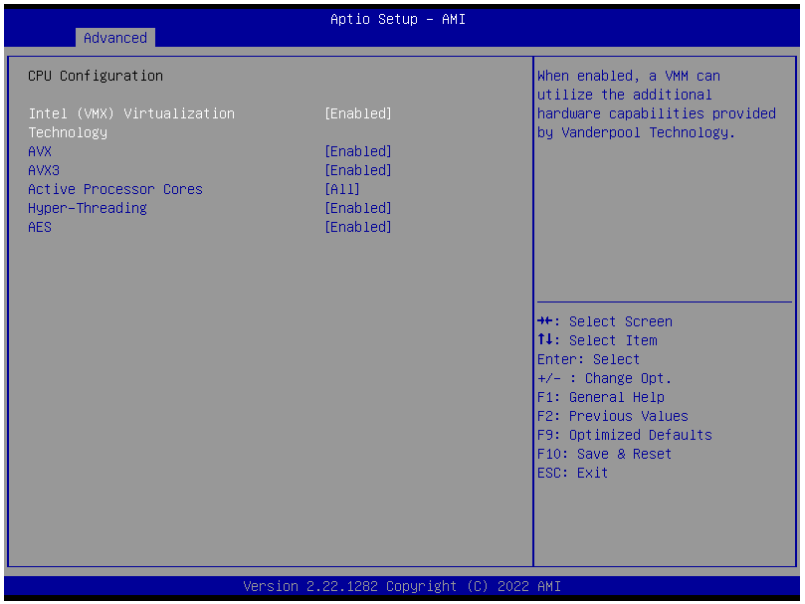
The Advanced menu allows you to configure your system for basic operation. Some entries are defaults required by the system board, while others, if enabled, will improve the performance of your system or let you set some features according to your preference.

Important:
Setting incorrect field values may cause the system to malfunction.



▶ Advanced

CPU Configuration



Intel (VMX) Virtualization Technology

When this field is set to Enabled, the VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

Active Processor Cores

Select number of cores to enable in each processor package.

Hyper-threading

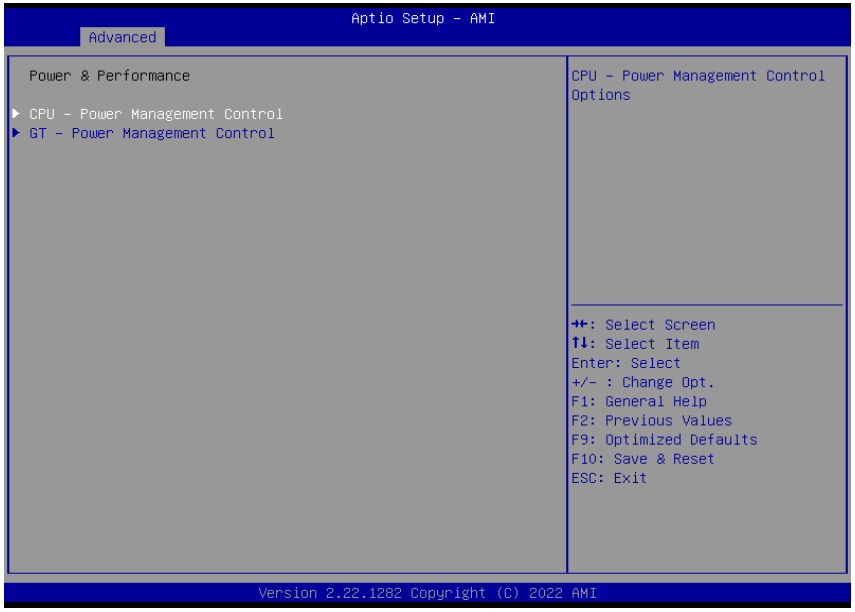
Enables this field for Windows XP and Linux which are optimized for Hyper-Threading technology. Select disabled for other OSes not optimized for Hyper-Threading technology. When disabled, only one thread per enabled core is enabled.

AES

Enable/Disable AES (Advanced Encryption Standard)

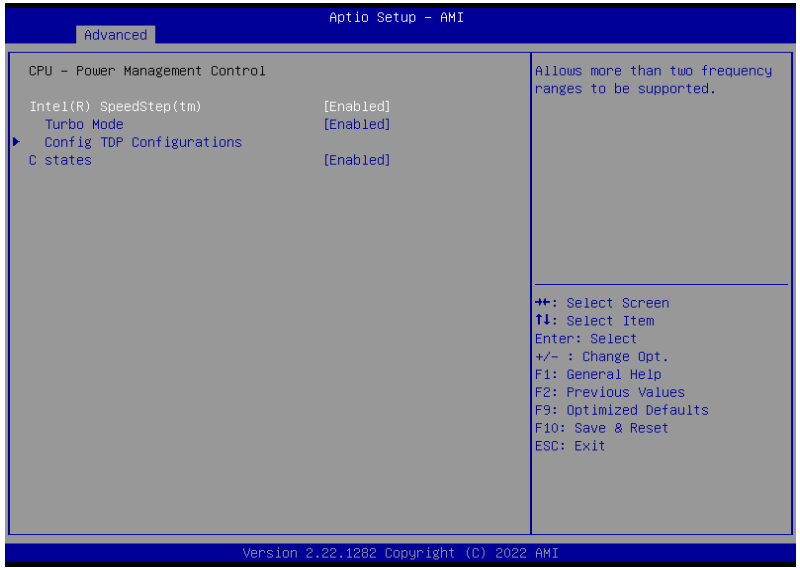
▶ Advanced

Power & Performance



▶ Advanced

Power & Performance ▶ CPU- Power Management Control



Intel (R) SpeedStep(tm)

This field is used to enable or disable the Intel SpeedStep® Technology, which helps optimize the balance between system's power consumption and performance. After it is enabled in the BIOS, EIST features can then be enabled via the operating system's power management.

Turbo Mode

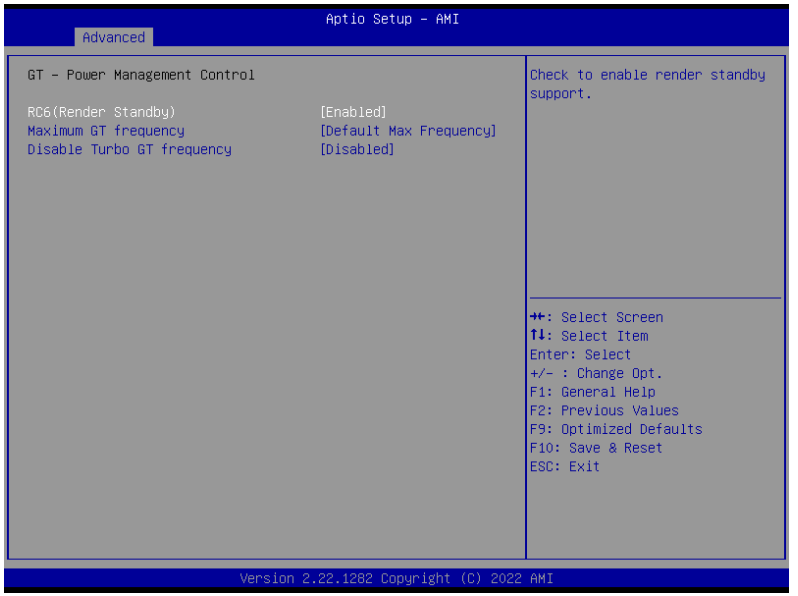
Enable or disable turbo mode of the processor. This field will only be displayed when EIST is enabled.

C states

Enable or disable CPU Power Management. It allows CPU to enter "C states" when it's not 100% utilized.

▶ Advanced

Power & Performance ▶ GT- Power Management Control



RC6 (Render Standby)

Check to enable render standby support.

Maximum GT frequency

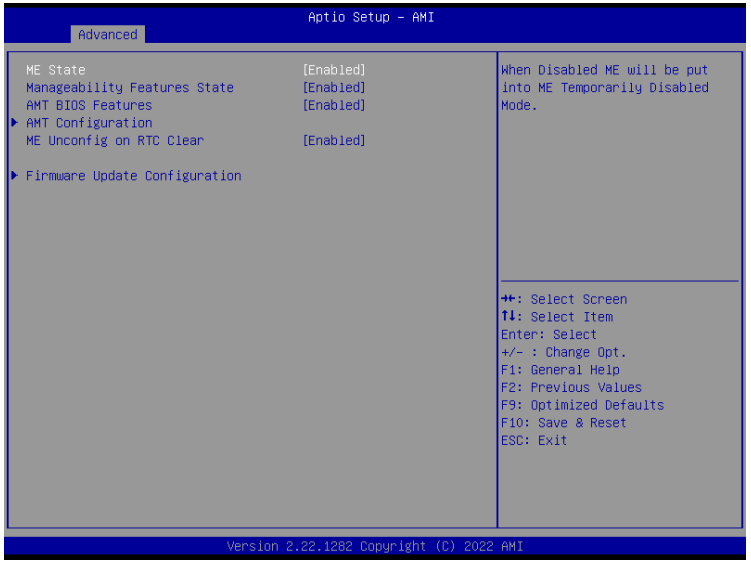
Maximum GT frequency limited by the user. Choose between 100MHz (RPN) and 1200MHZ(RPO). Value beyond the range will be clipped to min/max supported by SKU

Disable Turbo GT frequency

Enabled: Disables Turbo GT frequency. Disabled: GT frequency is not limited

▶ Advanced

PCH-FW Configuration



ME State
Enable or disable Management Engine. When this field is set to Disabled, ME will be put into ME Temporarily Disabled Mode. The following fields will only appear when ME State is enabled.

Manageability Features State
Enable or disable Intel(R) Manageability features. This option disables/enables Manageability Features support in FW. To disable, support platform must be in an unprovisioned state first.

AMT BIOS Features
When disabled, AMT BIOS features are no longer supported and user is no longer able to access MEBx Setup. This option does not disable manageability features in FW.

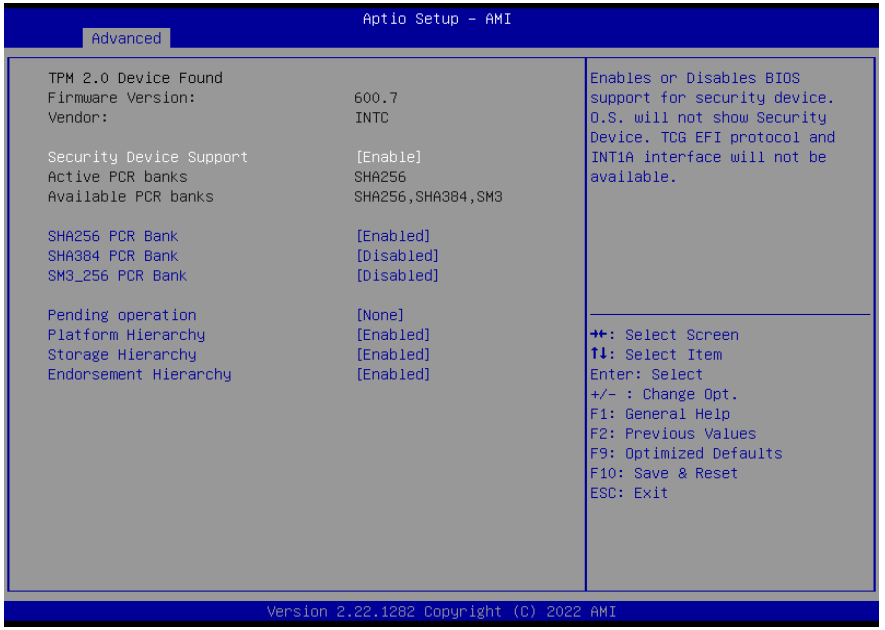
AMT Configuration
This section is used to configure Intel(R) Active Management Technology Parameters. Please refer to the following pages.

ME Unconfig on RTC Clear
When disabled, ME will not be unconfigured on RTC Clear.

Firmware Update Configuration
Please refer to the following pages.

▶ Advanced

Trusted Computing



Security Device Support

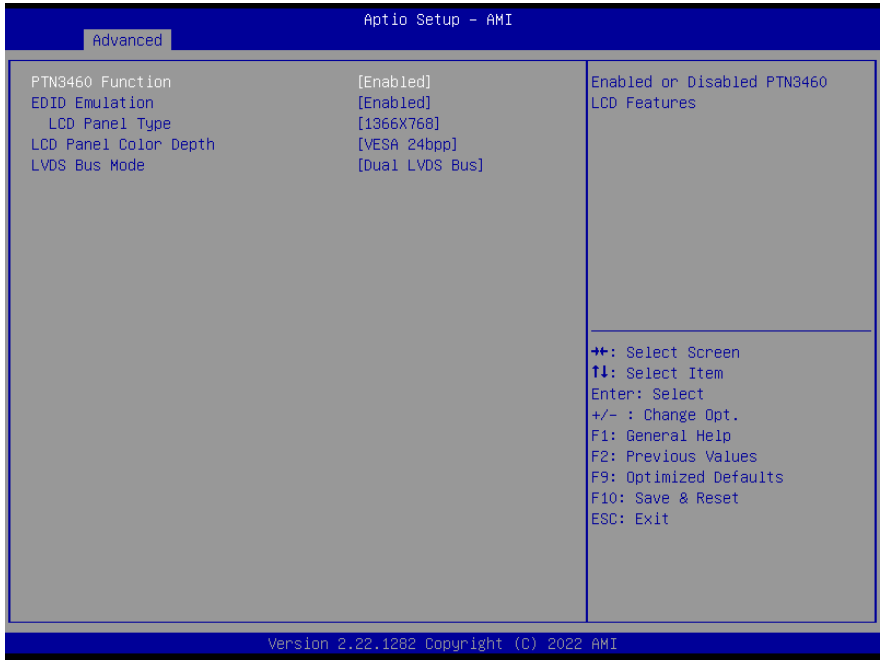
This field is used to enable or disable BIOS support for the security device such as an TPM 2.0 to achieve hardware-level security via cryptographic keys. TCG EFI protocol and INT1A interface will not be available.

Pending operation

To clear the existing TPM encryption, select "TPM Clear" and restart the system. This field is not available when "Security Device Support" is disabled. Schedule an Operation for the security Device. NOTE: Your computer will reboot during restart in order to change State of Security Device.

▶ Advanced

PTN3460 Configuration



PTN3460 Function

Enable or Disable PTN3460 LCD Features. When this field is disabled, the following fields will remain hidden.

EDID Emulation

Enable or Disable PTN3460 EDID Emulation Mode
It might cause system shutdown when disable EDID emulation with PTN3460 chip on the board.

LCD Panel Type

Select the resolution of the LCD Panel — 800X480, 800X600, 1024X768, 1366X768, 1280X1024, 1920X1080, or 1920X1200.

LCD Panel Color Depth

Select the color depth of the LCD Panel — VESA 24bpp, JEIDA 24bpp, VESA and JEIDA 18 bpp.

LVDS Bus Mode

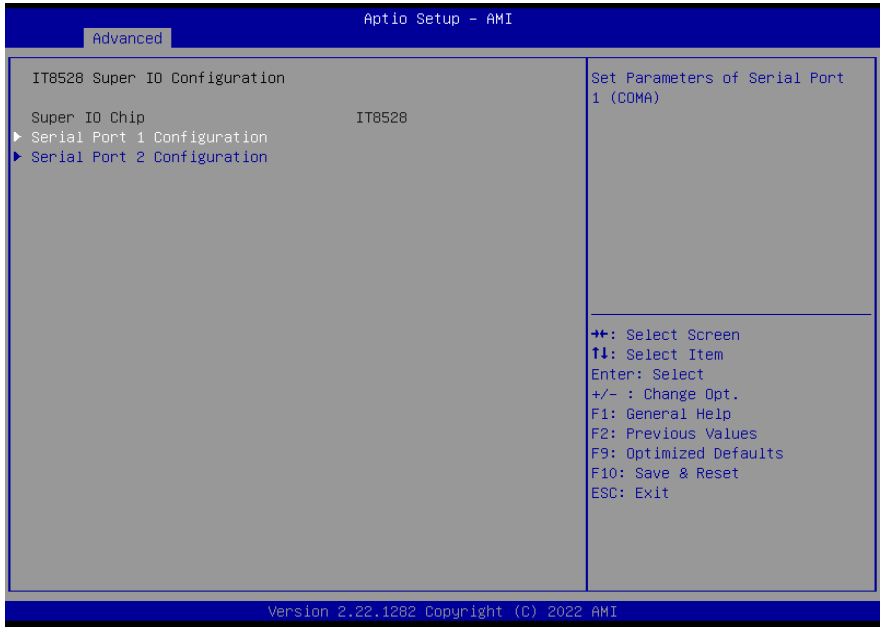
Select PTN3460 LVDS BUS Mode — Single LVDS Bus /Dual LVDS Bus

Note:
The configuration must match the specifications of your LCD Panel in order for the LCD Panel to display properly.

Note:
It might cause system hang-up when disable EDID emulation with PTN3460 chip on the board.

▶ Advanced

IT8528 Super IO Configuration



Serial Port 1 Configuration

Set Parameters of Serial Port 1 (COMA)

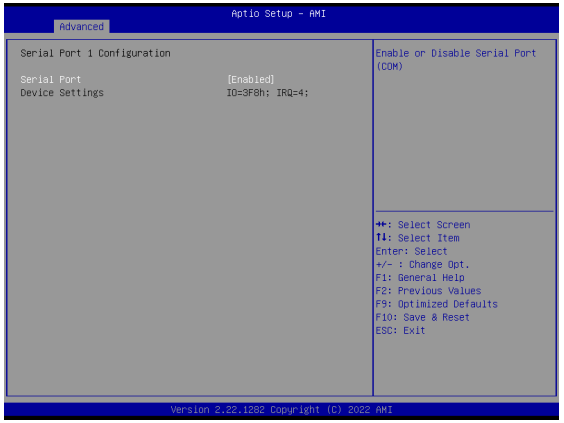
Serial Port 2 Configuration

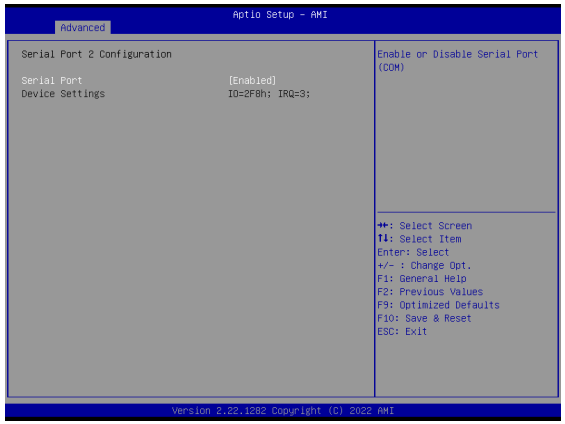
Set Parameters of Serial Port 2 (COMB)

Note:
The sub-menus are detailed in following sections.

▶ Advanced

IT8528 Super IO Configuration ▶ Serial Port 1, 2 Configuration

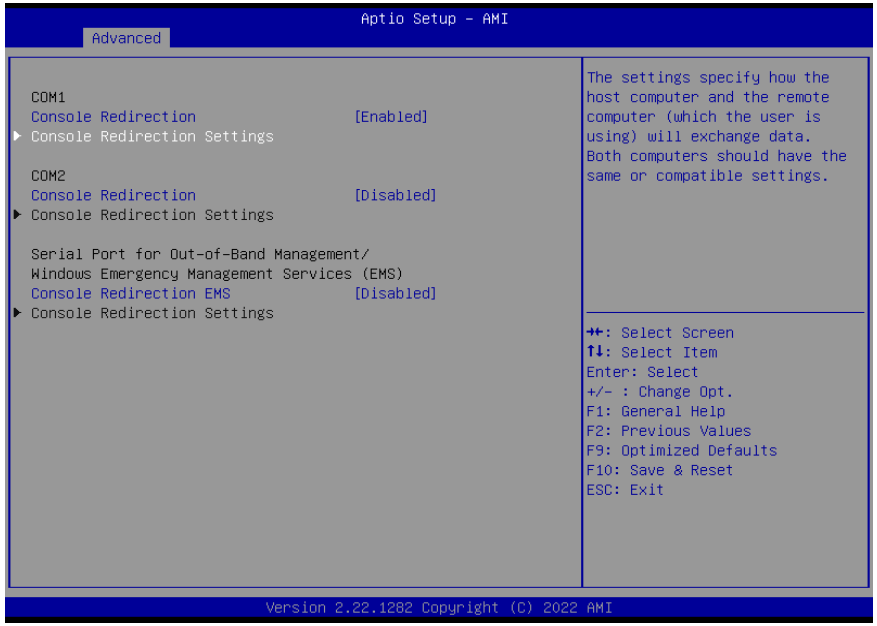




Serial Port
Enable or disable serial port.

▶ Advanced

Serial Port Console Redirection

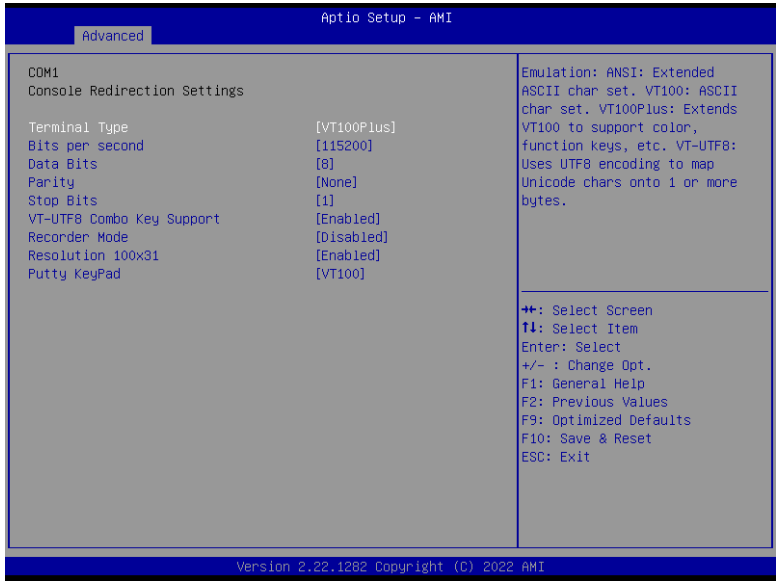


Console Redirection

By enabling Console Redirection of a COM port, the sub-menu of console redirection settings will become available for configuration as detailed in the following.

▶ Advanced

Serial Port Console Redirection ▶ Console Redirection Settings



Configure the serial settings of the current COM port.

Terminal Type

Select terminal type: VT100, VT100+, VT-UTF8 or ANSI.

Bits per second

Select serial port transmission speed: 9600, 19200, 38400, 57600 or 115200.

Data Bits

Select data bits: 7 bits or 8 bits.

Parity

Select parity bits: None, Even, Odd, Mark or Space.

Stop Bits

Select stop bits: 1 bit or 2 bits.

VT-UTF8 Combo Key Support

Enable or disable VT-UTF8 Combination Key Support for ANSI/VT100 terminals.

Recorder Mode

With this mode enabled only text will be sent. This is to capture Terminal data.

Resolution 100x31

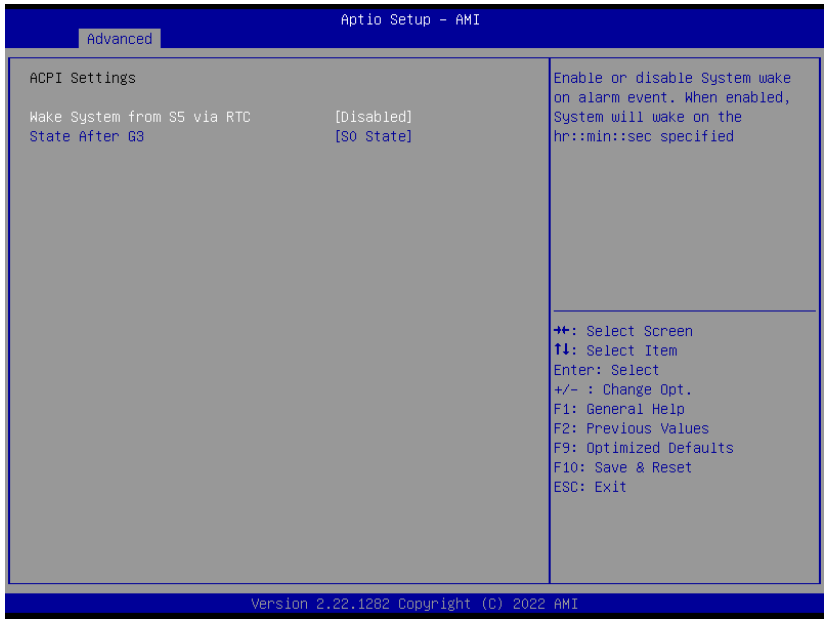
Enables or disables extended terminal resolution.

Putty Keypad

Select FunctionKey and KeyPad on Putty.

- VT100
- LINUX
- XTERMR6
- SCO
- ESCN
- VT400

ACPI Settings



Wake system from S5 via RTC

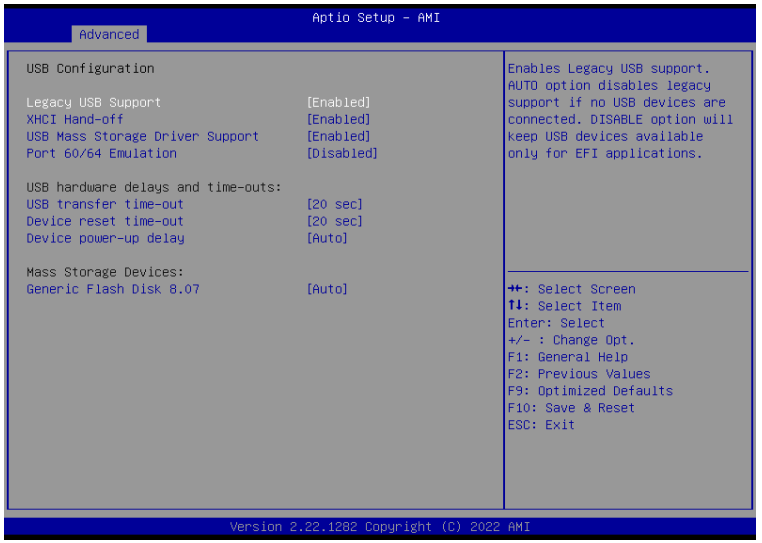
When Enabled, the system will automatically power up at a designated time every day. Once it's switched to [Enabled], please set up the time of day — hour, minute, and second — for the system to wake up.

State After G3

Select between S0 State, and S5 State. This field is used to specify what state the system is set to return to when power is re-applied after a power failure (G3 state).

- **S0 State** The system automatically powers on after power failure.
- **S5 State** The system enter soft-off state after power failure. Power-on signal input is required to power up the system.
- **Last State** The system returns to the last state right before power failure.

USB Configuration



Legacy USB Support

- **Enabled** Enable Legacy USB support.
- **Disabled** Keep USB devices available only for EFI applications.
- **Auto** Disable Legacy support if no USB devices are connected.

XHCI Hand-off

Enable or disable XHCI Hand-off.
This is a workaround for OSes without XHCI hand-off support.
The XHCI ownership change should be claimed by XHCI driver.

USB Mass Storage Driver Support

Enable or disable USB Mass Storage Driver Support.

Port 60/64 Emulation

Enables I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OSes.

USB hardware delays and time-outs:

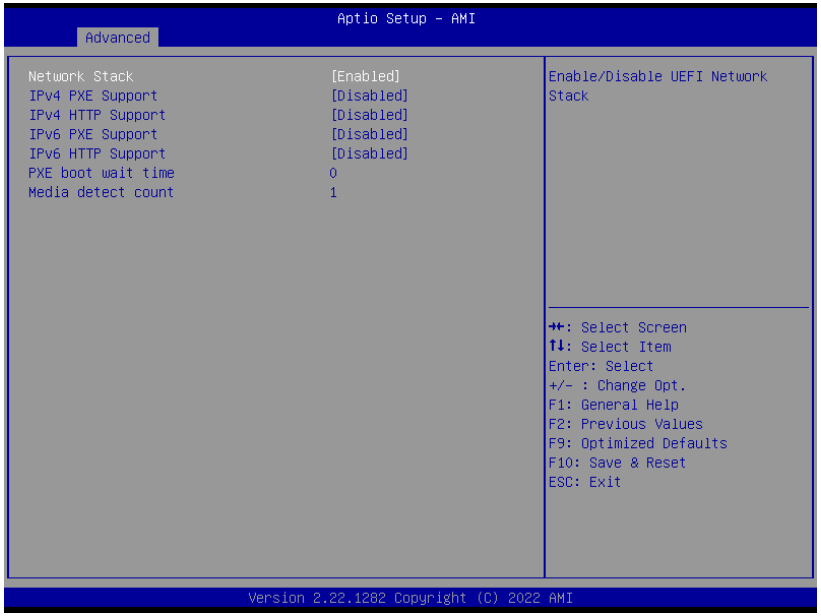
USB transfer time-out : The time-out value for Control, Bulk, and Interrupt transfers.

Device reset time-out : USB mass storage device Start Unit command time-out.

Device power-up delay : Maximum time the device will take before it properly reports itself to the Host Controller.'Auto' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.

▶ Advanced

Network Stack Configuration



Network Stack

Enable or disable UEFI network stack. The following fields will appear when this field is en-abled.

Ipv4 PXE Support

Enable or disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be avail-able.

Ipv4 HTTP Support

Enable or disable IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be avail-able.

Ipv6 PXE Support

Enable or disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be avail-able.

Ipv6 HTTP Support

Enable or disable IPv6 HTTP boot support. If disabled, IPv6 HTTP boot support will not be avail-able.

PXE boot wait time

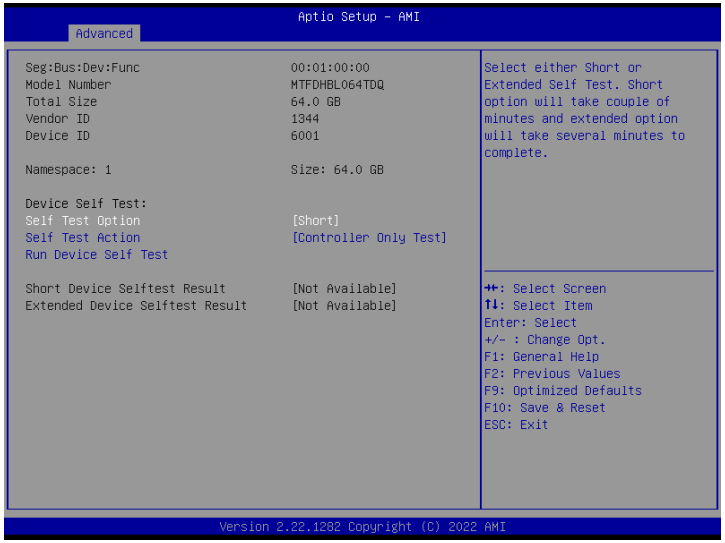
Set the wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.

Media detect count

Set the number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.

▶ Advanced

NVMe Configuration

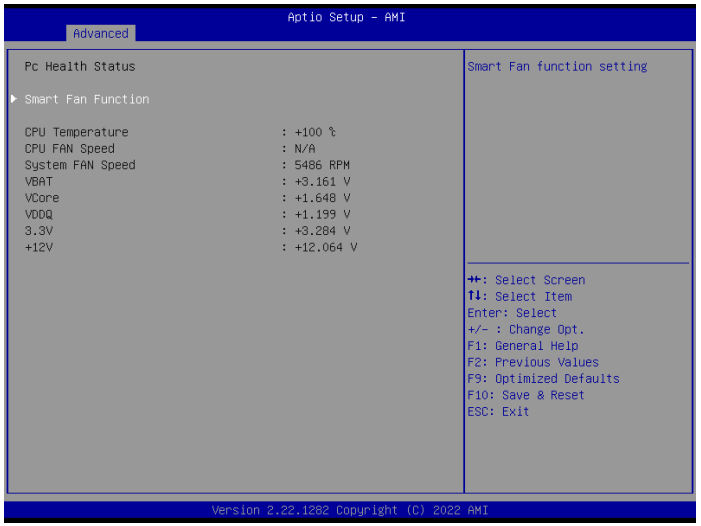


NVMe Configuration

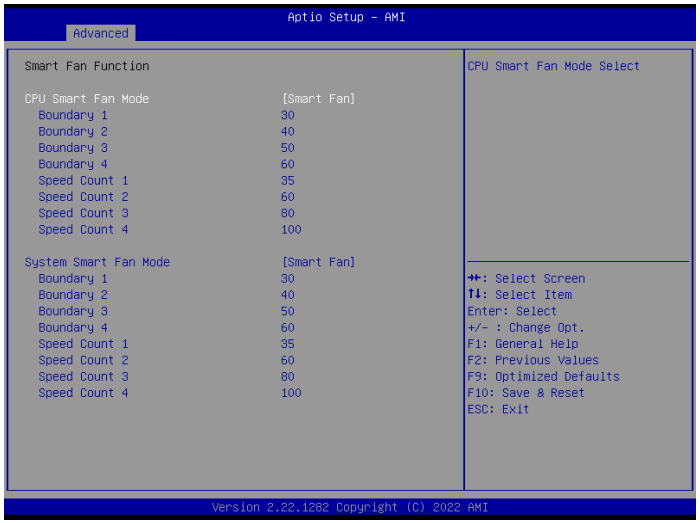
NVMe Device Options Settings

▶ Advanced

DFI EC HW Monitor



DFI EC HW Monitor ▶ Smart Fan Function



Smart Fan is a fan speed moderation strategy dependent on the current system temperature. When the system temperature goes higher than the Boundary setting, the fan speed will be turned up to the setting of the Fan Speed Count that bears the same index as the Boundary field.

▼ CPU/SYS Smart Fan Mode = [Smart Fan]

Boundary 1 to Boundary 4

Set the boundary temperatures that determine the fan speeds accordingly, the value ranging from 0-127℃. For example, when the system temperature reaches Boundary 1 setting, the fan speed will be turned up to the designated speed of the Fan Speed Count 1 field.

Fan Speed Count 1 to Fan Speed Count 4

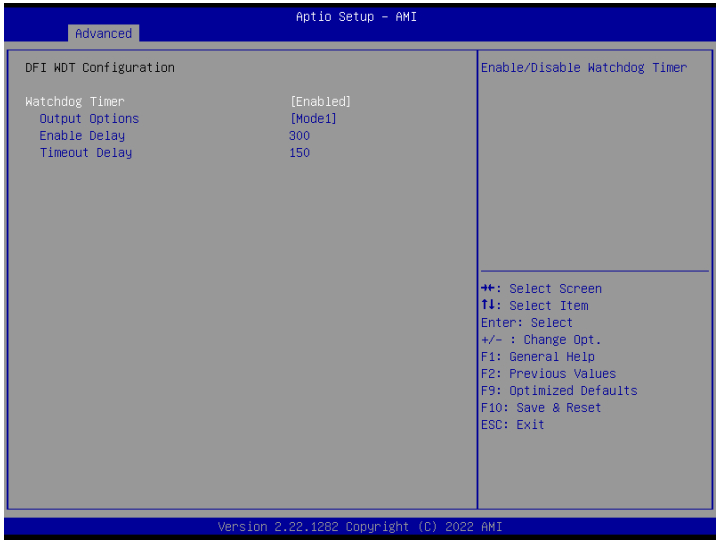
Set the fan speed, the value ranging from 1-100%, 100% being full speed. The fans will operate according to the specified boundary temperatures above-mentioned.

▼ CPU/SYS Smart Fan Mode = [Manual Mode]

Fix Fan Speed Count

Set the fan speed, the value ranging from 1-100%, 100% being full speed. The fans will always operate at the specified speed regardless of gauged temperatures.

DFI WDT Configuration



Watchdog Timer

Enable or disable watchdog timer.

Output Options

Mode1 = A Watchdog timeout causes the system to be reset.
Mode2 = WDT pin goes high upon timeout of the watchdog timer.
Mode3 = Generate NMI upon timeout of the watchdog timer.

Enable Delay

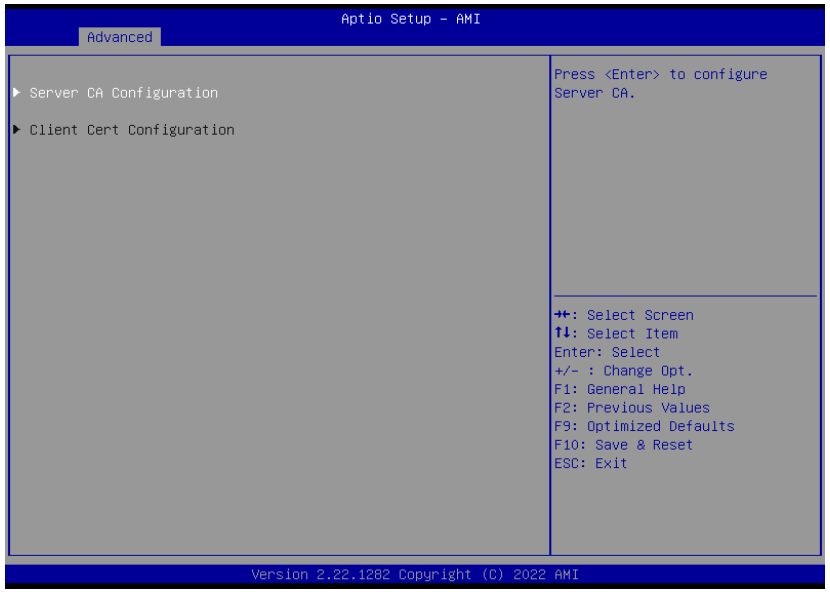
The enable delay allows time for the OS to boot and the application to load and initialize. The unit is 1 sec.

Timeout Delay

The timeout delay allows time for period of the watchdog timer. The unit is 0.1 sec.

▶ Advanced

Tls Auth Configuration



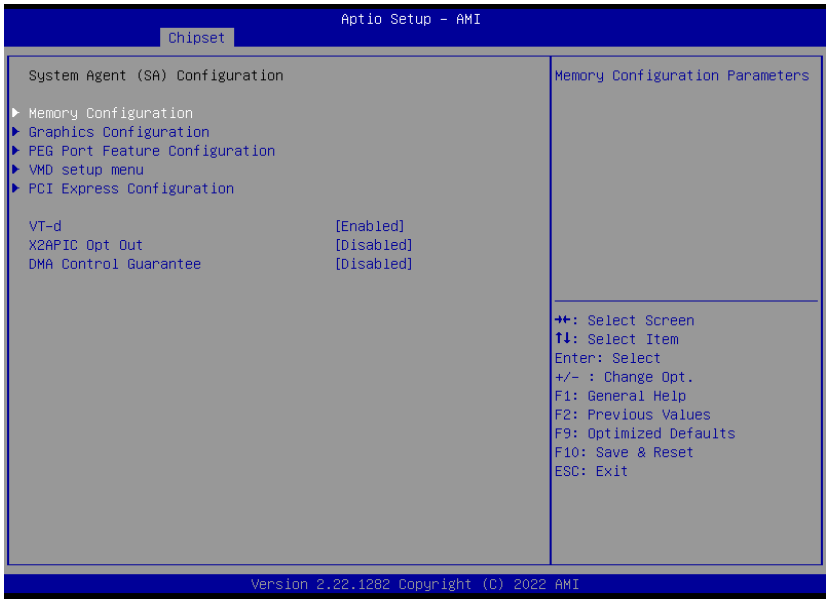
Server CA Configuration

Press <Enter> to configure Server CA.

▶ Chipset

Please select a submenu and press Enter. The submenus are detailed in the following pages.

System Agnet (SA) Configuration



Memory Configuration
Memory Configuration Parameter.

Graphics Configuration
Settings about graphic.

VMD setup menu
VMD Configuration Settings

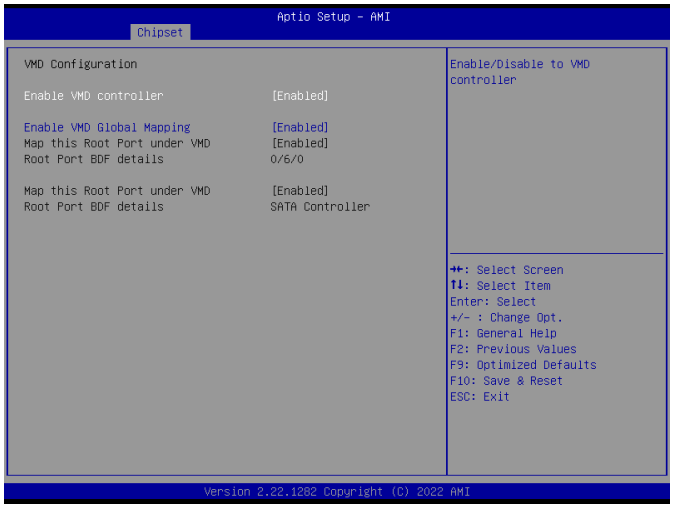
PCI Express Configuration :

VT-d
VT-d capability.

X2APIC Opt Out
Enable/Disable X2APIC_OPT_OUT bit

DMA Control Guarantee
Enable/Disable DMA_Control_Guarantee bit

System Agnet (SA) Configuration► VMD Setup Menu



Enable VMD Controller
Enable/Disable to VMD controller.

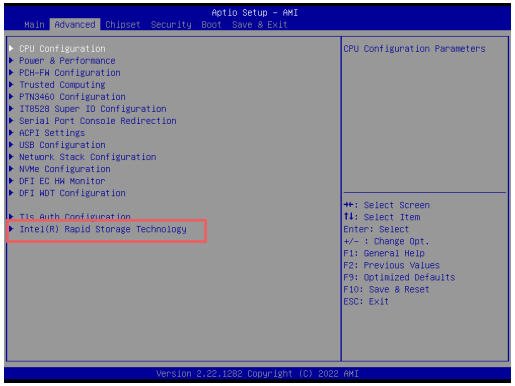
Enable VMD Global Mapping
Enable/Disable to Enable VMD Global Mapping.

Intel® Rapid Storage Technology

Step 1. Go to【**Chipset**】--->【**System Agnet (SA) Configuration► VMD Setup Menu**】to enable VMD Global Mapping

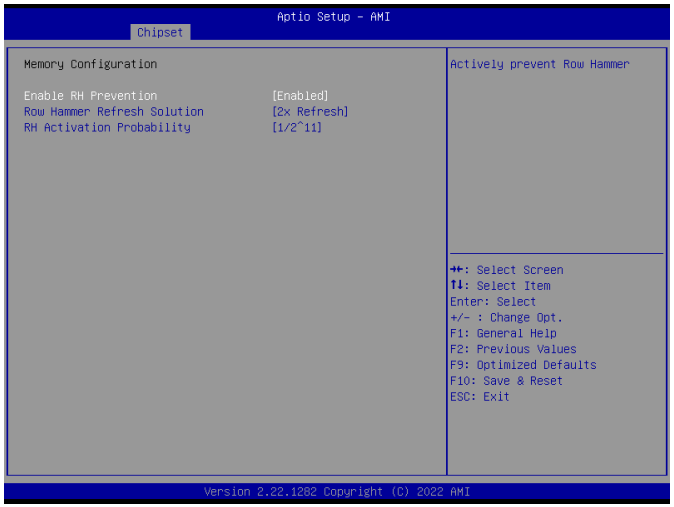
Step 2. Go to【**Save & Exit**】to save the setting and restart BIOS

Step 3. Go to【**Advanced**】and locate 【**Intel® Rapid Storage Technology** 】



Note:
Intel® Rapid Storage Technology will appear in **Advanced** menu when enabled VMD global mapping.

System Agnet (SA) Configuration▶ Memory Configuration

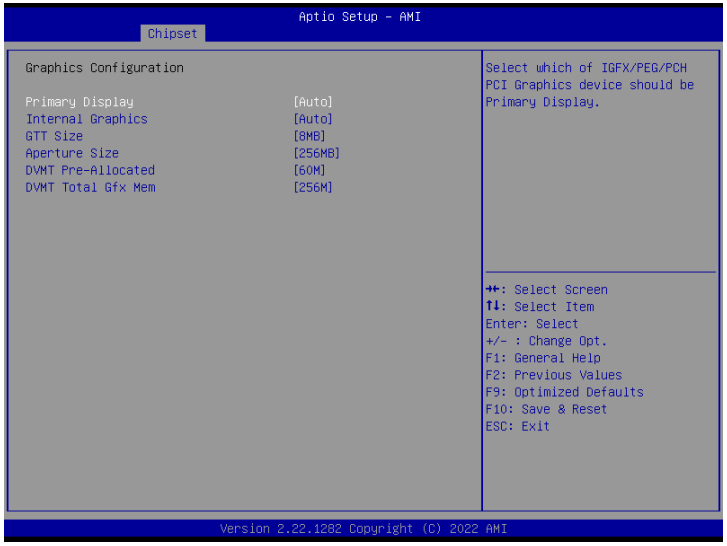


Enable RH Prevention
Actively prevent Row Hammer.

Row Hammer Refresh Solution
Type of Refresh Rate used to prevent Row Hammer: 2x Refresh, 4x Refresh or NORMAL Refresh.

RH Activation Probability
Used to adjust MC for Hardware RHP, select between: 1/2^1 ~ 1/2^15

System Agnet (SA) Configuration▶ Graphics Configuration



Primary Display
Select which of IGFX/PEG/PCH PCI Graphics device should be Primary Display.

Internal Graphics
Keep IGFX enabled based on the setup options.

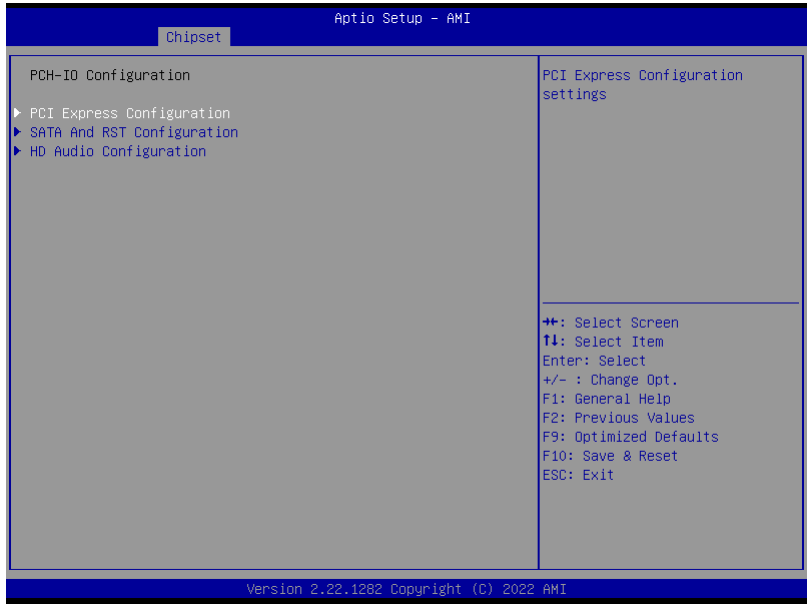
GTT Size
Select the GTT Size.

Aperture Size
Select the Aperture Size. Note : Above 4GB MMIO BIOS assignment is automatically enabled when selecting 2048MB aperture. To use this feature, please disable CSM Support.

DVMT Pre-Allocated
Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.

DVMT Total Gfx Mem
Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device.

PCH-IO Configuration



PCI Express Configuration

PCI Express Configuration Settings

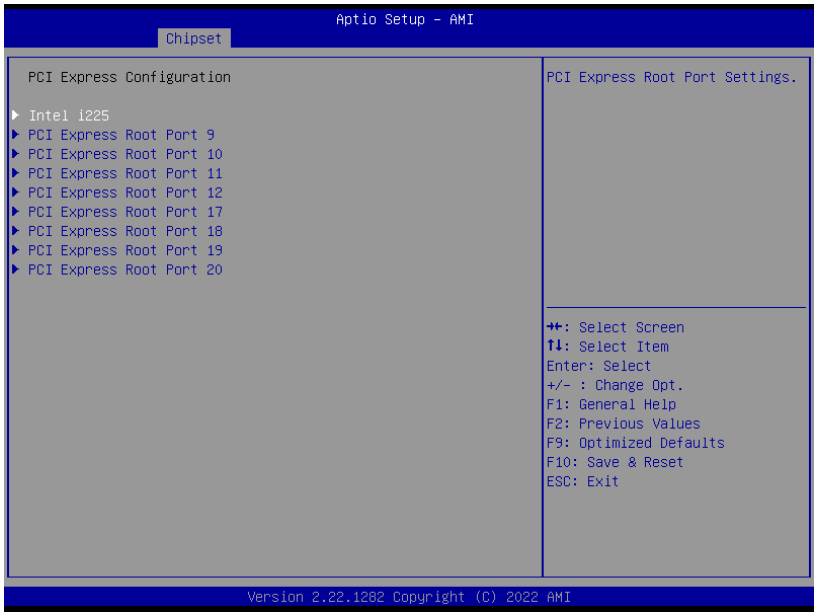
SATA And RST Configuration

SATA Device Otpions Settings

HD Audio Configuration

HD Audio Subsystem Configuration Settings

PCH-IO Configuration▶ PCI Express Configuration



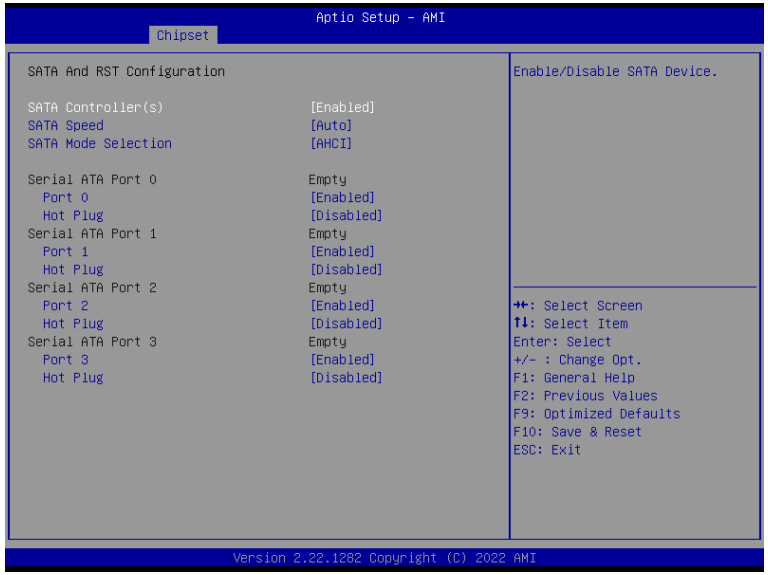
Select one of the PCI Express channels and press enter to configure the following settings.

PCI Express Root Port 9~12, 17~20 & Intel i225

Control the PCI Express Root Port.

▶ Chipset

PCH-IO Configuration▶ SATA And RST Configuration



SATA Controller(s)

This field is used to enable or disable the Serial ATA controller.

SATA Speed

This field is used to select SATA speed generation limit: Auto, Gen1, Gen2 or Gen3.

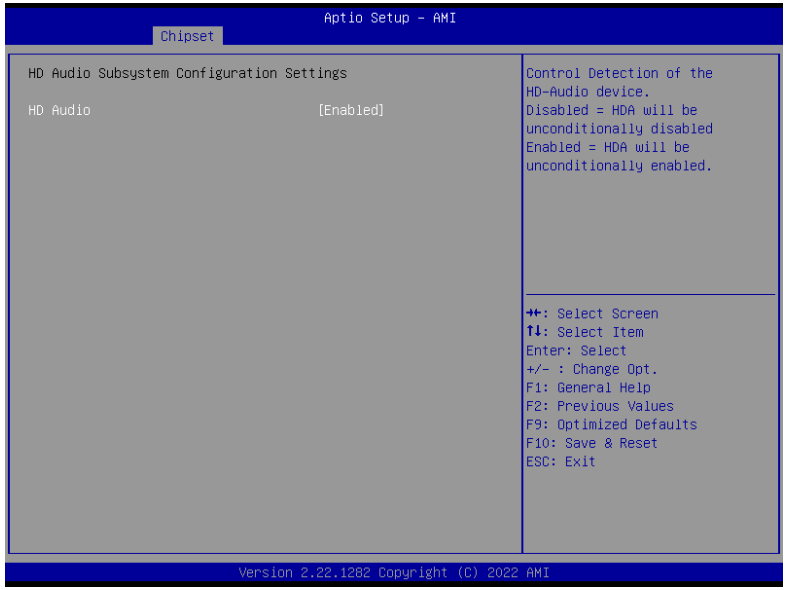
SATA Mode Selection

The mode selection determines how the SATA controller(s) operates.

- **AHCI** This option allows the Serial ATA controller(s) to use AHCI (Advanced Host Controller Interface).

▶ Chipset

PCH-IO Configuration▶ HD Audio Configuration

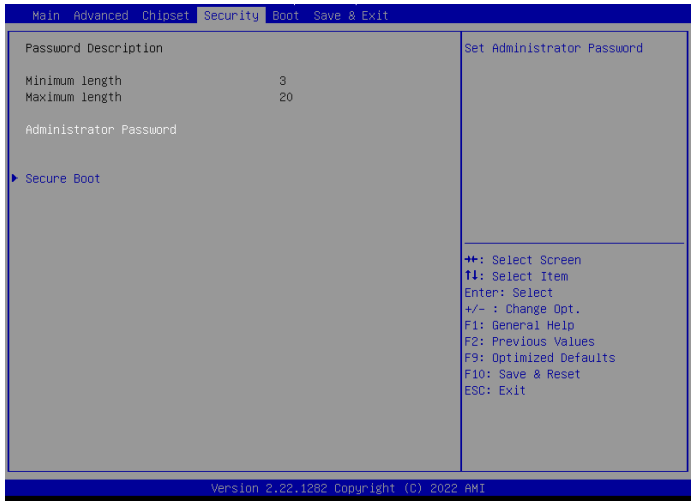


HD Audio

Control the detection of the HD Audio device.

- **Disabled** HDA will be unconditionally disabled.
- **Enabled** HDA will be unconditionally enabled.

▶ Security



Administrator Password

Set the administrator password. To clear the password, input nothing and press enter when a new password is asked. Administrator Password will be required when entering the BIOS.

User Password

Set the user password. To clear the password, input nothing and press enter when a new password is asked. User Password will be required when powering up the system.

▶ Security

Secure Boot

The Secure Boot store a database of certificates in the firmware and only allows the OSes with authorized signatures to boot on the system. To activate Secure Boot, please make sure that “Secure Boot” is “[Enabled]”, Platform Key (PK) is enrolled, “System Mode” is “User”, and CSM is disabled. After enabling/disabling Secure Boot, please save the configuration and restart the system. When configured and activated correctly, the Secure Boot status will be “Active”.

Secure Boot Mode

Select the secure boot mode — Standard or Custom. When set to Custom, the following fields will be configurable for the user to manually modify the key database.

Restore Factory Keys

Force system to User Mode. Load OEM-defined factory defaults of keys and databases onto the Secure Boot. Press Enter and a prompt will show up for you to confirm.

Reset To Setup Mode

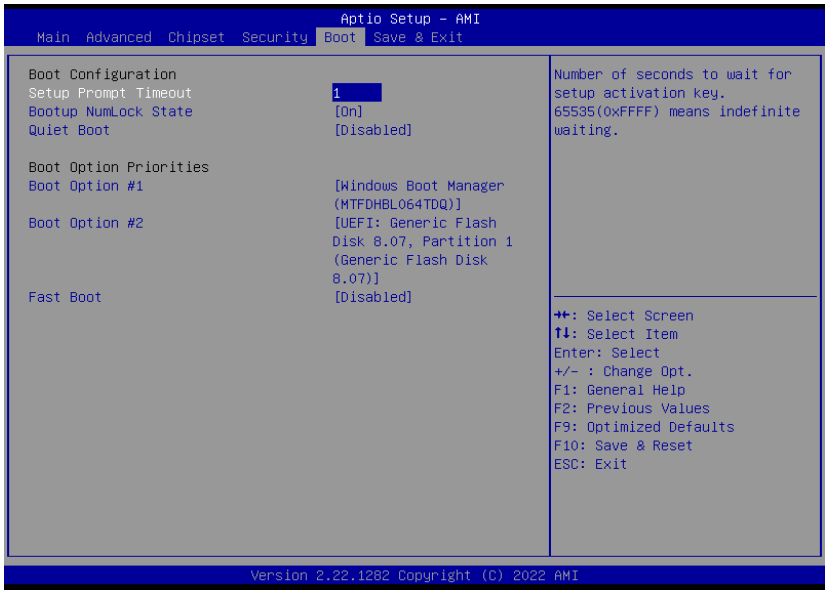
Clear the database from the NVRAM, including all the keys and signatures installed in the Key Management menu. Press Enter and a prompt will show up for you to confirm.

Key Management

Enables expert users to modify Secure Boot Policy variables

without full authentication.

▶ Boot



Setup Prompt Timeout

Set the number of seconds to wait for the setup activation key. 65535 (0xFFFF) denotes indefinite waiting.

Bootup NumLock State

Select the keyboard NumLock state: On or Off.

Quiet Boot

This section is used to enable or disable quiet boot option.

Boot Option Priorities

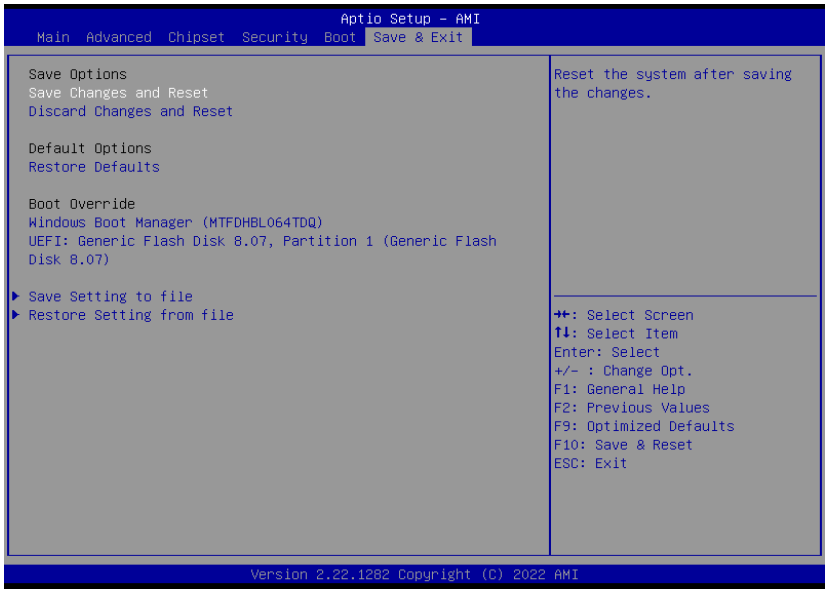
Rearrange the system boot order of available boot devices.

Fast Boot

Enables or disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.

Note:
If “Boot option filter” of “CSM Configuration” is set to “UEFI and Legacy” or “UEFI only”, and “Quiet Boot” is set to enabled, “BGRT Logo” will show up for configuration. Refer to the Advanced > CSM Configuration submenu for more information.

▶ Save & Exit



Save Changes and Reset

To save the changes, select this field and then press <Enter>. A dialog box will appear. Select Yes to reset the system after saving all changes made.

Discard Changes and Reset

To discard the changes, select this field and then press <Enter>. A dialog box will appear. Select Yes to reset the system setup without saving any changes.

Restore Defaults

To restore and load the optimized default values, select this field and then press <Enter>. A dia-log box will appear. Select Yes to restore the default values of all the setup options.

Boot Override

Move the cursor to an available boot device and press Enter, and then the system will immediately boot from the selected boot device. The Boot Override function will only be effective for the current boot. The “Boot Option Priorities” configured in the Boot menu will not be changed.

- **Save Setting to file** Select this option to save BIOS configuration settings to a USB flash device.
- **Restore Setting from file** This field will appear only when a USB flash device is detected. Select this field to restore set-ting from the USB flash device.