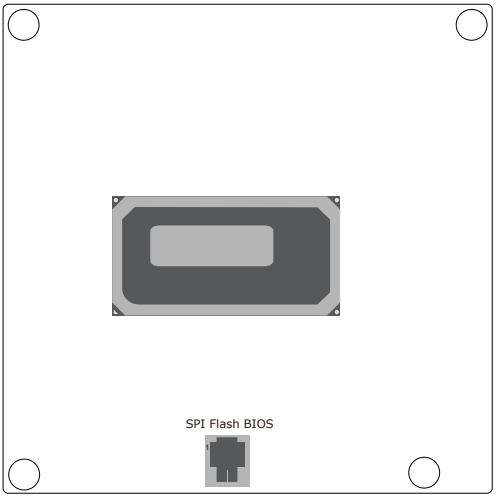
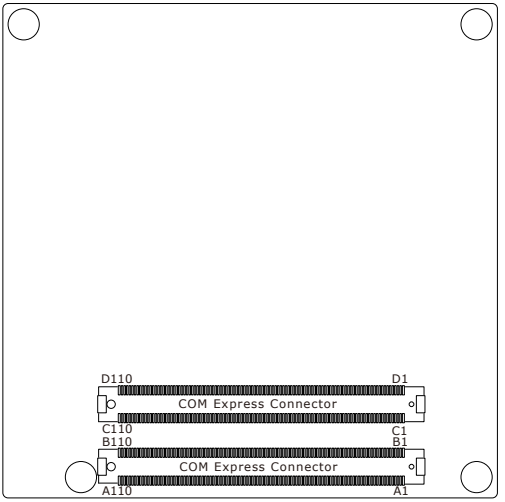
Board Layout and COM Express Pin Assignments

TOP



BOTTOM



▶ COM Express Pin Assignments

Pin List for Pin-Out Type 6

The table below is a comprehensive list of all signal pins supported on the dual 220-pin COM Express connectors as defined for Type 6 in the PICMG COM.0 R3.1 specification.

Pin	Row A	MTH966 Difference	Row B	MTH966 Difference
1	GND (FIXED)		GND (FIXED)	
2	GBE0_MDI3-		GBE0_ACT#	
3	GBE0_MDI3+		LPC_FRAME#/ESPI_CS0#	LPC_FRAME# *Note1
4	GBE0_LINKMID#	GBE_LED1000#	LPC_AD0/ESPI_IO_0	LPC_AD0 *Note1
5	GBE0_LINKMAX#	GBE_LED2500#	LPC_AD1/ESPI_IO_1	LPC_AD1 *Note1
6	GBE0_MDI2-		LPC_AD2/ESPI_IO_2	LPC_AD2 *Note1
7	GBE0_MDI2+		LPC_AD3/ESPI_IO_3	LPC_AD3 *Note1
8	GBE0_LINK#		LPC_DRQ0#/ESPI_ ALERT0#	LPC_DRQ0# *Note1
9	GBE0_MDI1-		LPC_DRQ1#/ESPI_ ALERT1#	LPC_DRQ1# *Note1
10	GBE0_MDI1+		LPC_CLK/ESPI_CK	LPC_CLK *Note1
11	GND (FIXED)		GND (FIXED)	
12	GBE0_MDI0-		PWRBTN#	
13	GBE0_MDI0+		SMB_CK	
14	GBE0_CTREF	NC	SMB_DAT	
15	SUS_S3#		SMB_ALERT#	
16	SATA0_TX+		SATA1_TX+	
17	SATA0_TX-		SATA1_TX-	
18	SUS_S4#		SUS_STAT#/ESPI_RESET#	NC *Note1
19	SATA0_RX+		SATA1_RX+	
20	SATA0_RX-		SATA1_RX-	
21	GND (FIXED)		GND (FIXED)	
22	SATA2_TX+	NC	SATA3_TX+	NC
23	SATA2_TX-	NC	SATA3_TX-	NC
24	SUS_S5#		PWR_OK	
25	SATA2_RX+	NC	SATA3_RX+	NC
26	SATA2_RX-	NC	SATA3_RX-	NC

Pin	Row A	MTH966 Difference	Row B	MTH966 Difference
27	BATLOW#		WDT	
28	(S)ATA_ACT#		HDA_SDN2/SNDW0_CLK	HDA_SDN2 *Note2
29	HDA_SYNA		HDA_SDIN1/SNDW0_DAT	HDA_SDIN1 *Note2
30	HDA_RST#		HDA_SDIN0	
31	GND (FIXED)		GND (FIXED)	
32	HDA_BITCLK		SPKR	
33	HDA_SDOUT		I2C_CK	
34	BIOS_DIS0#/ ESPI_SAFS	BIOS_DIS0# *Note1	I2C_DAT	
35	THRMTRIP#		THRM#	
36	USB6-		USB7-	
37	USB6+		USB7+	
38	USB_6_7_OC#	USBOC_4567#	USB_4_5_OC#	USBOC_4567#
39	USB4-		USB5-	
40	USB4+		USB5+	
41	GND (FIXED)		GND (FIXED)	
42	USB2-		USB3-	
43	USB2+		USB3+	
44	USB_2_3_OC#		USB_0_1_OC#	
45	USB0-		USB1-	
46	USB0+		USB1+	
47	VCC_RTC		ESPI_EN#	PU 47Kohm to 1V8SB
48	RSMRST_OUT#		USB0_HOST_PRSNT	PD 47Kohm
49	GBE0_SDP	*Note1	SYS_RESET#	
50	LPC_SERIRQ		CB_RESET#	
51	GND (FIXED)		GND (FIXED)	
52	PCIE_TX5+		PCIE_RX5+	
53	PCIE_TX5-		PCIE_RX5-	
54	GPI0/SD_DATA0	GPI0 *Note3	GPO1/SD_CMD	GPO1 *Note3
55	PCIE_TX4+		PCIE_RX4+	
56	PCIE_TX4-		PCIE_RX4-	

Pin	Row A	MTH966 Difference	Row B	MTH966 Difference
57	GND		GPO2/SD_WP	GPO2 *Note3
58	PCIE_TX3+		PCIE_RX3+	
59	PCIE_TX3-		PCIE_RX3-	
60	GND (FIXED)		GND(FIXED)	
61	PCIE_TX2+		PCIE_RX2+	
62	PCIE_TX2-		PCIE_RX2-	
63	GPI1/SD_DATA1	GPI1 *Note3	GPO3/SD_CD#	GPO3 *Note3
64	PCIE_TX1+		PCIE_RX1+	
65	PCIE_TX1-		PCIE_RX1-	
66	GND		WAKE0#	
67	GPI2/SD_DATA2	GPI2 *Note3	WAKE1#	
68	PCIE_TX0+		PCIE_RX0+	
69	PCIE_TX0-		PCIE_RX0-	
70	GND (FIXED)		GND(FIXED)	
71	LVDS_A0+/eDP_TX2+	LVDS_A0+ *Note4	LVDS_B0+	
72	LVDS_A0-/eDP_TX2-	LVDS_A0- *Note4	LVDS_B0-	
73	LVDS_A1+/eDP_TX1+	LVDS_A1+ *Note4	LVDS_B1+	
74	LVDS_A1-/eDP_TX1-	LVDS_A1- *Note4	LVDS_B1-	
75	LVDS_A2+/eDP_TX0+	LVDS_A2+ *Note4	LVDS_B2+	
76	LVDS_A2-/eDP_TX0-	LVDS_A2- *Note4	LVDS_B2-	
77	LVDS_VDD_EN/ eDP_ VDD_EN	LVDS_VDD_EN *Note4	LVDS_B3+	
78	LVDS_A3+		LVDS_B3-	
79	LVDS_A3-		LVDS_BKLT_EN/ eDP_BKLT_EN **	LVDS_BKLT_EN *Note4
80	GND (FIXED)		GND(FIXED)	
81	LVDS_A_CK+/ eDP_TX3+	LVDS_A_CK+ *Note4	LVDS_B_CK+	
82	LVDS_A_CK-/ eDP_TX3-	LVDS_A_CK- *Note4	LVDS_B_CK-	
83	LVDS_I2C_CK/ eDP_AUX+		LVDS_BKLT_CTRL/ eDP_BKLT_CTRL	LVDS_BKLT_CTRL *Note4
84	LVDS_I2C_DAT/ eDP_ AUX-	LVDS_I2C_DAT *Note4	VCC_5V_SBY	
85	GPI3/SD_DATA3	GPI3 *Note3	VCC_5V_SBY	
86	GP_SPI_MOSI		VCC_5V_SBY	
87	eDP_HPD	*Note4	VCC_5V_SBY	

Pin	Row A	MTH966 Difference	Row B	MTH966 Difference
88	PCIE_CLK_REF+		BIOS_DIS1#	
89	PCIE_CLK_REF-		VGA_RED	NC
90	GND(FIXED)		GND(FIXED)	
91	SPI_POWER		VGA_GRN	NC
92	SPI_MISO	GPO0 *Note3	VGA_BLU	NC
93	GPO0/SD_CLK		VGA_HSYNA	NC
94	SPI_CLK		VGA_VSYNA	NC
95	SPI_MOSI		VGA_I2C_CK	NC
96	TPM_PP		VGA_I2C_DAT	NC
97	TYPE10#	NC	SPI_CS#	
98	SER0_TX		GP_SPI_MISO	
99	SER0_RX		GP_SPI_CK	
100	GND (FIXED)		GND (FIXED)	
101	SER1_TX/CAN0_TX	SER1_TX *Note5	FAN_PWMOUT	
102	SER1_RX/CAN0_RX	SER1_RX *Note5	FAN_TACHIN	
103	LID#		SLEEP#	
104	VCC_12V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
105	VCC_12V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
106	VCC_12V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
107	VCC_12V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
108	VCC_12V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
109	VCC_V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
110	GND (FIXED)		GND (FIXED)	

Note:

1. Th eAPI is BOM option supported by project basis.
2. The SoundWire function is not supported. The Pin B28 is reserved for PCIE_CLK_REQ function.
3. The SDIO function is not supported.
4. The eDP (in place of LVDS) is BOM option supported by project basis.
5. The CAN function (in place of SER) is BOM option supported by project basis.
6. For PCIe device down components on the carrier board, please use and place on the PCIe Lane0 port first.

Pin	Row C	MTH966 Difference	Row D	MTH966 Difference
1	GND (FIXED)		GND (FIXED)	
2	GND		GND	
3	USB_SSRX0-		USB_SSTX0-	
4	USB_SSRX0+		USB_SSTX0+	
5	GND		GND	
6	USB_SSRX1-		USB_SSTX1-	
7	USB_SSRX1+		USB_SSTX1+	
8	GND		GND	
9	USB_SSRX2-		USB_SSTX2-	
10	USB_SSRX2+		USB_SSTX2+	
11	GND (FIXED)		GND (FIXED)	
12	USB_SSRX3-		USB_SSTX3-	
13	USB_SSRX3+		USB_SSTX3+	
14	GND		GND	
15	USB4_1_LSTX	NC *Note7	DDI1_CTRLCLK_AUX+/ USB4_1_AUX+	DDI1_CTRLCLK_AUX+ *Note7
16	USB4_1_LSRX	NC *Note7	DDI1_CTRLDATA_AUX-/ USB4_1_AUX-	DDI1_CTRLDATA_AUX- *Note7
17	USB4_RT_ENA	NC *Note7	USB4_PD_I2C_ALERT#	*Note7
18	GND		PMCALERT#	
19	PCIE_RX6+		PCIE_TX6+	
20	PCIE_RX6-		PCIE_TX6-	
21	GND (FIXED)		GND (FIXED)	
22	PCIE_RX7+		PCIE_TX7+	
23	PCIE_RX7-		PCIE_TX7-	
24	DDI1_HPD		GND	
25	SML0_CLK		GND	
26	SML0_DAT		DDI1_PAIR0+/ USB4_1_SSTX0+	DDI1_PAIR0+ *Note7
27	SML1_CLK		DDI1_PAIR0-/ USB4_1_SSTX0-	DDI1_PAIR0- *Note7

Note:

7. The USB4 function is BOM option supported by project basis.

Pin	Row C	MTH966 Difference	Row D	MTH966 Difference
28	SML1_DAT		GND	
29	USB4_PD_I2C_CLK	*Note7	DDI1_PAIR1+/ USB4_1_ SSRX0+	DDI1_PAIR1+ *Note7
30	USB4_PD_I2C_DAT	*Note7	DDI1_PAIR1-/ USB4_1_SSRX0-	DDI1_PAIR1- *Note7
31	GND (FIXED)		GND(FIXED)	
32	DDI2_CTRLCLK_AUX+ / USB4_2_AUX+	DDI2_CTRLC LK_AUX+ *Note7	DDI1_PAIR2+/ USB4_1_SSTX1+	DDI1_PAIR2+ *Note7
33	DDI2_CTRLDATA_AUX-/ USB4_2_AUX-	DDI2_ CTRLDATA_AUX- *Note7	DDI1_PAIR2-/ USB4_1_ SSTX1-	DDI1_PAIR2- *Note7
34	DDI2_DDC_AUX_SEL		DDI1_DDC_AUX_SEL	
35	USB4_2_LSTX	NC *Note7	USB4_2_LSRX	NC *Note7
36	DDI3_CTRLCLK_AUX+		DDI1_PAIR3+/ USB4_1_SSRX1+	DDI1_PAIR3+ *Note7
37	DDI3_CTRLDATA_AUX-		DDI1_PAIR3-/ USB4_1_SSRX1-	DDI1_PAIR3- *Note7
38	DDI3_DDC_AUX_SEL		GND	
39	DDI3_PAIR0+		DDI2_PAIR0+/ USB4_2_SSTX0+	DDI2_PAIR0+ *Note7
40	DDI3_PAIR0-		DDI2_PAIR0-/ USB4_2_SSTX0-	DDI2_PAIR0- *Note7
41	GND (FIXED)		GND(FIXED)	
42	DDI3_PAIR1+		DDI2_PAIR1+/ USB4_2_SSRX0+	DDI2_PAIR1+ *Note7
43	DDI3_PAIR1-		DDI2_PAIR1-/ USB4_2_SSRX0-	DDI2_PAIR1- *Note7
44	DDI3_HPD		DDI2_HPD	
45	GP_SPI_CS#		GND	
46	DDI3_PAIR2+		DDI2_PAIR2+/ USB4_2_ SSTX1+	DDI2_PAIR2+ *Note7
47	DDI3_PAIR2-		DDI2_PAIR2-/ USB4_2_ SSTX1-	DDI2_PAIR2- *Note7
48	RSVD		GND	
49	DDI3_PAIR3+		DDI2_PAIR3+/ USB4_2_ SSRX1+	DDI2_PAIR3+ *Note7
50	DDI3_PAIR3-		DDI2_PAIR3-/ USB4_2_ SSRX1-	DDI2_PAIR3- *Note7
51	GND (FIXED)		GND(FIXED)	
52	PEG_RX0+		PEG_TX0+	
53	PEG_RX0-		PEG_TX0-	
54	TYPE0#	NC	PEG_LANE_RV#	
55	PEG_RX1+		PEG_TX1+	

Pin	Row C	MTH966 Difference	Row D	MTH966 Difference
56	PEG_RX1-		PEG_TX1-	
57	TYPE1#	NC	TYPE2#	GND
58	PEG_RX2+		PEG_TX2+	
59	PEG_RX2-		PEG_TX2-	
60	GND (FIXED)		GND (FIXED)	
61	PEG_RX3+		PEG_TX3+	
62	PEG_RX3-		PEG_TX3-	
63	GND		GND	
64	GND		GND	
65	PEG_RX4+	*Note8	PEG_TX4+	*Note8
66	PEG_RX4-	*Note8	PEG_TX4-	*Note8
67	RAPID_SHUTDOWN		GND	
68	PEG_RX5+	*Note8	PEG_TX5+	*Note8
69	PEG_RX5-	*Note8	PEG_TX5-	*Note8
70	GND (FIXED)		GND (FIXED)	
71	PEG_RX6+	*Note8	PEG_TX6+	*Note8
72	PEG_RX6-	*Note8	PEG_TX6-	*Note8
73	GND		GND	
74	PEG_RX7+	*Note8	PEG_TX7+	*Note8
75	PEG_RX7-	*Note8	PEG_TX7-	*Note8
76	GND		GND	
77	GND		GND	
78	PEG_RX8+	*Note9	PEG_TX8+	*Note9
79	PEG_RX8-	*Note9	PEG_TX8-	*Note9
80	GND (FIXED)		GND (FIXED)	
81	PEG_RX9+	*Note9	PEG_TX9+	*Note9
82	PEG_RX9-	*Note9	PEG_TX9-	*Note9

Note:

8. The onboard NVME SSD (in place of PEG) is BOM option supported by project basis.
9. The PEG LANE 8~15 is supported by the H sku CPU only.

Pin	Row C	MTH966 Difference	Row D	MTH966 Difference
83	GND		GND	
84	GND		GND	
85	PEG_RX10+	*Note9	PEG_TX10+	*Note9
86	PEG_RX10-	*Note9	PEG_TX10-	*Note9
87	GND		GND	
88	PEG_RX11+	*Note9	PEG_TX11+	*Note9
89	PEG_RX11-	*Note9	PEG_TX11-	*Note9
90	GND (FIXED)		GND (FIXED)	
91	PEG_RX12+	*Note9	PEG_TX12+	*Note9
92	PEG_RX12-	*Note9	PEG_TX12-	*Note9
93	GND		GND	
94	PEG_RX13+	*Note9	PEG_TX13+	*Note9
95	PEG_RX13-	*Note9	PEG_TX13-	*Note9
96	GND		GND	
97	GND		GND	
98	PEG_RX14+	*Note9	PEG_TX14+	*Note9
99	PEG_RX14-	*Note9	PEG_TX14-	*Note9
100	GND (FIXED)		GND (FIXED)	
101	PEG_RX15+	*Note9	PEG_TX15+	*Note9
102	PEG_RX15-	*Note9	PEG_TX15-	*Note9
103	GND		GND	
104	VCC_12V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
105	VCC_12V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
106	VCC_12V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
107	VCC_12V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
108	VCC_12V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
109	VCC_12V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
110	GND (FIXED)		GND (FIXED)	

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