



HM920-QM87/HM86

COM Express Basic Module User's Manual

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COM Express Specification Reference

PICMG[®] COM Express Module[™] Base Specification.

http://www.picmg.org/

FCC and DOC Statement on Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio TV technician for help.

Notice:

- The changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.
- 2. Shielded interface cables must be used in order to comply with the emission limits.

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About this Manual

An electronic file of this manual is included in the CD. To view the user's manual in the CD, insert the CD into a CD-ROM drive. The autorun screen (Main Board Utility CD) will appear. Click "User's Manual" on the main menu.

Warranty

- Warranty does not cover damages or failures that arised from misuse of the product, inability to use the product, unauthorized replacement or alteration of components and product specifications.
- 2. The warranty is void if the product has been subjected to physical abuse, improper installation, modification, accidents or unauthorized repair of the product.
- Unless otherwise instructed in this user's manual, the user may not, under any circumstances, attempt to perform service, adjustments or repairs on the product, whether in or out of warranty. It must be returned to the purchase point, factory or authorized service agency for all such work.
- 4. We will not be liable for any indirect, special, incidental or consequencial damages to the product that has been modified or altered.

Static Electricity Precautions

It is quite easy to inadvertently damage your PC, system board, components or devices even before installing them in your system unit. Static electrical discharge can damage computer components without causing any signs of physical damage. You must take extra care in handling them to ensure against electrostatic build-up.

- To prevent electrostatic build-up, leave the system board in its anti-static bag until you are ready to install it.
- 2. Wear an antistatic wrist strap.
- 3. Do all preparation work on a static-free surface.
- Hold the device only by its edges. Be careful not to touch any of the components, contacts or connections.
- Avoid touching the pins or contacts on all modules and connectors. Hold modules or connectors by their ends.



Important:

Electrostatic discharge (ESD) can damage your processor, disk drive and other components. Perform the upgrade instruction procedures described at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

Safety Measures

To avoid damage to the system:

Use the correct AC input voltage range.

To reduce the risk of electric shock:

Unplug the power cord before removing the system chassis cover for installation or servicing. After installation or servicing, cover the system chassis before plugging the power cord.

About the Package

The package contains the following items. If any of these items are missing or damaged, please contact your dealer or sales representative for assistance.

- One HM920 board
- One DVD
- One QR (Quick Reference)
- Heat spreader with heat sink and fan

Optional Items

- COM330-B carrier board kit
- Heat spreader

The board and accessories in the package may not come similar to the information listed above. This may differ in accordance with the sales region or models in which it was sold. For more information about the standard package in your region, please contact your dealer or sales representative.

Before Using the System Board

Before using the system board, prepare basic system components.

If you are installing the system board in a new system, you will need at least the following internal components.

- Memory module
- Storage devices such as hard disk drive, CD-ROM, etc.

You will also need external system peripherals you intend to use which will normally include at least a keyboard, a mouse and a video display monitor.

Chapter 1 - Introduction

Specifications

Processor	HM920-QM87: • 4th generation Intel® Core™ processors 4700EQ: Intel® Core™ i7-4700EQ, 6M Cache, up to 3.4 GHz, 47W 4400E: Intel® Core™ i5-4400E, 3M Cache, up to 3.3 GHz, 37W 4402E: Intel® Core™ i5-4402E, 3M Cache, up to 2.7 GHz, 25W • BGA 1364 packaging technology • 22nm process technology HM920-HM86: • 4th generation Intel® Core™ processors 4400E: Intel® Core™ i5-4400E, 3M Cache, up to 3.3 GHz, 37W 4402E: Intel® Core™ i5-4402E, 3M Cache, up to 2.7 GHz, 25W 2000E: Intel® Celeron® 2000E, 2M Cache, 2.2 GHz, 37W 2002E: Intel® Celeron® 2002E, 2M Cache, 1.5 GHz, 25W • BGA 1364 packaging technology • 22nm process technology
Chipset	Intel® QM87 Express Chipset (HM920-QM87) Intel® HM86 Express Chipset (HM920-HM86)
System Memory	 Two 204-pin DDR3L SODIMM sockets Supports DDR3L 1333/1600MHz SODIMM Supports up to 16GB system memory DRAM device technologies: 1Gb, 2Gb and 4Gb DDR3L DRAM technologies are supported for x8 and x16 devices, unbuffered, non-ECC
Graphics	Intel® HD Graphics 4600 Supports 1 VGA and 1 LVDS VGA: resolution up to 2048x1536 @60Hz LVDS: NXP PTN3460, 24-bit, dual channel, resolution up to 1920x1200 @60Hz Intel® Clear Video Technology Intel® Advanced Vector Extensions (Intel® AVX) Instructions Supports DirectX 11.1, OpenGL 4.0, OpenCL 1.2
Audio	Supports High Definition Audio interface
LAN	 Intel® I217LM with iAMT9.0 Gigabit Ethernet Phy (HM920-QM87) Intel® I217LM Gigabit Ethernet Phy (HM920-HM86) Integrated 10/100/1000 transceiver Fully compliant with IEEE 802.3, IEEE 802.3u, IEEE 802.3ab
Serial ATA	HM920-QM87: • Supports 4 SATA 3.0 with data transfer rate up to 6Gb/s • Integrated Advanced Host Controller Interface (AHCI) controller • Supports RAID 0/1/5/10 • Supports Intel® Smart Response Technology
	HM920-HM86: • Supports 2 SATA 3.0, 2 SATA 2.0 • Supports 2 SATA 3.0, 1 SATA 2.0, and 1 SSD* (optional) • Integrated Advanced Host Controller Interface (AHCI) controller
SSD* (optional)	2GB/4GB/8GB/16GB/32GB/64GBWrite: 30MB/sec (max), Read: 70MB/sec (max)SATA to SSD onboard
Trusted Platform Module - TPM* (optional)	 Provides a Trusted PC for secure transactions Provides software license protection, enforcement and password protection

Expansion Interfaces	 Supports 8 USB 2.0 interfaces Supports 1 PCIe x16 Gen 3 interface Supports 5 PCIe x1 interfaces Supports 4 PCI interfaces (PCI 2.3) Supports LPC interface Supports SMBus interface Supports 1²C interface Supports IDE interface Supports 4-bit input and 4-bit output GPIO
IDE Interface	Supports one IDE device DMA mode: Ultra ATA up to 100MB/s PIO mode: up to 16MB/s
Intel® Active Management Technology - AMT (HM920-QM87)	 Supports iAMT9.0 Out-of-band system access Remote troubleshooting and recovery Hardware-based agent presence checking Proactive alerting Remote hardware and software asset tracking
Damage Free Intelligence	 Monitors CPU temperature and overheat alarm Monitors CPU fan speed and failure alarm Monitors Vcore/1.05V/DDR voltages and failure alarm
BIOS	• AMI BIOS - 64Mbit SPI BIOS
WatchDog Timer	Software programmable from 1 to 255 seconds
OS Support	 Windows XP Professional x86 & SP3 (32-bit) (limited function) Windows 7 Ultimate x86 & SP1 (32-bit) Windows 7 Ultimate x64 & SP1 (64-bit) Windows 8 Enterprise x86 (32-bit) Windows 8 Enterprise x64 (64-bit)
Temperature	• Operating: 0°C to 60°C • Storage: -20°C to 85°C
Humidity	• 5% to 90%
Power	• Input: 12V, VCC_RTC, 5VSB* (optional)
Power Consumption	\bullet HM920-HM86BS0-4100E: 37.62W with i3-4100E at 2.4GHz and 1x 4GB DDR3L SODIMM
PCB	Dimensions COM Express® Basic Somm (3.74") x 125mm (4.9") Compliance PICMG COM Express® R2.1, Type 2



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Note:*Optional and is not supported in standard model. Please contact your sales representative for more information.

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Chapter 1 Introduction

Features

Watchdog Timer

The Watchdog Timer function allows your application to regularly "clear" the system at the set time interval. If the system hangs or fails to function, it will reset at the set time interval so that your system will continue to operate.

• DDR3L

DDR3L is a higher performance DDR3 SDRAM interface providing less voltage and higher speed successor. DDR3L SDRAM modules support 1333/1600MHz for DDR modules. DDR3L delivers increased system bandwidth and improved performance to provide its higher bandwidth and its increase in performance at a lower power than DDR3 and DDR2.

Graphics

The integrated Intel® HD graphics engine delivers an excellent blend of graphics performance and features to meet business needs. It provides excellent video and 3D graphics with outstanding graphics responsiveness. These enhancements deliver the performance and compatibility needed for today's and tomorrow's business applications. Supports VGA and LVDS interfaces for 2 display outputs.

Serial ATA

Serial ATA is a storage interface that is compliant with SATA 1.0a specification. With speed of up to 3Gb/s (SATA 2.0) and 6Gb/s (SATA 3.0), it improves hard drive performance faster than the standard parallel ATA whose data transfer rate is 100MB/s. The bandwidth of the SATA 3.0 will be limited by carrier board design.

Gigabit LAN

Chapter 1 Introduction

The Intel® I217LM Gigabit LAN controller supports up to 1Gbps data transmission.

• USB

The system board supports USB 2.0 ports. USB 2.0 supports 480Mb/second bandwidth providing a marked improvement in device transfer speeds between your computer and a wide range of simultaneously accessible external Plug and Play peripherals.

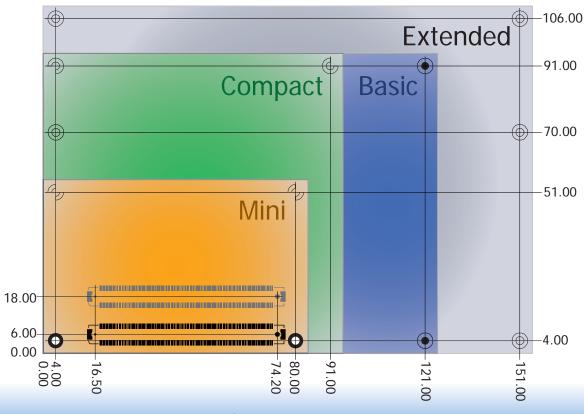
Chapter 2 - Concept

COM Express Module Standards

The figure below shows the dimensions of the different types of COM Express modules.

HM920-QM87/HM86 is a COM Express Basic module. The dimension is 95mm x 125mm.

- O Common for all Form Factors
- Extended only
- Basic only
- **©** Compact only
- [♠] Compact and Basic only
- ^Q
 _O Mini only



Chapter 2 Concept www.dfi.com

Specification Comparison Table

The table below shows the COM Express standard specifications and the corresponding specifications supported on the HM920-QM87/HM86 module.

Connector	Feature	COM Express Module Base Specification Type 2 (IDE + PCI) Min / Max	DFI HM920-QM87/HM86 Type 2
A-B		System I/O	
A-B	PCI Express Lanes 0 - 5	1/6	6
A-B	LVDS Channel A	0 / 1	1
A-B	LVDS Channel B	0 / 1	1
A-B	eDP on LVDS CH A pins	NA	NA
A-B	VGA Port	0 / 1	1
A-B	TV-Out	NA	NA
A-B	DDI 0	NA	NA
A-B ⁵	Serial Ports 1 - 2	NA	NA
A-B	CAN interface on SER1	NA	NA
A-B	SATA / SAS Ports	1 / 4	4
A-B	AC'97 / HDA Digital Interface	0 / 1	1
A-B	USB 2.0 Ports	4 / 8	8
A-B	USB Client	0 / 1	0
A-B	USB 3.0 Ports	NA	NA
A-B	LAN Port 0	1 / 1	1
A-B	Express Card Support	1 / 2	2
A-B	LPC Bus	1 / 1	1
A-B	SPI	1 / 2	1
A-B		System Management	
A-B ⁶	SDIO (muxed on GPIO)	NA	NA
A-D	General Purpose I/O	8 / 8	8
A-B	SMBus	1 / 1	1
A-B	12C	1 / 1	1
A-B	Watchdog Timer	0 / 1	1
A-B	Speaker Out	1 / 1	1
A-B	External BIOS ROM Support	0 / 2	2
A-B	Reset Functions	1 / 1	1

- 5 Indicates 12V-tolerant features on former VCC_12V signals.
- 6 Cells in the connected columns spanning rows provide a rough approximation of features sharing connector pins.

Connector	Feature	Type 2 (IDE + PCI) Min / Max	DFI HM920-QM87/HM86 Type 2
A-B		Power Management	
A-B	Thermal Protection	0 / 1	1
A-B	Battery Low Alarm	0 / 1	1
A-B	Suspend/Wake Signals	0 / 3	2
A-B	Power Button Support	1 / 1	1
A-B	Power Good	1 / 1	1
A-B	VCC_5V_SBY Contacts	4 / 4	4
A-B ⁵	Sleep Input	NA	NA
A-B ⁵	Lid Input	NA	NA
A-B ⁵	Fan Control Signals	NA	NA
A-B	Trusted Platform Modules	NA	NA
A-B		Power	
A-B	VCC_12V Contacts	12 / 12	12

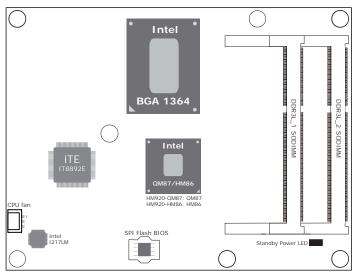
Module Pin-out - Required and Optional Features C-D Connector. PICMG® COM.0Revision 2.1

Connector	Feature	Type 2 (IDE + PCI) Min / Max	DFI HM920-QM87/HM86 Type 2
C-D		System I/O	
	PCI Express Lanes 16 - 31	0 / 16	16
	PCI Express Graphics (PEG)	0 / 1	1
C-D ⁶	Muxed SDVO Channels 1 - 2	0 / 2	NA
	PCI Express Lanes 6 - 15	NA	NA
	PCI Bus - 32 Bit	1 / 1	1
	PATA Port	1/1	1
	LAN Ports 1 - 2	NA	NA
	DDIs 1 - 3	NA	NA
C-D ⁶	USB 3.0 Ports	NA	NA
C-D		Power	
C-D	VCC_12V Contacts	12 / 12	12

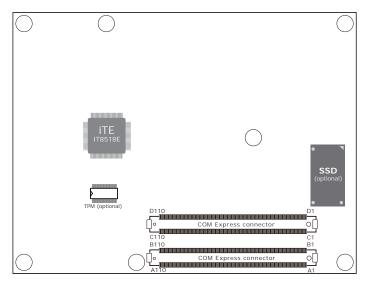
Chapter 2 Concept www.dfi.com

Chapter 3 - Hardware Installation

Board Layout

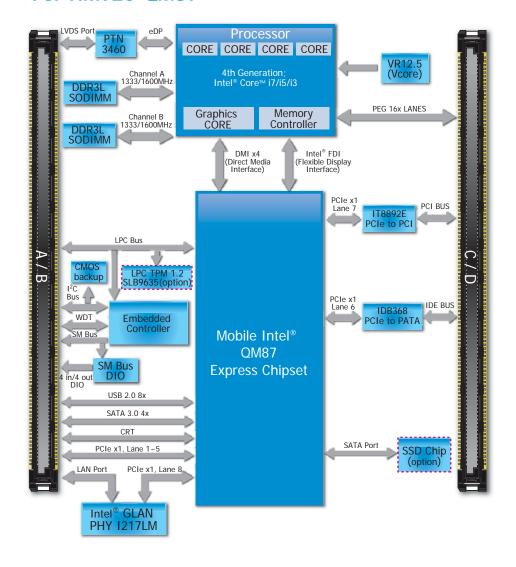


Top View

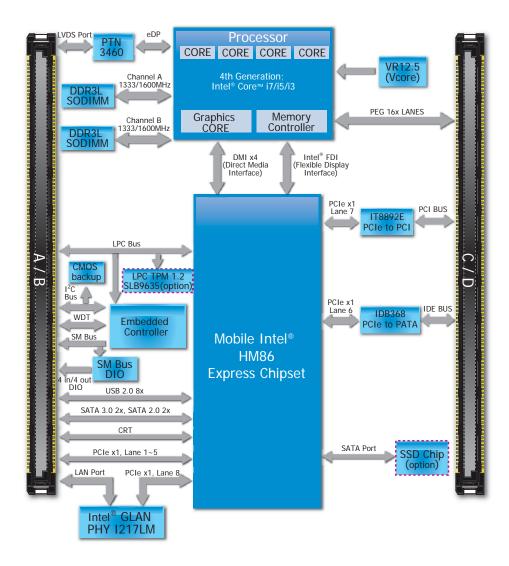


Bottom View

Block Diagram For HM920-QM87

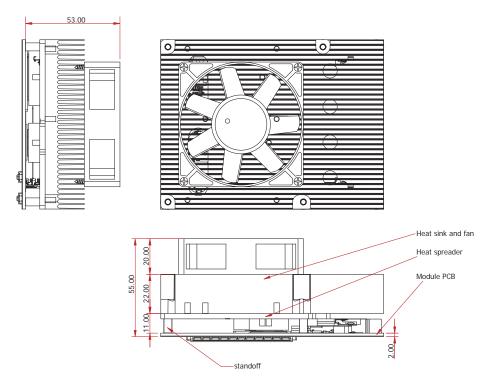


For HM920-HM86



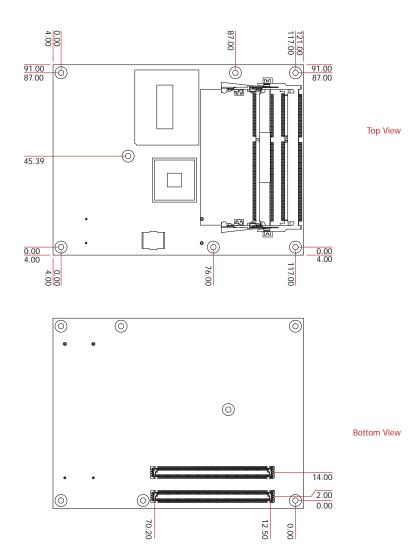
Mechanical Diagram

HM920-QM87/HM86 Module with Heat Sink



Side View of the Module with Heat Sink and Carrier Board

HM920-QM87/HM86 Module



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Important:

Electrostatic discharge (ESD) can damage your board, processor, disk drives, add-in boards, and other components. Perform installation procedures at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

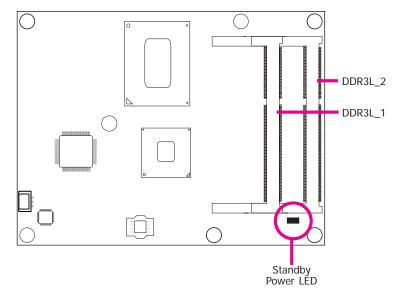
System Memory

The system board is equipped with two 204-pin DDR3L SODIMM sockets that supports up to 16GB system memory.



Important:

When the Standby Power LED lights red, it indicates that there is power on the board. Power-off the PC then unplug the power cord prior to installing any devices. Failure to do so will cause severe damage to the board and components.



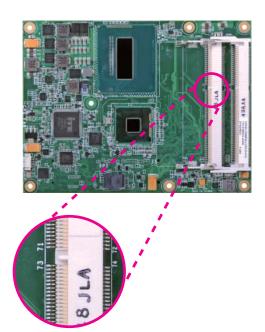
Installing the DIMM Module



Note:

The system board used in the following illustrations may not resemble the actual one. These illustrations are for reference only.

- 1. Make sure the PC and all other peripheral devices connected to it has been powered down.
- 2. Disconnect all power cords and cables.
- 3. Locate the SODIMM socket on the system board.
- 4. Note the key on the socket. The key ensures the module can be plugged into the socket in only one direction.



Grasping the module by its edges, align the module into the socket at an approximately 30 degrees angle. Apply firm even pressure to each end of the module until it slips down into the socket. The contact fingers on the edge of the module will almost completely disappear inside the socket.

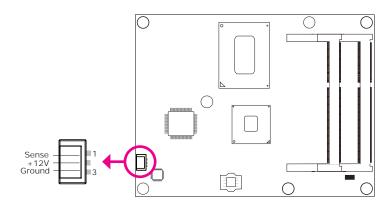


6. Push down the module until the clips at each end of the socket lock into position. You will hear a distinctive "click", indicating the module is correctly locked into position.



Connectors

CPU Fan Connector



Connect the CPU fan's cable connector to the CPU fan connector on the board. The cooling fan will provide adequate airflow throughout the chassis to prevent overheating the CPU and board components.

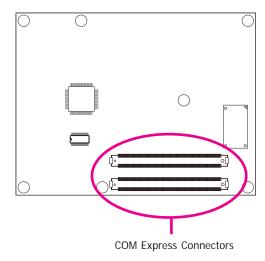
BIOS Setting

"PC Health Status" submenu in the Advanced menu of the BIOS will display the current speed of the cooling fan. Refer to chapter 4 of the manual for more information.

COM Express Connectors

The COM Express connectors are used to interface the HM920-QM87/HM86 COM Express board to a carrier board. Connect the COM Express connectors (located on the solder side of the board) to the COM Express connectors on the carrier board.

Refer to the "Installing HM920-QM87/HM86 onto a Carrier Board" section for more information.



Refer to the following pages for the pin functions of these connectors.

COM Express Connectors

Pin	Row A	Row B
1	GND(FIXED)	GND(FIXED)
2	GBE0_MDI3-	GBE0_ACT#
3	GBE0_MDI3+	LPC_FRAME#
4	GBE0_LINK100#	LPC_AD0
5	GBE0_LINK1000#	LPC_AD1
6	GBE0_MDI2-	LPC_AD2
7	GBE0_MDI2+	LPC_AD3
8	GBE0_LINK#	LPC_DRQ0#
9	GBE0_MDI1-	LPC_DRQ1#
10	GBE0_MDI1+	LPC_CLK
11	GND(FIXED)	GND(FIXED)
12	GBE0_MDI0-	PWRBTN#
13	GBE0_MDI0+	SMB_CK
14	GBE0_CTREF	SMB_DAT
15	SUS_S3#	SMB_ALERT#
16	SATA0_TX+	SATA1_TX+
17	SATA0_TX-	SATA1_TX-
18	SUS_S4#	SUS_STAT#
19	SATA0_RX+	SATA1_RX+
20	SATA0_RX-	SATA1_RX-
21	GND(FIXED)	GND(FIXED)
22	SATA2_TX+	SATA3_TX+
23	SATA2_TX-	SATA3_TX-
24	SUS_S5#	PWR_OK
25	SATA2_RX+	SATA3_RX+
26	SATA2_RX-	SATA3_RX-
27	BATLOW#	WDT
28	(S)ATA_ACT#	AC/HDA_SDIN2
29	AC/HDA_SYNC	AC/HDA_SDIN1
30	AC/HDA_RST#	AC/HDA_SDIN0
31	GND(FIXED)	GND(FIXED)
32	AC/HDA_BITCLK	SPKR
33	AC/HDA_SDOUT	I2C_CK
34	BIOS_DIS0#	I2C_DAT
35	THRMTRIP#	THRM#
36	USB6-	USB7-
37	USB6+	USB7+
38	USB_6_7_OC#	USB_4_5_OC#
39	USB4-	USB5-
40	USB4+	USB5+

Pin	Row A	Row B
41	GND(FIXED)	GND(FIXED)
42	USB2-	USB3-
43	USB2+	USB3+
44	USB_2_3_OC#	USB_0_1_OC#
45	USB0-	USB1-
46	USB0+	USB1+
47	VCC_RTC	EXCD1_PERST#
48	EXCD0_PERST#	EXCD1_CPPE#
49	EXCD0_CPPE#	SYS_RESET#
50	LPC_SERIRQ	CB_RESET#
51	GND(FIXED)	GND(FIXED)
52	PCIE_TX5+	PCIE_RX5+
53	PCIE_TX5-	PCIE_RX5-
54	GPI0	GPO1
55	PCIE_TX4+	PCIE_RX4+
56	PCIE_TX4-	PCIE_RX4-
57	GND	GPO2
58	PCIE_TX3+	PCIE_RX3+
59	PCIE_TX3-	PCIE_RX3-
60	GND(FIXED)	GND(FIXED)
61	PCIE_TX2+	PCIE_RX2+
62	PCIE_TX2-	PCIE_RX2-
63	GPI1	GPO3
64	PCIE_TX1+	PCIE_RX1+
65	PCIE_TX1-	PCIE_RX1-
66	GND	WAKE0#
67	GPI2	WAKE1#
68	PCIE_TX0+	PCIE_RX0+
69	PCIE_TX0-	PCIE_RX0-
70	GND(FIXED)	GND(FIXED)
71	LVDS_A0+	LVDS_B0+
72	LVDS_A0-	LVDS_B0-
73	LVDS_A1+	LVDS_B1+
74	LVDS_A1-	LVDS_B1-
75	LVDS_A2+	LVDS_B2+
76	LVDS_A2-	LVDS_B2-
77	LVDS_VDD_EN	LVDS_B3+
78	LVDS_A3+	LVDS_B3-
79	LVDS_A3-	LVDS_BKLT_EN
80	GND(FIXED)	GND(FIXED)

Pin	Row A	Row B
81	LVDS A CK+	LVDS B CK+
82	LVDS A CK-	LVDS B CK-
83	LVDS_I2C_CK	LVDS_BKLT_CTRL
84	LVDS_I2C_DAT	VCC_5V_SBY
85	GPI3	VCC_5V_SBY
86	KBD_RST#	VCC_5V_SBY
87	KBD_A20GATE	VCC_5V_SBY
88	PCIE_CLK_REF+	BIOS_DIS1#
89	PCIE_CLK_REF-	VGA_RED
90	GND(FIXED)	GND(FIXED)
91	SPI_POWER	VGA_GRN
92	SPI_MISO	VGA_BLU
93	GPO0	VGA_HSYNC
94	SPI_CLK	VGA_VSYNC
95	SPI_MOSI	VGA_I2C_CK
96	GND	VGA_I2C_DAT
97	TYPE10#	SPI_CS#
98	RSVD ¹⁶	RSVD ¹⁶
99	RSVD ¹⁶	RSVD
100	GND(FIXED)	GND(FIXED)
101	RSVD ¹⁶	RSVD ¹⁶
102	RSVD ¹⁶	RSVD ¹⁶
103	RSVD ¹⁶	RSVD ¹⁶
104	VCC_12V	VCC_12V
105	VCC_12V	VCC_12V
106	VCC_12V	VCC_12V
107	VCC_12V	VCC_12V
108	VCC_12V	VCC_12V
109	VCC_12V	VCC_12V
110	GND(FIXED)	GND(FIXED)

16

Pin	Row C	Row D
1	GND(FIXED)	GND(FIXED)
2	IDE D7	IDE D5
3	IDE_D6	IDE_D10
4	IDE D3	IDE D11
5	IDE_D15	IDE_D12
6	IDE_D8	IDE_D4
7	IDE_D9	IDE_D0
8	IDE_D2	IDE_REQ
9	IDE_D13	IDE_IOW#
10	IDE_D1	IDE_ACK#
11	GND(FIXED)	GND(FIXED)
12	IDE_D14	IDE_IRQ
13	IDE_IORDY	IDE_A0
14	IDE_IOR#	IDE_A1
15	PCI_PME#	IDE_A2
16	PCI_GNT2#	IDE_CS1#
17	PCI_REQ2#	IDE_CS3#
18	PCI_GNT1#	IDE_RESET#
19	PCI_REQ1#	PCI_GNT3#
20	PCI_GNT0#	PCI_REQ3#
21	GND(FIXED)	GND(FIXED)
22	PCI_REQ0#	PCI_AD1
23	PCI_RESET#	PCI_AD3
24	PCI_AD0	PCI_AD5
25	PCI_AD2	PCI_AD7
26	PCI_AD4	PCI_C/BE0#
27	PCI_AD6	PCI_AD9
28	PCI_AD8	PCI_AD11
29	PCI_AD10	PCI_AD13
30	PCI_AD12	PCI_AD15
31	GND(FIXED)	GND(FIXED)
32	PCI_AD14	PCI_PAR
33	PCI_C/BE1#	PCI_SERR#
34	PCI_PERR#	PCI_STOP#
35	PCI_LOCK#	PCI_TRDY#
36	PCI_DEVSEL#	PCI_FRAME#
37	PCI_IRDY#	PCI_AD16
38	PCI_C/BE2#	PCI_AD18
39	PCI_AD17	PCI_AD20
40	PCI_AD19	PCI_AD22

Pin	Row C	Row D
41	GND(FIXED)	GND(FIXED)
42	PCI AD21	PCI AD24
43	PCI_AD23	PCI_AD26
44	PCI_C/BE3#	PCI_AD28
45	PCI_AD25	PCI_AD30
46	PCI_AD27	PCI_IRQC#
47	PCI_AD29	PCI_IRQD#
48	PCI_AD31	PCI_CLKRUN#
49	PCI_IRQA#	PCI_M66EN
50	PCI_IRQB#	PCI_CLK
51	GND(FIXED)	GND(FIXED)
52	PEG_RX0+	PEG_TX0+
53	PEG_RX0-	PEG_TX0-
54	TYPE0#	PEG_LANE_RV#
55	PEG_RX1+	PEG_TX1+
56	PEG_RX1-	PEG_TX1-
57	TYPE1#	TYPE2#
58	PEG_RX2+	PEG_TX2+
59	PEG_RX2-	PEG_TX2-
60	GND(FIXED)	GND(FIXED)
61	PEG_RX3+	PEG_TX3+
62	PEG_RX3-	PEG_TX3-
63	RSVD ¹⁶	RSVD ¹⁶
64	RSVD ¹⁶	RSVD ¹⁶
65	PEG_RX4+	PEG_TX4+
66	PEG_RX4-	PEG_TX4-
67	RSVD ¹⁶	GND
68	PEG_RX5+	PEG_TX5+
69	PEG_RX5-	PEG_TX5-
70	GND(FIXED)	GND(FIXED)
71	PEG_RX6+	PEG_TX6+
72	PEG_RX6-	PEG_TX6-
73	SDVO_DATA	SDVO_CLK
74	PEG_RX7+	PEG_TX7+
75	PEG_RX7-	PEG_TX7-
76	GND	GND
77	RSVD ¹⁶	IDE_CBLID#
78	PEG_RX8+	PEG_TX8+
79	PEG_RX8-	PEG_TX8-
80	GND(FIXED)	GND(FIXED)

Pin	Row C	Row D
81	PEG_RX9+	PEG_TX9+
82	PEG_RX9-	PEG_TX9-
83	RSVD ¹⁶	RSVD ¹⁶
84	GND	GND
85	PEG_RX10+	PEG_TX10+
86	PEG_RX10-	PEG_TX10-
87	GND	GND
88	PEG_RX11+	PEG_TX11+
89	PEG_RX11-	PEG_TX11-
90	GND(FIXED)	GND(FIXED)
91	PEG_RX12+	PEG_TX12+
92	PEG_RX12-	PEG_TX12-
93	GND	GND
94	PEG_RX13+	PEG_TX13+
95	PEG_RX13-	PEG_TX13-
96	GND	GND
97	RSVD ¹⁶	PEG_ENABLE#
98	PEG_RX14+	PEG_TX14+
99	PEG_RX14-	PEG_TX14-
100	GND(FIXED)	GND(FIXED)
101	PEG_RX15+	PEG_TX15+
102	PEG_RX15-	PEG_TX15-
103	GND	GND
104	VCC_12V	VCC_12V
105	VCC_12V	VCC_12V
106	VCC_12V	VCC_12V
107	VCC_12V	VCC_12V
108	VCC_12V	VCC_12V
109	VCC_12V	VCC_12V
110	GND(FIXED)	GND(FIXED)

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COM Express Connectors Signal Description

PCIE

O PCIE

PCIE

A59

A56

B55 B56

AC coupled off Module

AC coupled on Module

AC coupled off Module

AC Coupling capacitor

AC Coupling capacitor

AC Coupling capacitor

PCIE_TX3-

PCIE_RX3+

PCIE_TX4+

PCIE_TX4-

PCIE_RX4+ PCIE_RX4-

Pin Types
I Input to the Module

O Output from the Module
I/O Bi-directional input / output signal
OD Open drain output

OD Open drain output						
AC97/HDA Signals Des	criptions					
Signal	Pin#	Module Pin Ty	pe Pwr Rail /Tolerance	HM920	Carrier Board	Description
AC/HAD_RST#	A30	O CMOS	3.3V Suspend/3.3V		Connect to CODEC pin 11 RESET#	Reset output to CODEC, active low.
C/HDA_SYNC	A29	O CMOS	3.3V/3.3V	PU 1K to 3.3VSB	Connect to CODEC pin 10 SYNC	Sample-synchronization signal to the CODEC(s).
C/HDA_BITCLK	A32	I/O CMOS	3.3V/3.3V		Connect to CODEC pin 6 BIT_CLK	Serial data clock generated by the external CODEC(s).
C/HDA_SDOUT	A33	O CMOS	3.3V/3.3V		Connect to CODEC pin 5 SDATA_OUT	Serial TDM data output to the CODEC.
C/HDA_SDIN2	B28	I/O CMOS	3.3V Suspend/3.3V		Connect 33 Ω in series to CODEC2 pin 8 SDATA_IN	
C/HDA_SDIN1	B29	I/O CMOS	3.3V Suspend/3.3V		Connect 33 Ω in series to CODEC1 pin 8 SDATA_IN	Serial TDM data inputs from up to 3 CODECs.
C/HDA_SDIN0	B30	I/O CMOS	3.3V Suspend/3.3V		Connect 33 Ω in series to CODECO pin 8 SDATA_IN	
		•			· <u>-</u>	
Gigabit Ethernet Signal gnal	IS Descriptio		pe Pwr Rail /Tolerance	HM920	Carrier Board	Description
EO_MDIO+	A13	I/O Analog	3.3V max Suspend			Gigabit Ethernet Controller 0: Media Dependent Interface Differential
BEO_MDIO-	A12	I/O Analog	3.3V max Suspend		Connect to Magnetics Module MDI0+/-	Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec
BEO_MDI1+	A10	I/O Analog	3.3V max Suspend			modes. Some pairs are unused in some modes, per the following:
E0_MDI1-	A9	I/O Analog	3.3V max Suspend		Connect to Magnetics Module MDI1+/-	1000BASE-T 100BASE-TX 10BASE-T
EO_MDI1+	A7	I/O Analog	3.3V max Suspend			MDI[0]+/- B1_DA+/- TX+/- TX+/-
	A7 A6				Connect to Magnetics Module MDI2+/-	MDI[0]+/- B1_DB+/- RX+/- RX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/-
E0_MD12-		I/O Analog	3.3V max Suspend			
E0_MDI3+	A3	I/O Analog	3.3V max Suspend		Connect to Magnetics Module MDI3+/-	MDI[2]+/- B1_DC+/-
E0_MDI3-	A2	I/O Analog	3.3V max Suspend		9	MDI[3]+/- B1_DD+/-
EO_ACT#	B2	OD CMOS	3.3V Suspend/3.3V		Connect to LED and recommend current limit resistor NC 150 Ω to 3.3VSB	Gigabit Ethernet Controller 0 activity indicator, active low.
E0_LINK#	A8	OD CMOS	3.3V Suspend/3.3V		NC	Gigabit Ethernet Controller 0 link indicator, active low.
E0_LINK100#	A4	OD CMOS	3.3V Suspend/3.3V		Connect to LED and recommend current limit resistor 150 \(\Omega\$ to 3.3VSB	Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.
EO_LINK1000#	A5	OD CMOS	3.3V Suspend/3.3V		Connect to LED and $$ recommend current limit resistor 150 $$ Ω to 3.3VSB	Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.
ATA Signals Description	ons					
nal	Pin#	Module Pin Tv	pe Pwr Rail /Tolerance	HM920	Carrier Board	Description
TAO_TX+	A16	O SATA	AC coupled on Module	AC Coupling capacitor		
TAO_TX-	A17	O SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATAO Conn TX pin	Serial ATA or SAS Channel 0 transmit differential pair.
TAO_RX+	A19	I SATA	AC coupled on Module	AC Coupling capacitor		
TAO_RX-	A20	I SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATAO Conn RX pin	Serial ATA or SAS Channel 0 receive differential pair.
TA1_TX+	B16	O SATA	AC coupled on Module	AC Coupling capacitor		
TA1_TX-	B17	O SATA			Connect to SATA1 Conn TX pin	Serial ATA or SAS Channel 1 transmit differential pair.
TA1_RX+	B17	I SATA	AC coupled on Module AC coupled on Module	AC Coupling capacitor		
				AC Coupling capacitor	Connect to SATA1 Conn RX pin	Serial ATA or SAS Channel 1 receive differential pair.
TA1_RX-	B20	I SATA	AC coupled on Module	AC Coupling capacitor		
TA2_TX+	A22	O SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATA2 Conn TX pin	Serial ATA or SAS Channel 2 transmit differential pair.
TA2_TX-	A23	O SATA	AC coupled on Module	AC Coupling capacitor		
TA2_RX+	A25	I SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATA2 Conn RX pin	Serial ATA or SAS Channel 2 receive differential pair.
ΓA2_RX-	A26	I SATA	AC coupled on Module	AC Coupling capacitor	CONTROL TO GATAL CONTINA PIN	Social Title St. St. S. Statistica 2 receive differential pair.
TA3_TX+	B22	O SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATA3 Conn TX pin	Serial ATA or SAS Channel 3 transmit differential pair.
TA3_TX-	B23	O SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATAS COURT IX PILL	Serial KTK of SKS Chairlier'S transmit unreferitial pail.
TA3_RX+	B25	I SATA	AC coupled on Module	AC Coupling capacitor	Ct t- CATA2 C BV -i-	Control ATA on CAS Channel 2 annoting differential and
TA3_RX-	B26	I SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATA2 Conn RX pin	Serial ATA or SAS Channel 3 receive differential pair.
A_ACT#	A28	I/O CMOS	3.3V / 3.3V	PU 10K to 3.3V	Connect to LED and recommend current limit resistor 220Ω to 3.3V	ATA (parallel and serial) or SAS activity indicator, active low.
CI Express Lanes Sign	nale Descript	ions				
inal	Pin#	Module Pin Tu	pe Pwr Rail /Tolerance	HM920	Carrier Board	Description
IE_TX0+	A68			AC Coupling capacitor		
E_TX0-	A69	O PCIE	AC coupled on Module	AC Coupling capacitor AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 0
			1	Ac Coupling capacitor	Devides Comment AC Complian and O days	
E_RX0+	B68	I PCIE	AC coupled off Module		Device - Connect AC Coupling cap 0.1uF	PCI Express Differential Receive Pairs 0
E_RX0-	B69				Slot - Connect to PCIE Conn pin	
E_TX1+	A64	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 1
E_TX1-	A65	0.012	coapica on module	AC Coupling capacitor		
E_RX1+	B64	I PCIE	AC coupled off Module		Device - Connect AC Coupling cap 0.1uF	PCI Express Differential Receive Pairs 1
E_RX1-	B65	I PUIE	Ac coupled on Module		Slot - Connect to PCIE Conn pin	roi express dinerential Receive Pairs 1
IE_TX2+	A61			AC Coupling capacitor	•	
E_TX2-	A62	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 2
IE_RX2+	B61			oodpinig odpasitoi	Device - Connect AC Coupling cap 0.1uF	
E_RX2-	B62	I PCIE	AC coupled off Module		Slot - Connect to PCIE Conn pin	PCI Express Differential Receive Pairs 2
				AC Coupling conscit	•	
IE_TX3+	A58	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 3

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PCI Express Differential Receive Pairs 3

PCI Express Differential Transmit Pairs 4

PCI Express Differential Receive Pairs 4

Device - Connect AC Coupling cap 0.1uF

Device - Connect AC Coupling cap 0.1uF

Slot - Connect to PCIE Conn pin

Connect to PCIE device or slot

Slot - Connect to PCIE Conn pin

Chapter 3

PCI Express Lanes Signa	Is Description	ns			
Signal	Pin#	Module Pin Typ	pe Pwr Rail /Tolerance HM920	Carrier Board	Description
PCIE_TX5+ PCIE_TX5-	A52 A53	O PCIE	AC coupled on Module AC Coupling capacitor AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 5
PCIE_RX5+	B52	I PCIE	AC coupled off Module	Device - Connect AC Coupling cap 0.1uF	PCI Express Differential Receive Pairs 5
PCIE_RX5- PCIEO_CK_REF+	B53		· ·	Slot - Connect to PCIE Conn pin	Pol Express differential Receive Pails 5
PCIEO_CK_REF+	A88 A89	O PCIE	PCIE	Connect to PCIE device, PCIe CLK Buffer or slot	Reference clock output for all PCI Express and PCI Express Graphics lanes.
DEC Ciamala Danamintian		•	•	•	·
PEG Signals Description Signal	Pin#	Module Pin Typ	pe Pwr Rail /Tolerance HM920	Carrier Board	Description
PEG_TX0+	D52	O PCIE	AC coupled on Module AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Graphics transmit differential pairs 0
PEG_TX0- PEG_RX0+	D53 C52	I DOLE	AC Coupling capacitor	0 1400 1 000 5	2015
PEG_RX0-	C53	I PCIE	AC coupled off Module	Connect AC Coupling cap 0.22uF	PCI Express Graphics receive differential pairs 0
PEG_TX1+ PEG_TX1-	D55 D56	O PCIE	AC coupled on Module AC Coupling capacitor AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Graphics transmit differential pairs 1
PEG_RX1+	C55	I PCIE	AC coupled off Module	Connect AC Coupling cap 0.22uF	PCI Express Graphics receive differential pairs 1
PEG_RX1- PEG_TX2+	C56 D58		AC Coupling capacitor		
PEG_TX2-	D59	O PCIE	AC coupled on Module AC Coupling capacitor AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Graphics transmit differential pairs 2
PEG_RX2+ PEG_RX2-	C58 C59	I PCIE	AC coupled off Module	Connect AC Coupling cap 0.22uF	PCI Express Graphics receive differential pairs 2
PEG_TX3+	D61	O PCIE	AC coupled on Module AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Graphics transmit differential pairs 3
PEG_TX3- PEG_RX3+	D62 C61		AC Coupling capacitor		
PEG_RX3-	C62	I PCIE	AC coupled off Module	Connect AC Coupling cap 0.22uF	PCI Express Graphics receive differential pairs 3
PEG_TX4+ PEG_TX4-	D65 D66	O PCIE	AC coupled on Module AC Coupling capacitor AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Graphics transmit differential pairs 4
PEG_RX4+	C65	I PCIE	AC coupled off Module	Connect AC Coupling cap 0.22uF	PCI Express Graphics receive differential pairs 4
PEG_RX4- PEG_TX5+	C66 D68	O PCIE	AC coupled on Module AC Coupling capacitor	Company to DOIS device and the	DOL Furnass Complies to a south differential point F
PEG_TX5- PEG_RX5+	D69 C68	O PCIE	AC coupled on Module AC Coupling capacitor AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Graphics transmit differential pairs 5
PEG_RX5+	C69	I PCIE	AC coupled off Module	Connect AC Coupling cap 0.22uF	PCI Express Graphics receive differential pairs 5
PEG_TX6+ PEG_TX6-	D71 D72	O PCIE	AC coupled on Module AC Coupling capacitor AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Graphics transmit differential pairs 6
PEG_RX6+	C71	I PCIE	AC coupled off Module	Connect AC Coupling cap 0.22uF	PCI Express Graphics receive differential pairs 6
PEG_RX6- PEG_TX7+	C72		AC Counting connector		
PEG_TX7-	D75	O PCIE	AC coupled on Module AC Coupling capacitor AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Graphics transmit differential pairs 7
PEG_RX7+ PEG_RX7-	C74 C75	I PCIE	AC coupled off Module	Connect AC Coupling cap 0.22uF	PCI Express Graphics receive differential pairs 7
PEG_TX8+	D78	O PCIE	AC coupled on Module AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Graphics transmit differential pairs 8
PEG_TX8- PEG_RX8+	D79 C78		AC Coupling capacitor		
PEG_RX8-	C79	I PCIE	AC coupled off Module	Connect AC Coupling cap 0.22uF	PCI Express Graphics receive differential pairs 8
PEG_TX9+ PEG_TX9-	D81 D82	O PCIE	AC coupled on Module AC Coupling capacitor AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Graphics transmit differential pairs 9
PEG_RX9+ PEG_RX9-	C81 C82	I PCIE	AC coupled off Module	Connect AC Coupling cap 0.22uF	PCI Express Graphics receive differential pairs 9
PEG_TX10+	D85	O PCIE	AC coupled on Module AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Graphics transmit differential pairs 10
PEG_TX10- PEG_RX10+	D86 C85		AC Coupling capacitor		
PEG_RX10-	C86	I PCIE	AC coupled off Module	Connect AC Coupling cap 0.22uF	PCI Express Graphics receive differential pairs 10
PEG_TX11+ PEG_TX11-	D88 D89	O PCIE	AC coupled on Module AC Coupling capacitor AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Graphics transmit differential pairs 11
PEG_RX11+	C88	I PCIE	AC coupled off Module	Connect AC Coupling cap 0.22uF	PCI Express Graphics receive differential pairs 11
PEG_RX11- PEG_TX12+	C89 D91		AC Counling capacitor		<u>'</u>
PEG_TX12-	D92	O PCIE	AC coupled on Module AC Coupling capacitor AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Graphics transmit differential pairs 12
PEG_RX12+ PEG_RX12-	C91 C92	I PCIE	AC coupled off Module	Connect AC Coupling cap 0.22uF	PCI Express Graphics receive differential pairs 12
PEG_TX13+	D94	O PCIE	AC coupled on Module AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Graphics transmit differential pairs 13
PEG_TX13- PEG_RX13+	D95 C94		AC Coupling capacitor		
PEG_RX13-	C95	I PCIE	AC coupled off Module	Connect AC Coupling cap 0.22uF	PCI Express Graphics receive differential pairs 13
PEG_TX14+ PEG_TX14-	D98 D99	O PCIE	AC coupled on Module AC Coupling capacitor AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Graphics transmit differential pairs 14
PEG_RX14+	C98	I PCIE	AC coupled off Module	Connect AC Coupling cap 0.22uF	PCI Express Graphics receive differential pairs 14
PEG_RX14- PEG_TX15+	C99 D101	O PCIE	AC coupled on Module AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Graphics transmit differential pairs 15
PEG_TX15-	D102		AC Coupling capacitor	CONTROL TO FOIE DEVICE OF SIDE	
PEG_RX15+ PEG_RX15-	C101 C102	I PCIE	AC coupled off Module	Connect AC Coupling cap 0.22uF	PCI Express Graphics receive differential pairs 15
PEG_ENABLE#	D97	I CMOS	3.3V / 3.3V PU 10k to 3.3V		Strap to enable PCI Express x16 external graphics interface. Pull low to enable the x16 PEG interface.
PEG_LANE_RV#	D54	I CMOS	3.3V / 3.3V	PU 4.7k to 3.3V	PCI Express Graphics lane reversal input strap. Pull low on the Carrier
LO_DANC_RV#	D34	1 CIVIOS	J.57 / J.57	FO 4.7K to 5.5V	board to reverse lane order.

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ExpressCard Signals Descriptions								
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	HM920	Carrier Board	Description		
EXCD0_CPPE#	A49	I CMOS	3.3V /3.3V	PU 10k to 3.3V		PCI ExpressCard: PCI Express capable card request, active low, one per		
EXCD1_CPPE#	B48	I CIVIOS	3.37 /3.37	PU 10k to 3.3V		card		
EXCD0_PERST#	A48	o cmos	3.3V /3.3V			PCI ExpressCard: reset, active low, one per card		
EXCD1_PERST#	B47	U CIVIUS	3.3V /3.3V			PCT Expressional Teset, active low, one per card		
	•				•	•		

EXCD1_PERST#	B47	0 011105	3.34 73.34			Tot Expressed d. Teset, active low, one per card						
DOL Cinnala Description	_											
PCI Signals Descriptions	Pin#	Modulo Din Tuno	Dur Doil /Toloropeo	HM920	Carrier Board	Description						
Signal PCI_AD0	C24	wodule Pin Type	Pwr Rail /Tolerance	HIVI920	Carrier Board	Description						
PCI_AD0	D22											
PCI_AD1	C25											
PCI_AD3	D23											
PCI_AD4	C26											
PCI_AD5	D24											
PCI_AD6	C27	1										
PCI_AD7	D25											
PCI_AD8	C28											
PCI_AD9	D27											
PCI_AD9 PCI_AD10	C29											
PCI_AD10 PCI_AD11												
PCI_AD11	D28 C30											
PCI_AD12	D29											
PCI_AD13	C32											
PCI_AD14		1/0 01400	0.01/ /51/									
PCI_AD16	D37	I/O CMOS	3.3V /5V			PCI bus multiplexed address and data lines						
PCI_AD16 PCI_AD17	C39											
PCI_AD17	D38											
PCI_AD19	C40											
PCI_AD20	D39											
PCI_AD20 PCI_AD21	C42											
PCI_AD21	D40											
PCI_AD22 PCI_AD23	C43			l .								
PCI_AD24	D42											
PCI_AD24 PCI_AD25	C45			-	-							
PCI_AD26	D43											
PCI_AD20	C46											
PCI_AD28	D44											
PCI_AD29	C47											
PCI_AD30	D45											
PCI_AD31	C48											
PCI_CBEO-	D26											
PCI_CBE1-	C33	I/O CMOS	3.3V /5V			PCI bus byte enable lines, active low						
PCI_CBE2-	C38											
PCI_DEVSEL#	C36	I/O CMOS	3.3V / 5V	PU 8.2K TO 3.3V		PCI bus Device Select, active low.						
PCI_FRAME#		I/O CMOS	3.3V / 5V	PU 8.2K TO 3.3V		PCI bus Frame control line, active low.						
PCI_IRDY#		I/O CMOS	3.3V / 5V	PU 8.2K TO 3.3V		PCI bus Initiator Ready control line, active low.						
PCI_TRDY#		I/O CMOS	3.3V / 5V	PU 8.2K TO 3.3V		PCI bus Target Ready control line, active low.						
PCI_STOP#		I/O CMOS	3.3V / 5V	PU 8.2K TO 3.3V		PCI bus STOP control line, active low, driven by cycle initiator.						
PCI_PAR		I/O CMOS	3.3V / 5V			PCI bus parity						
PCI_PERR#		I/O CMOS	3.3V / 5V	PU 8.2K TO 3.3V		Parity Error: An external PCI device drives PERR# when it receives data that has a parity error.						
PCI_REQ0-	C22											
PCI_REQ1-	C19	I CMOS	3.3V / 5V	PU 8.2K TO 3.3V		PCI bus master request input lines, active low.						
PCI_REQ2-	CT/		1			The second secon						
PCI_REQ3-	D20											
P_GNT_0-	C20											
P_GNT_1-	C18	O CMOS	3.3V / 5V			PCI bus master grant output lines, active low.						
P_GNT_2-	C16											
P_GNT_3-	D19	0.01400	2.21/ 0			DCI Deset extent active law						
PCI_RESET#		O CMOS I/O CMOS	3.3V Suspend/ 5V	DILO 2K TO 2 2W		PCI Reset output, active low.						
PCI_LOCK#			3.3V / 5V	PU 8.2K TO 3.3V		PCI Lock control line, active low.						
PCI_SERR#	D33	I/O OD CMOS	3.3V / 5V	PU 8.2K TO 3.3V		System Error: SERR# may be pulsed active by any PCI device that detects a system error condition.						
PCI_PME#	C15	I CMOS	3.3V Suspend/ 5V	PU 10K TO 3.3VSB		PCI Power Management Event: PCI peripherals drive PME# to wake system from low-power states S1–S5.						
PCI_CLKRUN#		I/O CMOS	3.3V / 5V	PU 8.2K TO 3.3V		Bidirectional pin used to support PCI clock run protocol for mobile systems.						
PCI_IRQA#	C49	5 555		10 0.21 10 0.04								
PCI_IRQB#	CEO											
PCI_IRQC#	D46	I CMOS	3.3V / 5V	PU 8.2K TO 3.3V		PCI interrupt request lines.						
PCI_IRQD#	D47											
		O CMOS	3.3V / 3.3V			PCI 33MHz clock output.						
		O CIVIOS	J.JV / J.JV			Module input signal indicates whether an off-Module PCI device is capable of 66MHz operation. Pulled to						
PCI_CLK	וסט											
	DSU											
PCI_CLK		I CMOS	3.3V / 5V			GND by Carrier Board device or by Slot Card if the devices are NOT capable of 66 MHz operation.						
		I CMOS	3.3V / 5V									

USB Signals Description	ions					
Signal	Pin#	Module Pin Typ	e Pwr Rail /Tolerance	HM920	Carrier Board	Description
USB0+ USB0-	A46 A45	I/O USB	3.3V Suspend/3.3V		Connect 90 \textit{\Omega} @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 0
USB1+	B46	_			Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB	
USB1-	B45	I/O USB	3.3V Suspend/3.3V		connector	USB differential pairs 1
USB2+	A43				Connect 90 \(\Omega \) @100MHz Common Choke in series and ESD suppressors to GND to USB	
USB2-	A42	I/O USB	3.3V Suspend/3.3V		connector	USB differential pairs 2
USB3+	B43	I/O USB	3.3V Suspend/3.3V		Connect 90 @100MHz Common Choke in series and ESD suppressors to GND to USB	USB differential pairs 3
USB3-	B42	1/O USB	3.3V Suspend/3.3V		connector	USB differential pairs 3
USB4+	A40	I/O USB	3.3V Suspend/3.3V		Connect 90 @ 100MHz Common Choke in series and ESD suppressors to GND to USB	USB differential pairs 4
USB4-	A39	170 035	3.34 Suspend/3.34		connector	OSB unit citital pairs 4
USB5+	B40	I/O USB	3.3V Suspend/3.3V		Connect 90 @100MHz Common Choke in series and ESD suppressors to GND to USB	USB differential pairs 5
USB5-	B39				connector	
USB6+ USB6-	A37 A36	I/O USB	3.3V Suspend/3.3V		Connect 90 \textit{Q} @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 6
USB7+	B37				connector	
		I/O USB	3.3V Suspend/3.3V		Connect 90 \(\Omega \) @100MHz Common Choke in series and ESD suppressors to GND to USB	USB differential pairs 7, USB7 may be configured as a USB client or as a host, or both, at the
USB7-	B36	170 035	3.34 Suspend/3.34		connector	Module designer's discretion.(CR901-B default set as a host)
						USB over-current sense, USB channels 0 and 1. A pull-up for this line
						shall be present on the Module. An open drain driver from a USB
USB_0_1_OC#	B44	I CMOS	3.3V Suspend/3.3V	PU 10k to 3.3VSB	Connect to Overcurrent of USB Power Switch	current monitor on the Carrier Board may drive this line low. Do not
						pull this line high on the Carrier Board.
						USB over-current sense, USB channels 2 and 3. A pull-up for this line
USB_2_3_OC#	A44	I CMOS	3.3V Suspend/3.3V	PU 10k to 3.3VSB	Connect to Overcurrent of USB Power Switch	shall be present on the Module. An open drain driver from a USB
						current monitor on the Carrier Board may drive this line low. Do not
						pull this line high on the Carrier Board. USB over-current sense, USB channels 4 and 5. A pull-up for this line
						shall be present on the Module. An open drain driver from a USB
USB_4_5_OC#	B38	I CMOS	3.3V Suspend/3.3V	PU 10k to 3.3VSB	Connect to Overcurrent of USB Power Switch	current monitor on the Carrier Board may drive this line low. Do not
						pull this line high on the Carrier Board.
						USB over-current sense, USB channels 6 and 7. A pull-up for this line
USB_6_7_OC#	A38	I CMOS	3.3V Suspend/3.3V	PU 10k to 3.3VSB	Connect to Overcurrent of USB Power Switch	shall be present on the Module. An open drain driver from a USB
U3B_6_7_UC#	MOO	I CIVIOS	3.3V Suspenu/3.3V	PU TUK 10 3.3V3B	Connect to overcurrent of OSB Power Switch	current monitor on the Carrier Board may drive this line low. Do not
						pull this line high on the Carrier Board.
LVDC Ciamala Dassain	41					
LVDS Signals Descript Signal	Pin#	Module Pin Tyn	e Pwr Rail /Tolerance	HM920	Carrier Board	Description
LVDS_A0+	A71			1111720	Connect to LVDS connector	LVDS Channel A differential pairs
LVDS_A0-	A72	O LVDS	LVDS			Ther LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/-, LVDS_A_CK+/-,
LVDS_A1+	A73				Connect to LVDS connector	LVDS_B_CK+/-) shall have 100Ω terminations across the pairs at the destination. These
		O LVDS	LVDS		Connect to EVB3 connector	terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer
LVDS_A1-	A74	_				on-board
LVDS_A2+	A75	O LVDS	LVDS		Connect to LVDS connector	
LVDS_A2-	A76					
LVDS_A3+	A78	O LVDS	LVDS		Connect to LVDS connector	
LVDS_A3-	A79	O LVD3	LVD3			
LVDS_A_CK+	A81	O LVDS	LVDS		Connect to LVDS connector	LVDS Channel A differential clock
LVDS_A_CK-	A82	O LVDS	LVDS			LVDS Channel A differential clock
LVDS_B0+	B71	O LVDS	LVDS		Connect to LVDS connector	
LVDS_B0-	B72	0 2003	2100			LVDS Channel B differential pairs
LVDS_B1+	B73	O LVDS	LVDS		Connect to LVDS connector	Ther LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/ LVDS_A_CK+/-,
LVDS_B1-	B74					
		O EVBS			0 11 11/00	LVDS_B_CK+/-) shall have 100Ω terminations across the pairs at the destination. These
LVDS_B2+	B75	O LVDS	LVDS		Connect to LVDS connector	-LVDS_B_CK+/-) shall have 100Ω terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer
LVDS_B2-	B75 B76	O LVDS				_LVDS_B_CK+/-) shall have 100Ω terminations across the pairs at the destination. These
LVDS_B2- LVDS_B3+	B75 B76 B77		LVDS		Connect to LVDS connector Connect to LVDS connector	–LVDS_B_CK+/-) shall have 100Ω terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer
LVDS_B2- LVDS_B3+ LVDS_B3-	B75 B76 B77 B78	O LVDS	LVDS		Connect to LVDS connector	—LVDS_B_CK+/-) shall have 1000 terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer—on-board ———————————————————————————————————
LVDS_B2- LVDS_B3+ LVDS_B3- LVDS_B_CK+	B75 B76 B77 B78 B81	O LVDS				–LVDS_B_CK+/-) shall have 100Ω terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer
LVDS_B2- LVDS_B3+ LVDS_B3- LVDS_B_CK+ LVDS_B_CK-	B75 B76 B77 B78	O LVDS	LVDS	PU 10K TO 3.3V	Connect to LVDS connector	—LVDS_B_CK+/-) shall have 1000 terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer—on-board ———————————————————————————————————
LVDS_B2- LVDS_B3+ LVDS_B3- LVDS_B_CK+ LVDS_B_CK- LVDS_VDD_EN	B75 B76 B77 B78 B81 B82	O LVDS O LVDS O LVDS	LVDS LVDS	PU 10K TO 3.3V	Connect to LVDS connector Connect to LVDS connector	-LVDS_B_CK-/-) shall have 1002 terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer on-board LVDS Channel B differential clock
LVDS_B2- LVDS_B3+ LVDS_B3- LVDS_B_CK+ LVDS_B_CK- LVDS_VDD_EN LVDS_WBLT_EN	B75 B76 B77 B78 B81 B82 A77	O LVDS O LVDS O LVDS O CMOS	LVDS LVDS 3.3V / 3.3V	PU 10K TO 3.3V	Connect to LVDS connector Connect to LVDS connector Connect to enable control of LVDS panel power circuit	LVDS_B_CK-/-) shall have 1000 terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer on-board LVDS Channel B differential clock LVDS panel power enable
LVDS_B2- LVDS_B3+ LVDS_B3- LVDS_B_CK+ LVDS_B_CK+ LVDS_D_EN LVDS_VS_EKLT_EN LVDS_WSLT_CTRL LVDS_LVDS_EKLT_CTRL LVDS_LVDS_CCK	B75 B76 B77 B78 B81 B82 A77 B79 B83 A83	O LVDS O LVDS O LVDS O CMOS O CMOS O CMOS I/O OD CMOS	LVDS LVDS 3.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V	PU 4.7K TO 3.3V	Connect to LVDS connector Connect to LVDS connector Connect to enable control of LVDS panel power circuit Connect to enable control of LVDS panel backlight power circuit. Connect to brightness control of LVDS panel backlight power circuit. Connect to DDC clock of LVDS panel	-LVDS_B_CK-/-) shall have 1000 terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer on-board LVDS channel B differential clock LVDS panel power enable LVDS panel backlight enable LVDS panel backlight brightness control 12C clock output for LVDS display use
LVDS B2- LVDS_B3+ LVDS_B3- LVDS_B_CK+ LVDS_B_CK+ LVDS_D_EN LVDS_WLT_EN LVDS_BKLT_CTRL LVDS_CK	B75 B76 B77 B78 B81 B82 A77 B79 B83	O LVDS O LVDS O LVDS O CMOS O CMOS O CMOS	LVDS LVDS 3.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V		Connect to LVDS connector Connect to LVDS connector Connect to enable control of LVDS panel power circuit Connect to enable control of LVDS panel backlight power circuit. Connect to brightness control of LVDS panel backlight power circuit.	-LVDS_B_CK-/-) shall have 1002 terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer on-board LVDS Channel B differential clock LVDS panel power enable LVDS panel backlight enable LVDS panel backlight enable
LVDS_B2- LVDS_B3+ LVDS_B3+ LVDS_B3- LVDS_B_CK+ LVDS_B_CK- LVDS_VDD_EN LVDS_BKLT_EN LVDS_BKLT_CTRL LVDS_IZC_CK LVDS_IZC_DAT	B75 B76 B77 B78 B81 B82 A77 B79 B83 A83 A84	O LVDS O LVDS O LVDS O CMOS O CMOS O CMOS I/O OD CMOS	LVDS LVDS 3.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V	PU 4.7K TO 3.3V	Connect to LVDS connector Connect to LVDS connector Connect to enable control of LVDS panel power circuit Connect to enable control of LVDS panel backlight power circuit. Connect to brightness control of LVDS panel backlight power circuit. Connect to DDC clock of LVDS panel	-LVDS_B_CK-/-) shall have 1000 terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer on-board LVDS channel B differential clock LVDS panel power enable LVDS panel backlight enable LVDS panel backlight brightness control 12C clock output for LVDS display use
LVDS_B2- LVDS_B3+ LVDS_B3- LVDS_B_CK+ LVDS_B_CK+ LVDS_B_CK+ LVDS_WDD_EN LVDS_BKLT_EN LVDS_BKLT_CTRL LVDS_LVDS_I2C_CK LVDS_I2C_DAT LPC Signals Description	875 876 877 878 881 881 82 A77 879 883 A83 A84	O LVDS O LVDS O LVDS O CMOS O CMOS O CMOS I/O OD CMOS I/O OD CMOS	LVDS 3.3V / 3.3V	PU 4.7K TO 3.3V PU 4.7K TO 3.3V	Connect to LVDS connector Connect to LVDS connector Connect to enable control of LVDS panel power circuit Connect to enable control of LVDS panel backlight power circuit. Connect to brightness control of LVDS panel backlight power circuit. Connect to DDC clock of LVDS panel Connect to DDC clock of LVDS panel	-LVDS_B_CK+/-) shall have 1002 terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer on-board LVDS Channel B differential clock LVDS panel power enable LVDS panel backlight enable LVDS panel backlight brightness control 12C clock output for LVDS display use 12C data line for LVDS display use
LVDS_B2- LVDS_B3+ LVDS_B3+ LVDS_B LVDS_B LVDS_B CK+ LVDS_VDD_EN LVDS_BKLT_EN LVDS_BKLT_CTRL LVDS_L2C_CK LVDS_L2C_DAT LPC_Signals_Descriptic Signal	B75 B76 B77 B78 B81 B81 B82 A77 B79 B83 A83 A84	O LVDS O LVDS O LVDS O CMOS O CMOS O CMOS I/O OD CMOS I/O OD CMOS	LVDS LVDS 3.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V	PU 4.7K TO 3.3V	Connect to LVDS connector Connect to LVDS connector Connect to enable control of LVDS panel power circuit Connect to enable control of LVDS panel backlight power circuit. Connect to brightness control of LVDS panel backlight power circuit. Connect to DDC clock of LVDS panel	-LVDS_B_CK-/-) shall have 1000 terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer on-board LVDS channel B differential clock LVDS panel power enable LVDS panel backlight enable LVDS panel backlight brightness control 12C clock output for LVDS display use
LVDS_B2- LVDS_B3+ LVDS_B3+ LVDS_B3- LVDS_B_CK+ LVDS_B_CK+ LVDS_VDD_EN LVDS_B_CK- LVDS_B_CT_EN LVDS_B_CT_CTR_ LV	B75 B76 B77 B78 B81 B81 B82 A77 B79 B83 A83 A84 ODS	O LVDS O LVDS O LVDS O LVDS O CMOS O CMOS O CMOS I/O OD CMOS I/O OD CMOS Module Pin Typ	LVDS 3.3V / 3.3V be Pwr Rail /Tolerance	PU 4.7K TO 3.3V PU 4.7K TO 3.3V	Connect to LVDS connector Connect to LVDS connector Connect to enable control of LVDS panel power circuit Connect to enable control of LVDS panel backlight power circuit. Connect to brightness control of LVDS panel backlight power circuit. Connect to DDC clock of LVDS panel Connect to DDC clock of LVDS panel	-LVDS_B_CK-/-) shall have 1000 terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer-on-board LVDS Channel B differential clock LVDS panel power enable LVDS panel backlight enable LVDS panel backlight rightness control 12C clock output for LVDS display use 12C data line for LVDS display use Description
LVDS B2- LVDS_B3+ LVDS_B3+ LVDS_B B- LVDS_B CK+ LVDS_B CK- LVDS_VDD_EN LVDS_BKLT_EN LVDS_BKLT_CTRL LVDS_LVDS_LVDC_CK LVDS_LVDS_LVDS_LVDS_LVDS_LVDS_LVDS_LVDS_	875 876 877 878 881 881 882 A77 879 883 A83 A84	O LVDS O LVDS O LVDS O CMOS O CMOS O CMOS I/O OD CMOS I/O OD CMOS	LVDS 3.3V / 3.3V	PU 4.7K TO 3.3V PU 4.7K TO 3.3V	Connect to LVDS connector Connect to LVDS connector Connect to enable control of LVDS panel power circuit Connect to enable control of LVDS panel backlight power circuit. Connect to brightness control of LVDS panel backlight power circuit. Connect to DDC clock of LVDS panel Connect to DDC clock of LVDS panel	-LVDS_B_CK+/-) shall have 1002 terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer on-board LVDS Channel B differential clock LVDS panel power enable LVDS panel backlight enable LVDS panel backlight brightness control 12C clock output for LVDS display use 12C data line for LVDS display use
LVDS B2- LVDS_B3+ LVDS_B3+ LVDS B. CR+ LVDS B. CK+ LVDS_VDD_EN LVDS B. CK- LVDS_VDD_EN LVDS_BKLT_EN LVDS_BKLT_CTRL LVDS_L2C_CK LVDS_L2C_DAT LPC_Signals Description Signal LPC_ADO LPC_ADO LPC_ADO LPC_ADO	B75 B76 B77 B78 B81 B81 B82 A77 B79 B83 A83 A83 A83 B81 B85 B86	O LVDS O LVDS O LVDS O LVDS O CMOS O CMOS O CMOS I/O OD CMOS I/O OD CMOS Module Pin Typ	LVDS 3.3V / 3.3V be Pwr Rail /Tolerance	PU 4.7K TO 3.3V PU 4.7K TO 3.3V	Connect to LVDS connector Connect to LVDS connector Connect to enable control of LVDS panel power circuit Connect to enable control of LVDS panel backlight power circuit. Connect to brightness control of LVDS panel backlight power circuit. Connect to DDC clock of LVDS panel Connect to DDC clock of LVDS panel	-LVDS_B_CK-/-) shall have 1000 terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer-on-board LVDS Channel B differential clock LVDS panel power enable LVDS panel backlight enable LVDS panel backlight rightness control 12C clock output for LVDS display use 12C data line for LVDS display use Description
LVDS_B2- LVDS_B3+ LVDS_B3+ LVDS_B3- LVDS_B_CK+ LVDS_B_CK+ LVDS_VDD_EN LVDS_BCK_CTRL LVDS_BKLT_EN LVDS_BKLT_CTRL LVDS_L2C_CK LVDS_L2C_DAT LPC_Signal Description LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD2 LPC_AD3	B75 B76 B77 B78 B81 B82 A77 B79 B83 A83 A84 IONS Pin# B4 B5 B6 B7	O LVDS O LVDS O LVDS O CMOS O CMOS O CMOS I/O OD CMOS	LVDS LVDS 3.3V / 3.3V	PU 4.7K TO 3.3V PU 4.7K TO 3.3V	Connect to LVDS connector Connect to enable control of LVDS panel power circuit Connect to enable control of LVDS panel power circuit Connect to enable control of LVDS panel backlight power circuit. Connect to brightness control of LVDS panel backlight power circuit. Connect to DDC clock of LVDS panel Connect to DDC data of LVDS panel Carrier Board	-LVDS_B_CK-/-) shall have 1000 terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer on-board LVDS Channel B differential clock LVDS panel power enable LVDS panel backlight enable LVDS panel backlight brightness control 12C clock output for LVDS display use 12C data line for LVDS display use Description LPC multiplexed address, command and data bus
LVDS B2- LVDS_B3+ LVDS_B3+ LVDS_B_CK+ LVDS_B_CK+ LVDS_B_CK+ LVDS_B_CK+ LVDS_BKLT_EN LVDS_BKLT_CTRL LVDS_BKLT_CTRL LVDS_BCC_CK LVDS_LCC_CK LVDS_CC_CK LVDS_LCC_CK L	875 876 877 878 881 882 A77 879 883 A83 A84 601 91 84 85 86 87 83 83	O LVDS O LVDS O LVDS O LVDS O CMOS O CMOS O CMOS I/O OD CMOS I/O OD CMOS I/O OD CMOS I/O OD CMOS O CMOS O CMOS O CMOS O CMOS O CMOS O CMOS	LVDS LVDS 3.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V 2.3V / 3.3V 2.3V / 3.3V 2.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V	PU 4.7K TO 3.3V PU 4.7K TO 3.3V	Connect to LVDS connector Connect to LVDS connector Connect to enable control of LVDS panel power circuit Connect to enable control of LVDS panel backlight power circuit. Connect to brightness control of LVDS panel backlight power circuit. Connect to DDC clock of LVDS panel Connect to DDC clock of LVDS panel	-LVDS_B_CK-/-) shall have 1000 terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer-on-board LVDS Channel B differential clock LVDS panel power enable LVDS panel backlight enable LVDS panel backlight brightness control 12c clock output for LVDS display use 12c data line for LVDS display use Description LPC multiplexed address, command and data bus LPC frame indicates the start of an LPC cycle
LIDS B2- LVDS_B3+ LVDS_B3+ LVDS_B3- LVDS_B_CK+ LVDS_B_CK+ LVDS_VDS_B_CK+ LVDS_VDS_B_CK- LVDS_VDS_B_CK- LVDS_BKLT_EN LVDS_BLT_CTRL LVDS_BLZ_CK LVDS_J2C_DAT LPC_Signal Description LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3	B75 B76 B77 B78 B81 B82 A77 B79 B83 A83 A84 IONS Pin# B4 B5 B6 B7	O LVDS O LVDS O LVDS O LVDS O LVDS O CMOS O CMOS O CMOS I/O OD CMOS I/O OD CMOS I/O CMOS I/O CMOS I/O CMOS I/O CMOS I/O CMOS	LVDS LVDS 3.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V 2.3V / 3.3V 2.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V	PU 4.7K TO 3.3V PU 4.7K TO 3.3V HM920	Connect to LVDS connector Connect to enable control of LVDS panel power circuit Connect to enable control of LVDS panel power circuit Connect to enable control of LVDS panel backlight power circuit. Connect to brightness control of LVDS panel backlight power circuit. Connect to DDC clock of LVDS panel Connect to DDC data of LVDS panel Carrier Board	-LVDS_B_CK-/-) shall have 1000 terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer on-board LVDS Channel B differential clock LVDS panel power enable LVDS panel backlight enable LVDS panel backlight brightness control 12C clock output for LVDS display use 12C data line for LVDS display use Description LPC multiplexed address, command and data bus LPC frame indicates the start of an LPC cycle LPC serial DMA request
LVDS_B2- LVDS_B3+ LVDS_B3+ LVDS_B_CK+ LVDS_B_CK+ LVDS_B_CK+ LVDS_VDD_EN LVDS_BKLT_ETR LVDS_BKLT_CTRL LVDS_BKLT_CTRL LVDS_BCCAT LVDS_	B75 B76 B77 B78 B81 B81 B82 A77 B79 B83 A83 A84 OOS Pin# B4 B5 B6 B7 B3 B8 B8 B8	O LVDS O LVDS O LVDS O LVDS O CMOS O CMOS O CMOS I/O OD CMOS I/O OD CMOS I/O OD CMOS I/O OD CMOS O CMOS O CMOS O CMOS O CMOS O CMOS O CMOS	LVDS LVDS 3.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V 2.3V / 3.3V 2.3V / 3.3V 2.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V	PU 4.7K TO 3.3V PU 4.7K TO 3.3V	Connect to LVDS connector Connect to enable control of LVDS panel power circuit Connect to enable control of LVDS panel power circuit Connect to enable control of LVDS panel backlight power circuit. Connect to brightness control of LVDS panel backlight power circuit. Connect to DDC clock of LVDS panel Connect to DDC data of LVDS panel Carrier Board	-LVDS_B_CK-/-) shall have 1000 terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer-on-board LVDS Channel B differential clock LVDS panel power enable LVDS panel backlight enable LVDS panel backlight brightness control 12c clock output for LVDS display use 12c data line for LVDS display use Description LPC multiplexed address, command and data bus LPC frame indicates the start of an LPC cycle

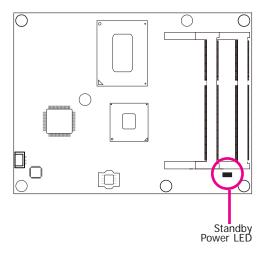
SPI Signals Descriptions Signal	S Pin#	Modulo Din Type	Pwr Rail /Tolerance	HM920	Carrier Board	Description							
SPI_CS#	B97	O CMOS	3.3V Suspend/3.3V	HIVI920	Connect a series resistor 33Ω to Carrier Board SPI Device CS# pin	Chip select for	Corrier Boo	rd CDI mov b	a courand from	a abincat CD	IIO or CDI1		
PI_CS# PI_MISO		I CMOS			-				e sourcea iron	ii criipset SP	10 01 3211		
	A92	O CMOS	3.3V Suspend/3.3V		Connect a series resistor 33Ω to Carrier Board SPI Device SO pin	Data in to Mod							
SPI_MOSI	A95		3.3V Suspend/3.3V		Connect a series resistor 33Ω to Carrier Board SPI Device SI pin	Data out from							
SPI_CLK	A94	O CMOS	3.3V Suspend/3.3V		Connect a series resistor 33Ω to Carrier Board SPI Device SCK pin	Clock from Mo			rood from M	dulo'	nally		
						Power supply							
SPI_POWER	A91	0	3.3V Suspend/3.3V			3.3V. The Mod					ER.		
_			·			Carriers shall u				_POWER			
						shall only be u							
						Selection strap							
						The Carrier sh							
BIOS_DISO#	A34					COM Express I	Module Base	Specification i	Revision 2.1 to	ir strapping	options of BIO	s disable sign	iais.
						BIOS	BIOS	Chipset	Chipset	Carrier	SPI	Bios	Ref
			-			DIS1#	DIS0#	SPI CS1#	SPI CS0#	SPI_CS#		Entry	Line
								Destination	Destination			'	
						1	1	Module	Module	High	Module	SPI0/SPI1	0
		I CMOS	NA			'	'	iviouule	ivioune	підії	Module	3710/3711	0
		1 011100				1	0	Module	Module	High	Module	Carrier FWH	1
							<u> </u>				ļ		
BIOS_DIS1#	B88					0	1	Module	Carrier	SPI0	Carrier	SPI0/SPI1	2
ыоэ_ыэт# I	500							Corri	Module	CDI1	Module	CDIO/CDI4	1 2
I.						0	0	Carrier (Default)	Module (Default)	SPI1 (Default)	Module (Default)	SPI0/SPI1 (Default)	3
								(Delault)	(Delault)	(Delault)	(Delault)	(Delault)	
			1			-1							
VGA Signals Description	is												
Signal	Pin#		Pwr Rail /Tolerance	HM920	Carrier Board	Description							
VGA_RED	B89	O Analog	Analog	PD 150 TO GND	PD 150R,connect to VGA connector with EMI filter & ESD protect component.	Red for monitor	or. Analog o	utput					
/GA_GRN	B91	O Analog	Analog	PD 150 TO GND	PD 150R,connect to VGA connector with EMI filter & ESD protect component.	Green for mor							
/GA_BLU	B92	O Analog	Analog	PD 150 TO GND	PD 150R,connect to VGA connector with EMI filter & ESD protect component.	Blue for monit							
VGA_HSYNC	B93	O CMOS	3.3V / 3.3V		Connect to VGA connector with a3.3V Buffer IC to isolate PCH & Display Device		c output to \	/GA monitor					
VGA_VSYNC	B94	O CMOS	3.3V / 3.3V		Connect to VGA connector with a 33V Buffer IC to isolate PCH & Display Device	Vertical sync of	utput to VG	A monitor					
VGA_I2C_CK	B95	I/O OD CMOS	3.3V / 3.3V	PU 2.2K TO 3.3V	Connect to VGA connector with a 3.3V to 5V Level shift circuit.	DDC clock line	(I2C port de	edicated to ide	ntify VGA mon	itor capabili	ities)		
VGA_I2C_DAT	B96	I/O OD CMOS	3.3V / 3.3V	PU 2.2K TO 3.3V	Connect to VGA connector with a 3.3V to 5V Level shift circuit.	DDC data line.							
	S					_							
IDE Signals Descriptions Signal	Pin#	Module Pin Type	e Pwr Rail /Tolerance	HM920	Carrier Board	Description							
Signal IDE_D0	Pin# D7	Module Pin Type	Pwr Rail /Tolerance	HM920	Carrier Board	Description							
Signal IDE_D0 IDE_D1	Pin# D7 C10	Module Pin Type	Pwr Rail /Tolerance	HM920	Carrier Board	Description							
Signal IDE_D0 IDE_D1 IDE_D2	Pin# D7 C10 C8	Module Pin Type	Pwr Rail /Tolerance	HM920	Carrier Board	Description							
Signal IDE_DO IDE_D1 IDE_D2 IDE_D3	Pin# D7 C10 C8 C4	Module Pin Type	Pwr Rail /Tolerance	HM920	Carrier Board	Description							
Signal IDE_D0 IDE_D1 IDE_D2 IDE_D3 IDE_D4	Pin# D7 C10 C8 C4 D6	Module Pin Type	Pwr Rail /Tolerance	HM920	Carrier Board	Description							
Signal IDE_DO IDE_D1 IDE_D2 IDE_D3 IDE_D4 IDE_D5	Pin# D7 C10 C8 C4	Module Pin Type	Pwr Rail /Tolerance	НМ920	Carrier Board	Description							
Signal	Pin# D7 C10 C8 C4 D6 D2 C3	Module Pin Type	e Pwr Rail /Tolerance	НМ920	Carrier Board	Description							
Signal	Pin# D7 C10 C8 C4 D6 D2 C3 C2			HM920	Carrier Board		ata to / from) IDE dovice					
Signal DIDE_DO DIDE_DO DIDE_DT DIDE_DT	Pin# D7 C10 C8 C4 D6 D2 C3 C2 C6	Module Pin Type	Pwr Rail /Tolerance	HM920	Carrier Board	Description Bidirectional d	ata to / from	n IDE device.					
Signal IDE_DO IDE_DI IDE_DZ IDE_D3 IDE_D4 IDE_D5 IDE_D6 IDE_D7 IDE_D8 IDE_D8 IDE_D9	Pin# D7 C10 C8 C4 D6 D2 C3 C2 C6 C7			HM920	Carrier Board		ata to / from	n IDE device.					
Signal	Pin# D7 C10 C8 C4 D6 D2 C3 C2 C6			HM920	Carrier Board		ata to / from	n IDE device.					
Signal DEE_DO	Pin# D7 C10 C8 C4 D6 D2 C3 C2 C6 C7			НМ920	Carrier Board		ata to / from	n IDE device.					
Signal IDE_DO IDE_DI IDE_DI	Pin# D7 C10 C8 C4 D6 D2 C3 C2 C6 C7 D3			HM920	Carrier Board		ata to / from	n IDE device.					
Signal	Pin# D7 C10 C8 C4 D6 D2 C3 C2 C6 C7 D3 D4			HM920	Carrier Board		ata to / from	n IDE device.					
Signal DE_ DO	Pin# D7 C10 C8 C4 D6 D2 C3 C2 C6 C7 D3 D4 D5			HM920	Carrier Board		ata to / from	n IDE device.					
Signal DE_DO	Pin# D7 C10 C8 C4 D6 D2 C3 C2 C6 C7 D3 D4 D5 C7 D3 C7 D3 C7 D3 C7 D3 D4 D5 C9 C12			HM920	Carrier Board		ata to / from	n IDE device.					
Signal	Pin# D7 C10 C8 C4 D6 D2 C3 C3 C2 C6 C7 D3 D4 D5 C9 C12 C5			HM920	Carrier Board		ata to / from	n IDE device.					
Signal DIE_DO DIE_DO	Pin# D7 C10 C8 C4 D6 D2 C3 C2 C6 C7 D3 D4 D5 C9 C12 C5 C5 C9 C12 C5 D13	I/O CMOS	3.3V /5V	HM920	Carrier Board	Bidirectional d							
Signal IDE_DO IDE_DI IDE_DI	Pin# D7 C10 C8 C4 D6 D2 C3 C2 C6 C7 D3 D4 D5 C9 C12 C5 D13 D14 D5 D14			HM920	Carrier Board								
Signal IDE_DO IDE_DI IDE_DI IDE_DZ IDE_D3 IDE_D4 IDE_D5 IDE_D6 IDE_D7 IDE_D8 IDE_D9 IDE_D9 IDE_D10 IDE_D11 IDE_D12 IDE_D13 IDE_D13 IDE_D14 IDE_D15 IDE_D15 IDE_D16 IDE_D17 IDE_D18 IDE_D19 IDE_D	Pin# D7 C10 C8 C4 D6 D2 C3 C2 C6 C7 D3 D4 D5 C9 C12 C5 D13 D4 D5 C9 C12 C5 D13 D14 D15	I/O CMOS	3.3V / 5V 3.3V / 3.3V	HM920	Carrier Board	Bidirectional d	to IDE device	3 .					
Signal DIE_DO DIE_DI DIE_DI	Pin# D7 C10 C8 C4 D6 D2 C3 C2 C6 C7 D3 D4 D5 C9 C12 C5 D13 D14 D5 D14	I/O CMOS	3.3V /5V	HM920	Carrier Board	Address lines	to IDE device	e.					
Signal IDEE_DO IDEE_DO IDEE_DT IDEE_	Pin# D7 C10 C8 C4 D6 D2 C3 C2 C6 C7 D3 D4 D5 C9 C12 C5 D13 D14 D15 D9	I/O CMOS O CMOS O CMOS	3.3V / 5.V 3.3V / 3.3V 3.3V / 3.3V	HM920	Carrier Board	Address lines I/O write line Data latched of	to IDE device to IDE device on trailing (ri	e. e. sing) edge.					
Signal DIE DO DIE DO DIE DI DE DI DI	Pin# D7 C10 C8 C4 D6 D2 C3 C2 C6 C7 D3 D4 D5 C9 C12 C5 D13 D14 D15 D9 C14	I/O CMOS O CMOS O CMOS O CMOS	3.3V / 5.V 3.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V		Carrier Board	Address lines I//O write line Data latched li/O readd line t	to IDE device to IDE device on trailing (ri o IDE device	e. e. sing) edge.					
Signal	Pin# D7 C10 C8 C4 D6 D2 C3 C2 C6 C7 D3 D4 D5 C9 C12 C5 D13 D14 D15 D9	I/O CMOS O CMOS O CMOS	3.3V / 5.V 3.3V / 3.3V 3.3V / 3.3V	HM920 PU 5.6K TO GND	Carrier Board	Address lines I/O write line Data latched c I/O read line t IDE Device DM	to IDE device to IDE device on trailing (ri o IDE device MA Request.	e. sing) edge.	st a data trans	fer			
Signal DEE DO DEE DO	Pin# D7 C10 C8 C4 D6 D2 C3 C2 C6 C7 D3 D4 D5 C9 C12 C5 D13 D14 D15 D9 C14 D8	I/O CMOS O CMOS O CMOS I CMOS	3.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V		Carrier Board	Address lines I/O write line Data latched o I/O read line t IDE Device DM It is asserted it	to IDE device to IDE device on trailing (ri o IDE device MA Request. by the IDE d	e. sing) edge. e.	st a data trans	fer.			
Signal DE DO DE DO DE DO DE DI DE DO DE	Pin# D7 C10 C8 C4 D6 D2 C3 C2 C6 C7 D3 D4 D5 C9 C12 C5 D13 D14 D15 D9 C14 D8 D10	I/O CMOS O CMOS O CMOS I CMOS O CMOS O CMOS	3.3V / 5V 3.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V		Carrier Board	Address lines li/O write line Data latched of I/O read line to I/O read li	to IDE device on trailing (ri o IDE device MA Request. oy the IDE d MA Acknowle	e. sing) edge. evice to reque! dge.		fer.			
Signal DEE DO DEE DO	Pin# D7 C10 C8 C4 D6 D2 C3 C2 C6 C6 C7 D3 D4 D5 C9 C12 C5 D13 D14 D15 D9 C14 D8 D9 C14 D8	O CMOS O CMOS I CMOS O CMOS O CMOS O CMOS O CMOS	3.3V / 5.V 3.3V / 3.3V 3.3V / 3.3V 3.3V / 5.V 3.3V / 3.3V 3.3V / 3.3V		Carrier Board	Address lines i I/O write line Data latched o I/O read line t	to IDE device to IDE device to IDE device on IDE device MA Request. by the IDE d MA Acknowle ip Select for	e. sing) edge. evice to reque: dge. 1F0h to 1FFh	range.	fer.			
	Pin# D7 C10 C8 C4 D6 D2 C3 C2 C6 C7 D3 D4 D5 C9 C12 C5 D13 D14 D15 D9 C14 D8 D10 D16 D17	O CMOS	3.3V / 3.3V 3.3V / 3.3V	PU 5.6K TO GND	Carrier Board	Address lines I/O write line Data latched of I/O read line t IDE Device Dh IDE Device Dh IDE Device Ch	to IDE device to IDE device on trailing (ri o IDE device AA Request. by the IDE d AA Acknowled ip Select for ip Select for	e. sing) edge. evice to reque: dge. 1F0h to 1FFh 3F0h to 3FFh	range.	fer.			
Signal DEE DO DEE DO	Pin# D7 C10 C8 C4 D6 D2 C3 C2 C6 C6 C7 D3 D4 D5 C9 C12 C5 D13 D14 D15 D9 C14 D8 D9 C14 D8	O CMOS O CMOS I CMOS O CMOS O CMOS O CMOS O CMOS	3.3V / 5.V 3.3V / 3.3V 3.3V / 3.3V 3.3V / 5.V 3.3V / 3.3V 3.3V / 3.3V		Carrier Board	Address lines I/O write line Data latched of I/O read line t I/O read line t I/O sasserted I/O E Device Dh	to IDE device to IDE device to IDE device IDE device IA Request. by the IDE d IA Acknowle ip Select for ip ready input	e. sing) edge. evice to reque: dge. 1F0h to 1FFh 3F0h to 3FFh	range. range.	fer.			
	Pin# D7 C10 C8 C4 D6 D2 C3 C2 C3 C2 C6 C7 D3 D4 D5 C9 C12 C5 D13 D14 D15 D9 C14 D8 D10 D10 D16 D17 C13	I/O CMOS O CMOS O CMOS I CMOS O CMOS O CMOS I CMOS O CMOS O CMOS I CMOS I CMOS	3.3V / 3.3V 3.3V / 3.3V	PU 5.6K TO GND	Carrier Board	Address lines I/O write line Data latched of I/O read line to IDE Device Dh IDE Device Ch	to IDE device to IDE device on trailing (ri o IDE device AA Request. oy the IDE d MA Acknowle ip Select for o ready input the IDE devi	e. sing) edge. evice to reque: dge. 1F0h to 1FFh 3F0h to 3FFh	range. range.	fer.			
Signal DIE DO DIE DO	Pin# D7 C10 C8 C4 D6 D2 C3 C2 C6 C7 D3 D4 D5 C9 C12 C5 D13 D14 D15 D9 C14 D15 D9 C14 D8 D10 D16 D17 C13 D18	I/O CMOS O CMOS O CMOS I CMOS O CMOS O CMOS I CMOS I CMOS I CMOS I CMOS I CMOS	3.3V / 5.V 3.3V / 3.3V	PU 5.6K TO GND PU 4.7K TO 3.3V	Carrier Board	Address lines I/O write line: Data latched of I/O read line t IDE Device Dh IDE Device Ch IDE Reset output	to IDE device to IDE device to IDE device AR Request. by the IDE d AA Acknowle ip Select for D ready input the IDE devi	e. sing) edge e. dge. 1F0h to 1FFh 3Fi 4F0, active low	range. range.	fer.			
Signal DE DO DE DO DE DO DE DI DE DI DE DO DE	Pin# D7 C10 C8 C4 D6 D2 C3 C2 C3 C2 C6 C7 D3 D4 D5 C9 C12 C5 D13 D14 D15 D9 C14 D8 D10 D10 D16 D17 C13	I/O CMOS O CMOS O CMOS I CMOS O CMOS O CMOS I CMOS O CMOS O CMOS I CMOS I CMOS	3.3V / 3.3V 3.3V / 3.3V	PU 5.6K TO GND	Carrier Board	Address lines I/O write line Data latched of I/O read line to I/O read lin	to IDE devices to IDE devices trailing (ri o IDE device MA Request. by the IDE d MA Acknowle ip Select for o ready input the IDE device set from IDE device set from IDE devices to IDE devices the IDE device	e. e. sing) edge. e. evice to reque: dge. 1760 to 1FFh 3760 to 3FFh i. ce to extend th a, active low.	range. range. he cycle.		ein		
	Pin# D7 C10 C8 C4 D6 D2 C3 C2 C3 C2 C6 C7 D3 D4 D5 C9 C12 C5 D13 D14 D15 D9 C14 D8 D10 D16 D17 C13 D18 D12	O CMOS O CMOS O CMOS I CMOS O CMOS O CMOS I CMOS O CMOS I CMOS I CMOS I CMOS	3.3V / 5.V 3.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V 3.3V / 5.V 3.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V 3.3V / 5.V	PU 5.6K TO GND PU 4.7K TO 3.3V	Carrier Board	Address lines : I/O write line Data latched of I/O read line t IDE Device Dh II is asserted I IDE Device (I) IDE Device (I) IDE Device (I) IDE device I/C Pulled low by Reset output I Interrupt requ Input from off	to IDE device on trailing (ri o IDE device AR Request. y the IDE d AR Acknowle ip Select for ip Select for ready input the IDE device of IDE device set from IDE Module har	e. sing) edge. e. evice to reque: dge. 1F0h to 1FFh 3F0h to 3FFh i. e to extend th a, active low. device.	range. range. ne cycle.	IDE cable be			
Signal DE DO DE DO DE DO DE DI DE DI DE DO DE	Pin# D7 C10 C8 C4 D6 D2 C3 C2 C6 C7 D3 D4 D5 C9 C12 C5 D13 D14 D15 D9 C14 D15 D9 C14 D8 D10 D16 D17 C13 D18	I/O CMOS O CMOS O CMOS I CMOS O CMOS O CMOS I CMOS I CMOS I CMOS I CMOS I CMOS	3.3V / 5.V 3.3V / 3.3V	PU 5.6K TO GND PU 4.7K TO 3.3V	Carrier Board	Address lines I I/O write line Data latched of I/O read line t I/O read line	to IDE devictor IDE devictor IDE device on trailing (ri or IDE device AM Request. by the IDE of AM Acknowled ip Select for or ready input the IDE device of	e. sing) edge	range. range. he cycle. ng the type of for legacy IDE	IDE cable be	w		
	Pin# D7 C10 C8 C4 D6 D2 C3 C2 C3 C2 C6 C7 D3 D4 D5 C9 C12 C5 D13 D14 D15 D9 C14 D8 D10 D16 D17 C13 D18 D12	O CMOS O CMOS O CMOS I CMOS O CMOS O CMOS I CMOS O CMOS I CMOS I CMOS I CMOS	3.3V / 5.V 3.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V 3.3V / 5.V 3.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V 3.3V / 5.V	PU 5.6K TO GND PU 4.7K TO 3.3V PU 10K TO GND	Carrier Board	Address lines : I/O write line Data latched of I/O read line t IDE Device Dh II is asserted I IDE Device (I) IDE Device (I) IDE Device (I) IDE device I/C Pulled low by Reset output I Interrupt requ Input from off	to IDE device to IDE device on trailing (ri o IDE device on trailing (ri o IDE device on IDE device	e. sing) edge. cvice to reque: dge. 1F0h to 1FFh 3F0h to 3FFh . ce to extend th 2, active low. ddwize lowication in cable used ble with interflu	range. range. he cycle. ng the type of for legacy IDE eaved grounds	IDE cable be modes. Low is used. Su	w		

Miscellaneous Sign			I			
ignal	Pin#		Pwr Rail /Tolerance	HM920	Carrier E	
2C_CK	B33		3.3V Suspend/3.3V	PU 2.2K to 3.3VSB		General purpose I2C port clock output
2C_DAT	B34	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3.3VSB		General purpose I2C port data I/O line
						Output for audio enunciator - the "speaker" in PC-AT systems.
SPKR	B32	O CMOS	3.3V / 3.3V			This port provides the PC beep signal and is mostly intended for
						debugging purposes.
VDT	B27	O CMOS	3.3V / 3.3V			Output indicating that a watchdog time-out event has occurred.
	+	*	+			1 2 2
ower and System					T	
gnal	Pin#	Module Pin Type	Pwr Rail /Tolerance	HM920	Carrier E	
						A falling edge creates a power button event. Power button events can
WRBTN#	B12	I CMOS	3.3V Suspend/3.3V	PU 10K TO 3.3VSB	PU 4.7K TO 3.3VSB	be used to bring a system out of S5 soft off and other suspend states,
						as well as powering the system down.
						Reset button input. Active low request for Module to reset and reboot.
YS RESET#	B49	I CMOS	3.3V Suspend/3.3V	PU 10K TO 3.3VSB	NC PU 4.7K TO 3.3VSB	May be falling edge sensitive. For situations when SYS_RESET# is
IJ_NLJEI#	D47	1 CIVIUS	a.av auspenu/a.aV	PU 10K 10 3.3V3B	NG FU 4./K TU 3.3V3D	not able to reestablish control of the system, PWR_OK or a power
			<u> </u>			cycle may be used.
						Reset output from Module to Carrier Board. Active low. Issued by
						Module chipset and may result from a low SYS_RESET# input, a low
B_RESET#	B50	O CMOS	3.3V Suspend/3.3V			PWR_OK input, a VCC_12V power input that falls below the minimum
						specification, a watchdog timeout, or may be initiated by the Module
						software.
			1			
						Power OK from main power supply. A high value indicates that the
WR_OK	B24	I CMOS	3.3V / 3.3V	PU 10K TO 3.3V		power is good. This signal can be used to hold off Module startup to
WK_OK	B24	I CIVIOS	3.34 / 3.34	FO TOK TO 3.3V		allow Carrier based FPGAs or other configurable devices time to be
						programmed.
US_STAT#	B18	O CMOS	3.3V Suspend/3.3V			Indicates imminent suspend operation; used to notify LPC devices.
						Indicates system is in Suspend to RAM state. Active low output. An
US_S3#	A15	O CMOS	3.3V Suspend/3.3V			inverted copy of SUS_S3# on the Carrier Board may be used to
						enable the non-standby power on a typical ATX supply.
US_S4#	A18	O CMOS	3.3V Suspend/3.3V			Indicates system is in Suspend to Disk state. Active low output.
US_S5#	A24	O CMOS	3.3V Suspend/3.3V			Indicates system is in Soft Off state.
VAKEO#	B66	I CMOS	3.3V Suspend/3.3V	PU 1K TO 3.3VSB		PCI Express wake up signal.
TAKEO#	500	1 CIVIOS	3.5V Suspend/3.5V	10 IK 10 3.3V3B		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
VAKE1#	B67	I CMOS	3.3V Suspend/3.3V	PU 10K TO 3.3VSB		General purpose wake up signal. May be used to implement wake-up
						on PS2 keyboard or mouse activity.
						Indicates that external battery is low.
ATLOW#	A27	I CMOS	3.3V Suspend/ 3.3V	PU 8.2K TO 3.3VSB		This port provides a battery-low signal to the Module for orderly
						transitioning to power saving or power cut-off ACPI modes.
HRM#	B35	I CMOS	3.3V / 3.3V	PU 10K TO 3.3V		Input from off-Module temp sensor indicating an over-temp situation.
HRMTRIP#	A35	O CMOS	3.3V / 3.3V	PU 10K TO 3.3V		Active low output indicating that the CPU has entered thermal shutdown.
MB_CK	B13	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K TO 3.3VSB	NC PU 4.7K TO 3.3VSB	System Management Bus bidirectional clock line.
MB_DAT	B14	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K TO 3.3VSB	NC PU 4.7K TO 3.3VSB	System Management Bus bidirectional data line.
MB_ALERT#	B15	I CMOS	3.3V Suspend/3.3V			System Management Bus Alert – active low input can be used to
VID_ALCK I#	010	1 CIVIUS	a.av auspenu/a.aV			generate an SMI# (System Management Interrupt) or to wake the system.
PIO Signals Desci			In			
gnal	Pin#	Module Pin Type	Pwr Rail /Tolerance	HM920	Carrier E	pard Description
PO0	A93		1			
PO1	B54	O CMOS	3.3V / 3.3V			General purpose output pins.
PO2	B57	5 014105	0.00 / 0.00			Upon a hardware reset, these outputs should be low.
PO3	B63					
PI0	A54			PU 100K to 3.3V		
GPI1	A63	I CMOS	3.3V / 3.3V	PU 100K to 3.3V		General purpose input pins.
GPI2	A67	1 CIVIUS	J.JV / J.JV	PU 100K to 3.3V		Pulled high internally on the Module.

Chapter 3

Power and GND Signal Descriptions									
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	HM920	Carrier Board	Description			
VCC_12V	A104~A109 B104~B109 C104~C109 D104~D109	Power				Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.			
VCC_5V_SBY	B84~B87	Power				Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.			
VCC_RTC	A47	Power				Real-time clock circuit-power input. Nominally +3.0V.			
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A96, A100, A110, B1, B11, B21, B31, B41, B51, B60, B70, B100, B110, C1, C11, C21, C31, C41, C51, C60, C70, C76, C80, C84, C87, C90, C93, C96, C110, D1, D11, D21, D31, D41 D51, D60, D67, D70, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110, D103,	rowei				Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.			

Standby Power LED



This LED will light when the system is in the standby mode.

Cooling Option

Heat Spreader with Heat Sink and Fan



Note:

The system board used in the following illustrations may not resemble the actual board. These illustrations are for reference only.



Top View of the Heat Sink



Bottom View of the Heat Sink

• "1" and "2" denote the locations of the thermal pads designed to contact the corresponding components that are on HM920-QM87/HM86.



Important:

Remove the plastic covering from the thermal pads prior to mounting the heat sink onto HM920-QM87/HM86.

Installing HM920-QM87/HM86 onto a Carrier Board

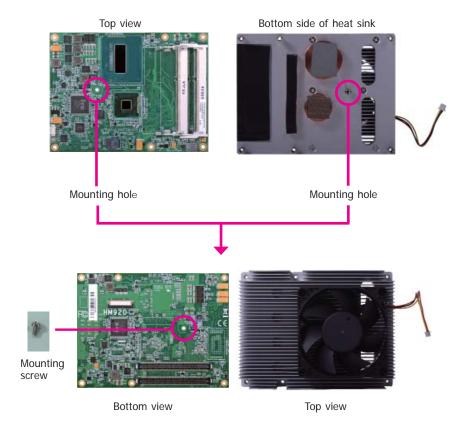


Important:

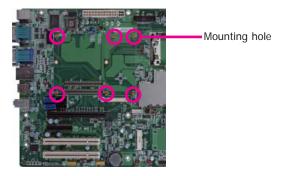
The carrier board (COM330-B) used in this section is for reference purpose only and may not resemble your carrier board. These illustrations are mainly to guide you on how to install HM920-QM87/HM86 onto the carrier board of your choice.

To download COM330-B datasheet and manual

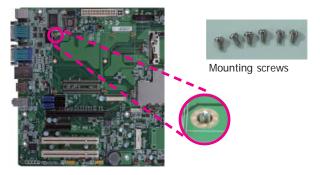
 Use the provided screw to install the heatsink onto the module. First align the mounting hole on the heatsink with the mounting hole on the module and then secure them with the provided screw from the bottom side of the module. The module and heatsink assembly should look like the one shown below.



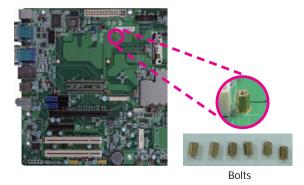
2. Now install the module and heatsink assembly onto the carrier board. The photo below shows the locations of the mounting holes on carrier board.



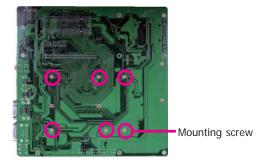
3. Insert the provided mounting screws into the mounting holes - from the bottom through the top of the carrier board.



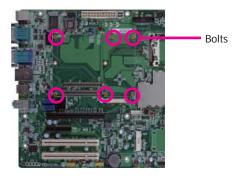
4. While supporting the mounting screw at the bottom, from the top side of the board, fasten a bolt into the screw.



5. The photo below shows the solder side of the board with the screws already fixed in place.



6. The photo below shows the component side of the board with the bolts already fixed in place.



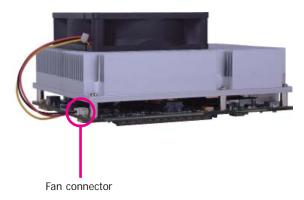
7. Position the heat sink on the top of HM920-QM87/HM86 with the heat sink's mounting holes aligned with HM920-QM87/HM86 mounting holes. Insert one of the provided long screws into the mounting hole shown in the photo below.



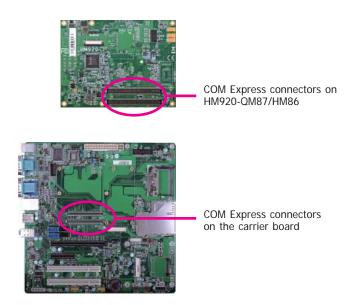


Long screw

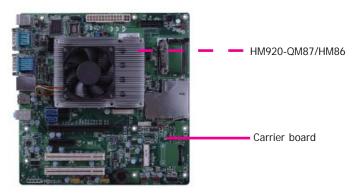
8. From the bottom of the board, fasten the provided bolt into the screw and then connect the heat spreader/heat spreader with heat sink and fan's cable to the fan connector on HM920-QM87/HM86.



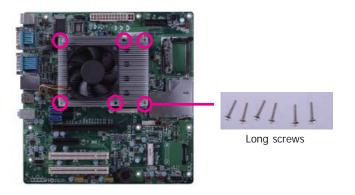
 Grasping HM920-QM87/HM86 by its edges, position it on the top of the carrier board with its mounting holes aligned with the bolts on the carrier board. This will also align the COM Express connectors of the two boards to each other.



10. Press HM920-QM87/HM86 down firmly until it is completely seated on the COM Express connectors of the carrier board.



11. Use the provided mounting screws to secure HM920-QM87/HM86 with heat sink to the carrier board. The photo below shows the locations of the long mounting screws.



Installing the COM Express Debug Card

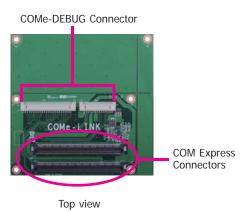
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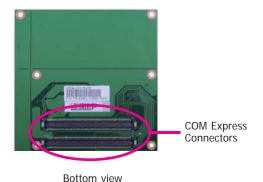
Note:

The system board used in the following illustrations may not resemble the actual board. These illustrations are for reference only.

 COMe-LINK1 is the COM Express debug card designed for COM Express Compact and Basic modules to debug and display signals and codes of COM Express modules.

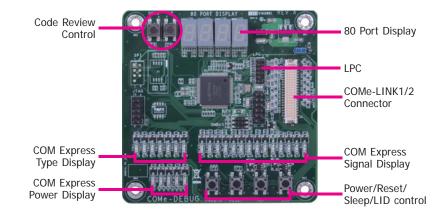
COMe-LINK1 (For Compact/Basic modules)

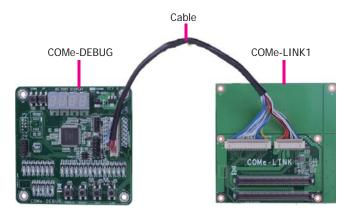




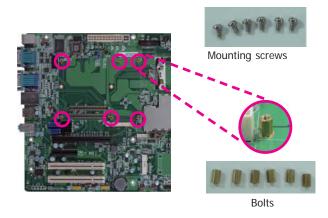
2. Connect the COMe-DEBUG card to COMe-LINK1 via a cable.

COMe-DEBUG

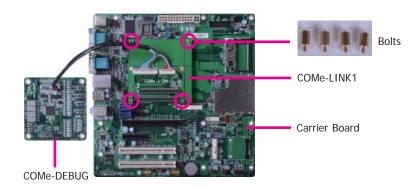




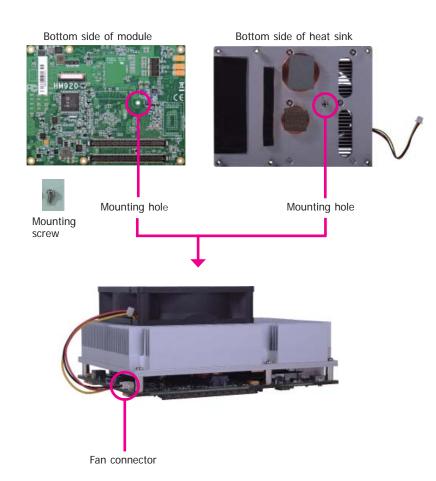
3. Fasten bolts with mounting screws through mounting holes to be fixed in place.



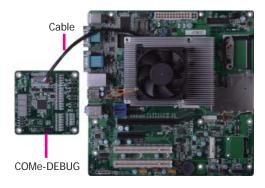
4. Use the provided bolts to fix the COMe-LINK1 debug card onto the carrier board.



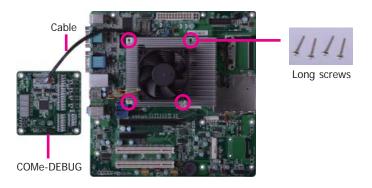
Align the mounting hole on the heat sink with the mounting hole on the module and secure the heat sink onto the module by a mounting screw from the bottom side of the module.

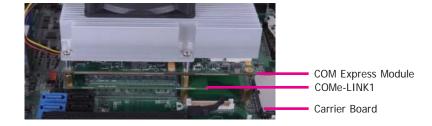


6. Grasp HM920-QM87/HM86 with the heat sink by its edges and position them down firmly on the top of the COMe-LINK1 debug card.



7. Use the long mounting screws to secure them on the top of the COMe-LINK1 debug card and the carrier board. The photo below shows the locations of long mounting screws.





Side View of the Module, Debug Card and Carrier Board

Chapter 4 - BIOS Setup

Overview

The BIOS is a program that takes care of the basic level of communication between the CPU and peripherals. It contains codes for various advanced features found in this system board. The BIOS allows you to configure the system and save the configuration in a battery-backed CMOS so that the data retains even when the power is off. In general, the information stored in the CMOS RAM of the EEPROM will stay unchanged unless a configuration change has been made such as a hard drive replaced or a device added. It is possible that the CMOS battery will fail causing CMOS data loss. If this happens, you need to install a new CMOS battery and reconfigure the BIOS settings.



Note:

The BIOS is constantly updated to improve the performance of the system board; therefore the BIOS screens in this chapter may not appear the same as the actual one. These screens are for reference purpose only.

Default Configuration

Most of the configuration settings are either predefined according to the Load Optimal Defaults settings which are stored in the BIOS or are automatically detected and configured without requiring any actions. There are a few settings that you may need to change depending on your system configuration.

Entering the BIOS Setup Utility

The BIOS Setup Utility can only be operated from the keyboard and all commands are keyboard commands. The commands are available at the right side of each setup screen.

The BIOS Setup Utility does not require an operating system to run. After you power up the system, the BIOS message appears on the screen and the memory count begins. After the memory test, the message "Press DEL to run setup" will appear on the screen. If the message disappears before you respond, restart the system or press the "Reset" button. You may also restart the system by pressing the <Ctrl> <Alt> and keys simultaneously.

Legends

KEYs	Function
Right and Left Arrows	Moves the highlight left or right to select a menu.
Up and Down Arrows	Moves the highlight up or down between submenus or fields.
<esc></esc>	Exits to the BIOS setup utility
+ (plus key)	Scrolls forward through the values or options of the hightlighted field.
- (minus key)	Scolls backward through the values or options of the hightlighted field.
<f1></f1>	Displays general help
<f2></f2>	Displays previous values
<f3></f3>	Optimized defaults
<f4></f4>	Saves and resets the setup program.
<enter></enter>	Press <enter> to enter the highlighted submenu</enter>

Scroll Bar

When a scroll bar appears to the right of the setup screen, it indicates that there are more available fields not shown on the screen. Use the up and down arrow keys to scroll through all the available fields.

Submenu

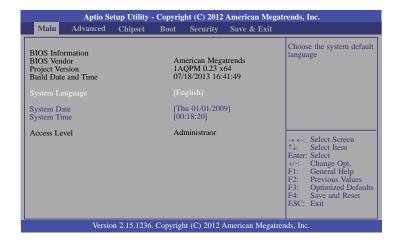
When ">" appears on the left of a particular field, it indicates that a submenu which contains additional options are available for that field. To display the submenu, move the highlight to that field and press <Enter>.

Chapter 4 BIOS Setup www.dfi.com

AMI BIOS Setup Utility

Main

The Main menu is the first screen that you will see when entering the BIOS Setup Utility.



System Date

The date format is <day>, <month>, <date>, <year>. Day displays a day, from Sunday to Saturday. Month displays the month, from January to December. Date displays the date, from 1 to 31. Year displays the year, from 1980 to 2099.

System Time

The time format is <hour>, <minute>, <second>. The time is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Hour displays hours from 00 to 23. Minute displays minutes from 00 to 59. Second displays seconds from 00 to 59.

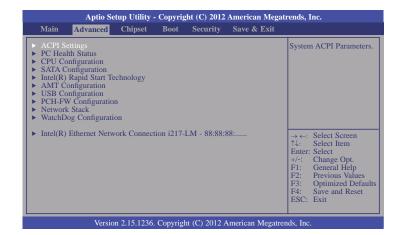
Advanced

The Advanced menu allows you to configure your system for basic operation. Some entries are defaults required by the system board, while others, if enabled, will improve the performance of your system or let you set some features according to your preference.



Important:

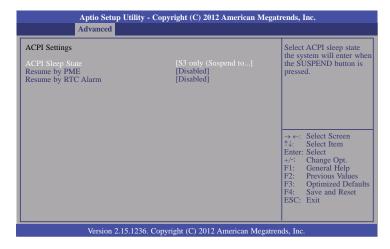
Setting incorrect field values may cause the system to malfunction.



Chapter 4 BIOS Setup www.dfi.com

ACPI Settings

This section is used to configure the ACPI settings.



ACPI Sleep State

Select the highest ACPI sleep state that the system will enter when the Suspend button is pressed.

S3(STR) Enable the Suspend to RAM function.

Resume by PME

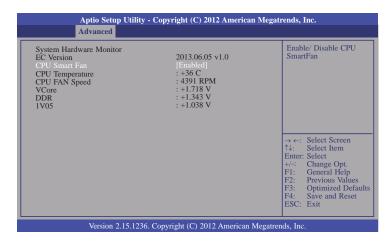
Enable this field to use the PME signal to wake up the system (via PCI, PCIE and onboard LAN).

Resume by RTC Alarm

When Enabled, the system uses the RTC to generate a wakeup event.

PC Health Status

This section only displays hardware health monitor.



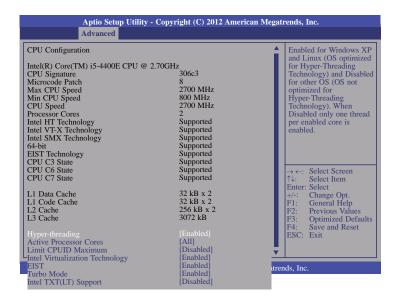
CPU Smart Fan

When this feature is enabled, the speed of CPU's fan will rotate according to the CPU's temperature. The higher the temperature, the faster the speed of rotation.

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CPU Configuration

This section is used to configure the CPU. It will also display the detection of CPU information.



Hyper-threading

Enable this field for Windows XP and Linux which are optimized for Hyper-Threading technology. Select disabled for other OSes not optimized for Hyper-Threading technology. When disabled, only one thread per enabled core is enabled.

Active Processor Cores

Number of cores to enable in each processor package.

Limit CUPID Maximum

The CPUID instruction of some newer CPUs will return a value greater than 3. The default is Disabled because this problem does not exist in the Windows series operating systems. If you are using an operating system other than Windows, this problem may occur. To avoid this problem, enable this field to limit the return value to 3 or less than 3.

Intel Virtualization Technology

When this field is set to Enabled, the VMM can utilize the additional hardware capabilities provided by the Intel Virtualization technology. A full reset is required to change the setting.

EIST

This field is used to enable or disable the Intel Enhanced SpeedStep Technology.

Turbo Mode

If you want the system to run at a faster speed, set this field to Enabled. However, compatibility problems may occur with some DRAMs if the system is running in Turbo mode. If you encounter this problem, set this field to Disabled.

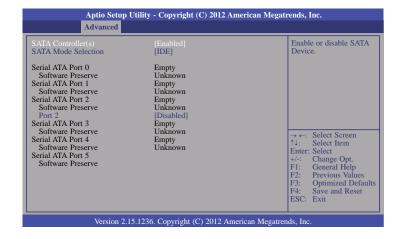
Intel TXT(LT) Support

Enable or disable the support of Intel Trusted Execution technology.

Chapter 4 BIOS Setup www.dfi.com

SATA Configuration

This section is used to configure the settings of SATA device.



SATA Controller(s)

This field is used to enable or disable the Serial ATA device.

SATA Mode Selection

The mode selection determines how the SATA controller(s) operates.

IDE Mode

This option configures the Serial ATA drives as Parallel ATA storage devices.

AHCI Mode

This option allows the Serial ATA devices to use AHCI (Advanced Host Controller Interface).

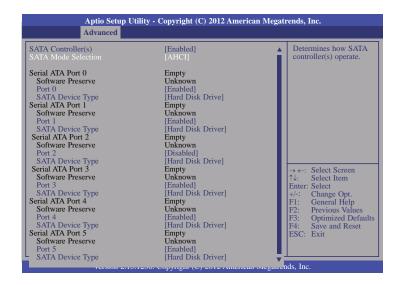
RAID Mode

This option allows the Serial ATA devices to use RAID 0/1/5/10/Recovery (Redundant Array of Independent Disks).

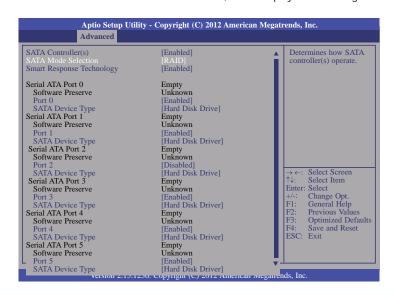
Port 2

This field is used to enable or disable the function of the onboard IDE device, and the default value is disable. When you use the onboard IDE device, you must enable the port 2.

When AHCI is selected in the SATA Mode Selection, it will display the following information:



When RAID is selected in the SATA Mode Selection, it will display the following information:



Chapter 4 BIOS Setup www.dfi.com

Smart Response Technology

This field is used to enable or disable the Smart Response Technology.

Port 0 to Port 5

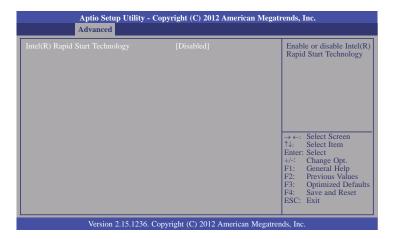
Enable or disable the Serial ATA port.

SATA Device Type

Identify the Serial ATA port is connected to Solid State Drive or Hard Disk Drive.

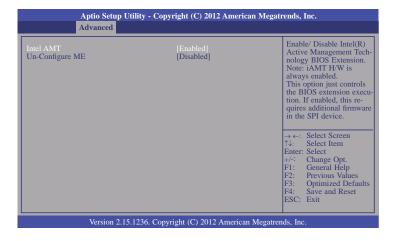
Intel(R) Rapid Start Technology

This section is used to enable or disable the Intel Rapid Start Technology.



AMT Configuration

This section configures the parameters of Active Management Technology.



Intel AMT

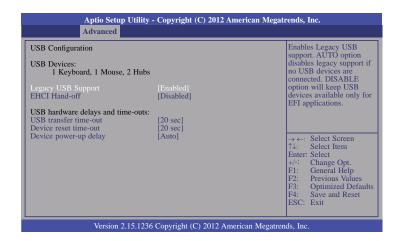
Enable or disable the AMT function.

Un-Configure ME

Select Enabled to un-configure the ME function without a password.

USB Configuration

This section is used to configure the parameters of USB device.



Legacy USB Support

Enabled

Enables legacy USB.

Auto

Disables support for legacy when no USB devices are connected.

Disabled

Keeps USB devices available only for EFI applications.

EHCI Hand-off

This is a workaround for OSes that does not support EHCI hand-off. The EHCI owner-ship change should be claimed by the EHCI driver.

USB transfer time-out

The time-out value for Control, Bulk and Interrupt transfers.

Device reset time-out

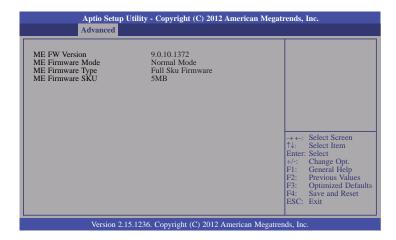
Select the USB mass storage device start unit command timeout.

Device power-up delay

Maximum time the device will take before it properly reports itself to the Host Controller. "Auto" uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.

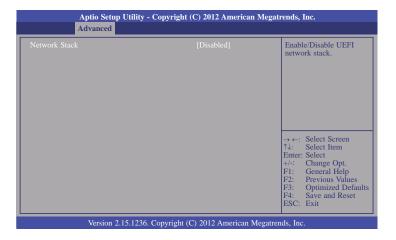
PCH-FW Configuration

This section displays the parameters of Management Engine Technology.

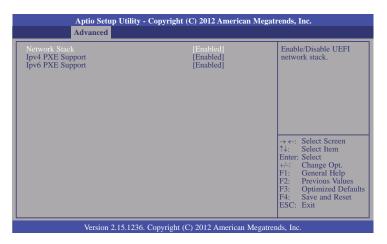


Network Stack

This section is used to enable or disable UEFI network stack.



When Network Stack is enabled, it will display the following information:



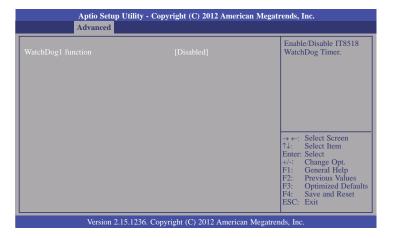
Ipv4 PXE Support

When enabled, Ipv4 PXE boot supports. When disabled, Ipv4 PXE boot option will not be created.

Ipv6 PXE Support

When enabled, Ipv6 PXE boot supports. When disabled, Ipv6 PXE boot option will not be created.

WatchDog Configuration

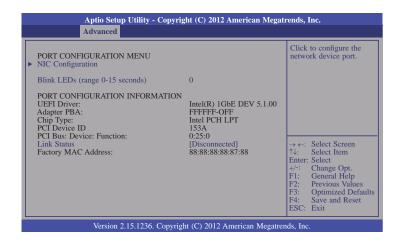


WatchDog1 function

This field is used to enable or disable the Watchdog timer function.

Intel(R) Ethernet Network Connection i217-LM - 88:88:88:...

This section is used to configure the parameters of Gigabit Ethernet device.



NIC Configuration

This field is used to configure the network device.

Blink LEDs

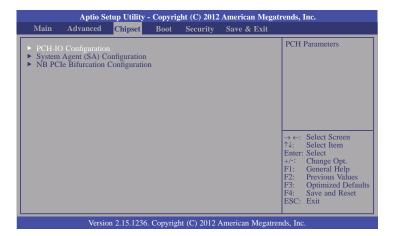
Blink LEDs for the specified duration (up to 15 seconds).

Link Status

This field indicates the link status of the network device.

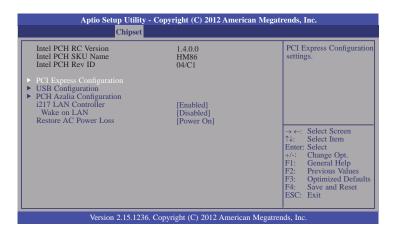
Chipset

This section configures the relevant functions of chipset.



PCH-IO Configuration

This section configures PCH parameters.



i217 LAN Controller

Enable or disable onboard NIC.

Wake on LAN

Set this field to enable to wake up the system via the onboard LAN or via a LAN card that supports the remote wake up function.

Restore AC Power Loss

Select AC power state when the power is re-applied after power failure.

Power-off

When power returns after an AC power failure, the system's power is off. You must press the Power button to power-on the system.

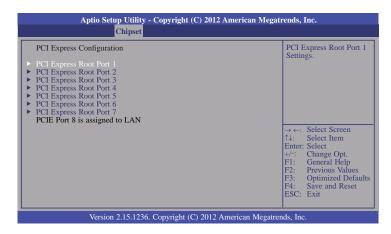
Power-or

When power returns after an AC power failure, the system will automatically power-on.

Last State

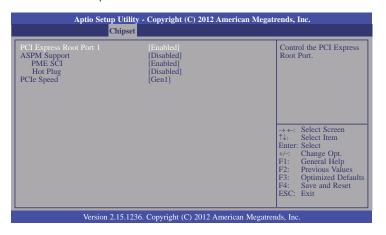
When power returns after an AC power failure, the system will return to the state where you left off before power failure occurs. If the system's power is off when AC power failure occurs, it will remain off when power returns. If the system's power is on when AC power failure occurs, the system will power-on when power returns.

PCI Express Configuration



PCI Express Root Port 1 to PCI Express Root Port 7

Control the PCI Express Root Port.



ASPM Support

Set the ASPM level. The options are listed as below:

Force LOs Forces all links to LOs State.

Auto The BIOS automatically select an ASPM level.

Disabled Disables ASPM.

PME SCI

Enable or disable PCI Express PME SCI.

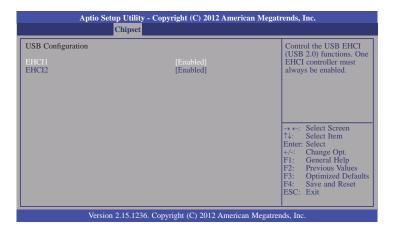
Hot Plug

Enable or disable PCI Express port as Hot Plug.

PCIe Speed

Select the speed of PCI Express port. The option is Gen1 or Gen 2.

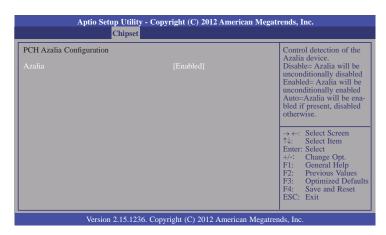
USB Configuration



EHCI1 and EHCI2

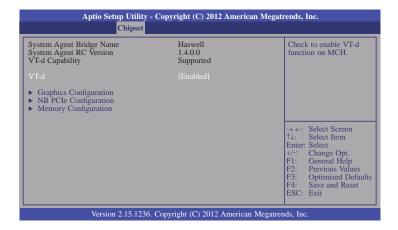
These fields are used to control the functions of USB EHCI (USB 2.0). One EHCI controller must always be enabled.

PCH Azalia Configuration



System Agent (SA) Configuration

This section configures the parameters of System Agent (SA).

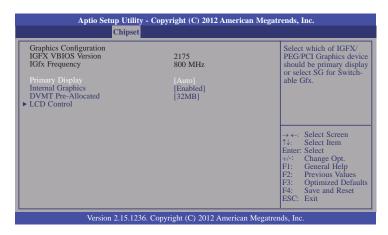


VT-d

Check to enable VT-d function on MCH.

Graphics Configuration

This section is used to configure the graphics settings.



Primary Display

Auto When the system boots, it will auto detects the display device.

IGFX When the system boots, it will first initialize the onboard VGA.

PEG When the system boots, it will first initialize the PCI Express x16 graphics

Internal Graphics

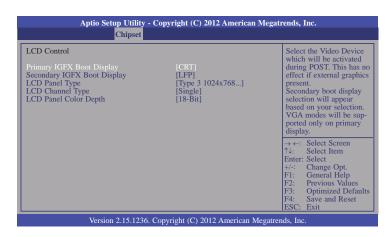
Keep IGD enabled based on setup options.

DVMT Pre-Allocated

Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device. Please refer to the screen shown below.



LCD Control



Primary IGFX Boot Display

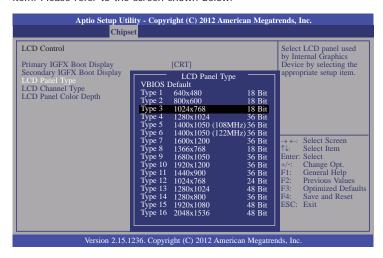
Select the Video Device which will be activated during POST. This has no effect if the external graphics presents. The selection of secondary boot display will appear based on your selection. VGA modes will be supported only on primary display.

Secondary IGFX Boot Display

Select secondary display device.

LCD Panel Type

Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item. Please refer to the screen shown below.



LCD Channel Type

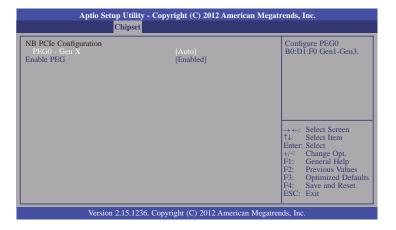
Select the LCD Channel Type. The option is dual or single.

LCD Panel Color Depth

Select the color mode of the LCD display. The option is 24-bit or 18-bit.

NB PCIe Configuration

This section is used to configure the settings of NB PCI Express.



PEGO-Gen X

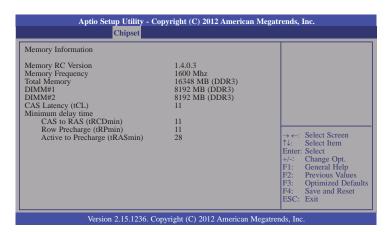
Configure PEG0 Gen1-Gen3.

Enable PEG

Enable or disable the PEG.

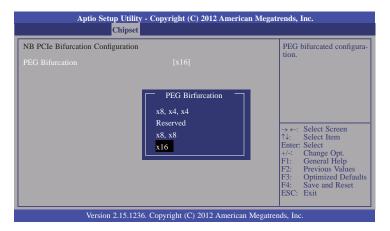
Memory Configuration

This section only display the parameters of memory configuration.

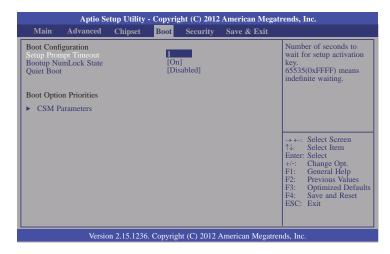


NB PCIe Bifurcation Configuration

This section configures CPU PEG Bifurcation.



Boot



Setup Prompt Timeout

Selects the number of seconds to wait for the setup activation key. 65535(0xFFFF) denotes indefinite waiting.

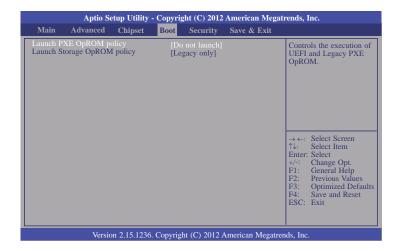
Bootup NumLock State

This allows you to determine the default state of the numeric keypad. By default, the system boots up with NumLock on wherein the function of the numeric keypad is the number keys. When set to Off, the function of the numeric keypad is the arrow keys.

Quiet Boot

Enables or disables the quiet boot function.

CSM Parameters



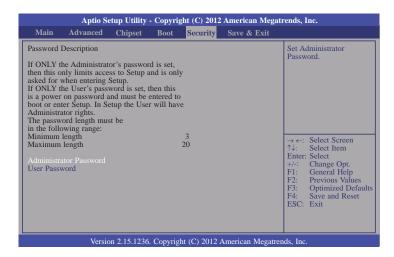
Launch PXE OpROM policy

Control the execution of UEFI and legacy PXE OpROM.

Launch Storage OpROM policy

Control the execution of UEFI and legacy storage OpROM.

Security



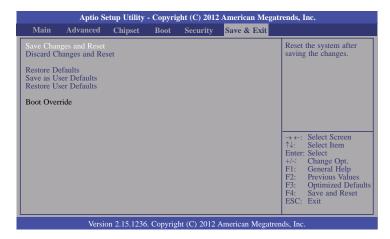
Administrator Password

Sets the administrator password.

User Password

Sets the user password.

Save & Exit



Save Changes and Reset

To save the changes, select this field and then press <Enter>. A dialog box will appear. Select Yes to reset the system after saving all changes made.

Discard Changes and Reset

To discard the changes, select this field and then press <Enter>. A dialog box will appear. Select Yes to reset the system setup without saving any changes.

Restore Defaults

To restore and load the optimized default values, select this field and then press <Enter>. A dialog box will appear. Select Yes to restore the default values of all the setup options.

Save as User Defaults

To save changes done so far as user default, select this field and then press <Enter>. A dialog box will appear. Select Yes to save values as user default.

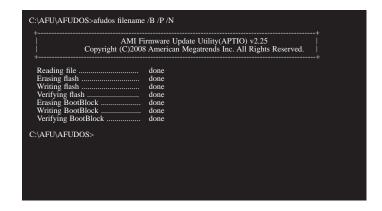
Restore User Defaults

To restore user default to all the setup options, select this field and then press <Enter>. A dialog box will appear. Select Yes to restore user default.

Updating the BIOS

To update the BIOS, you will need the new BIOS file and a flash utility, AFUDOS.EXE. Please contact technical support or your sales representative for the files.

To execute the utility, type: A:> AFUDOS BIOS_File_Name /b /p /n then press <Enter>.



After finishing BIOS update, please turn off the AC power. Wait about 10 seconds and then turn on the AC power again.

Notice: BIOS SPI ROM

- 1. The Intel® Management Engine has already been integrated into this system board. Due to the safety concerns, the BIOS (SPI ROM) chip cannot be removed from this system board and used on another system board of the same model.
- 2. The BIOS (SPI ROM) on this system board must be the original equipment from the factory and cannot be used to replace one which has been utilized on other system boards.
- 3. If you do not follow the methods above, the Intel® Management Engine will not be updated and will cease to be effective.



Note:

- a. You can take advantage of flash tools to update the default configuration of the BIOS (SPI ROM) to the latest version anytime.
- b. When the BIOS IC needs to be replaced, you have to populate it properly onto the system board after the EEPROM programmer has been burned and follow the technical person's instructions to confirm that the MAC address should be burned or not.

Chapter 5 - Supported Software

The CD that came with the system board contains drivers, utilities and software applications required to enhance the performance of the system board.

Insert the CD into a CD-ROM drive. The autorun screen (Mainboard Utility CD) will appear. If after inserting the CD, "Autorun" did not automatically start (which is, the Mainboard Utility CD screen did not appear), please go directly to the root directory of the CD and double-click "Setup".

For Windows 7/8





For Windows XP





Chapter 5 Supported Software www.dfi.com

Microsoft Framework 3.5 (For Windows XP)

To install the driver, click "Microsoft .NET Framework 3.5" on the main menu.



Note:

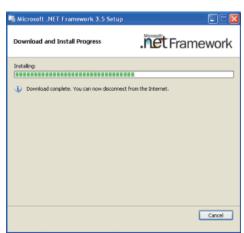
Before installing Microsoft .NET Framework 3.5, make sure you have updated your Windows XP operating system to Service Pack 3.

1. Read the license agreement carefully.

Click "I have read and accept the terms of the License Agreement" then click Install.



2. Setup is now installing the driver.



3. Click Exit.



Intel Chipset Software Installation Utility

The Intel Chipset Device Software is used for updating Windows® INF files so that the Intel chipset can be recognized and configured properly in the system.

To install the utility, click "Intel Chipset Device Software" on the main menu.

1. Setup is ready to install the utility. Click Next.



2. Read the license agreement then click Yes.



Go through the readme document for more installation tips then click Next.



4. After all setup operations are done, click Next.



5. Click "Yes, I want to restart this computer now" then click Finish.

Restarting the system will allow the new software installation to take effect.



Chapter 5 Supported Software www.dfi.com

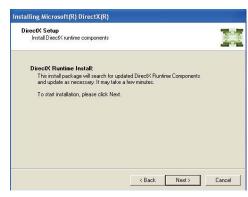
Microsoft DirectX 9.0C (For Windows XP)

To install the utility, click "Microsoft DirectX 9.0C Driver" on the main menu.

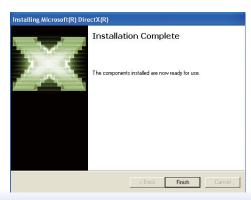
 Click "I accept the agreement" then click Next.



2. To start installation, click Next.



Click Finish. Reboot the system for DirectX to take effect.



Intel HD Graphics Drivers (For Windows XP)

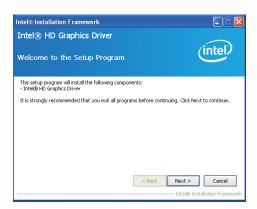


Note:

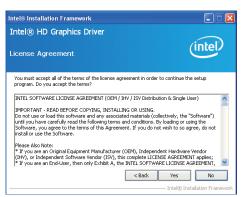
Before installing Intel HD Graphics Drivers, make sure you have installed Microsoft .NET Framework 3.5 SP1.

To install the driver, click "Intel HD Graphics Drivers" on the main menu.

Setup is ready to install the graphics driver. Click Next.

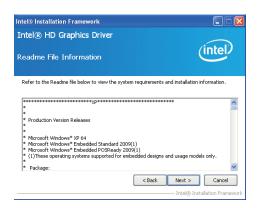


2. Read the license agreement then click Yes.

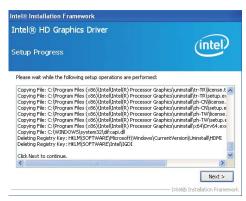


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Go through the readme document for more installation tips then click Next.

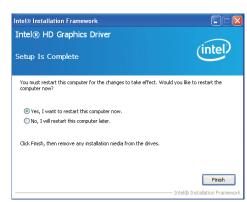


 Setup is currently installing the driver. After installation has completed, click Next.



5. Click "Yes, I want to restart this computer now." then click Finish.

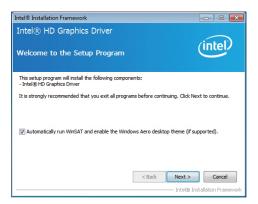
Restarting the system will allow the new software installlation to take effect



Intel HD Graphics Drivers (For Windows 7/8)

To install the driver, click "Intel HD Graphics Drivers" on the main menu.

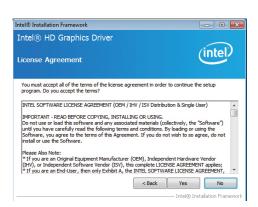
 Setup is now ready to install the graphics driver. Click Next.



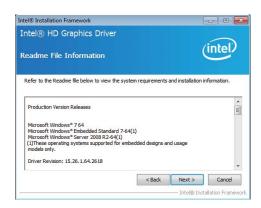
By default, the "Automatically run WinSAT and enable the Windows Aero desktop theme" is enabled. With this enabled, after installing the graphics driver and the system rebooted, the screen will turn blank for 1 to 2 minutes (while WinSAT is running) before the Windows 7/ Windows 8 desktop appears. The "blank screen" period is the time Windows is testing the graphics performance.

We recommend that you skip this process by disabling this function then click Next.

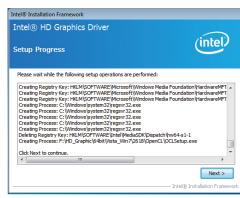
2. Read the license agreement then click Yes.



Go through the readme document for system requirements and installation tips then click Next.



4. Setup is now installing the driver. Click Next to continue.



5. Click "Yes, I want to restart this computer now" then click Finish.

Restarting the system will allow the new software installation to take effect.



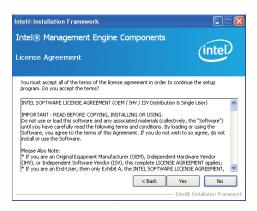
Intel Management Engine Drivers

To install the driver, click "Intel Management Engine Drivers" on the main menu.

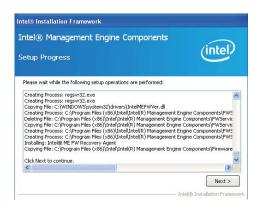
 Setup is ready to install the driver. Click Next.



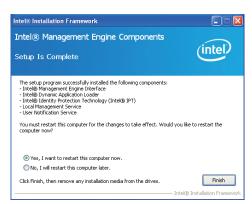
2. Read the license agreement then click Yes.



3. Setup is currently installing the driver. After installation has completed, click Next.



4. After completing installation, click Finish.



Audio Drivers (For COM330-B Carrier Board)

To install the driver, click "Audio Drivers (for COM330-B Carrier Board" on the main menu.

- 1. Setup is now ready to install the audio driver. Click Next.
- 2. Follow the remainder of the steps on the screen; clicking "Next" each time you finish a step.



3. Click "Yes, I want to restart my computer now" then click Finish.

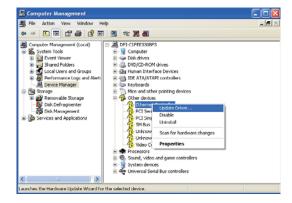
Restarting the system will allow the new software installation to take effect.



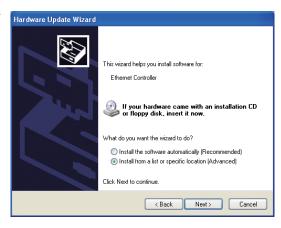
Intel LAN Drivers (For Windows XP)

The LAN drivers for Windows XP supporting on the HM920-QM87/HM86 system board has to be installed manually. When you want to install the LAN driver for Windows XP, please follow the steps below to accomplish the installation.

 Launch the Hardware Update Wizard for the selected device. Select "Update Driver."



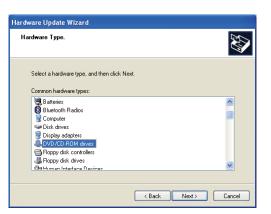
Choose "Install from a list or specific location (Advanced)" and click "Next" to continue the installation.



 Choose the option "Don't search. I will choose the driver to install" in order to select the device driver from a list, and click "Next."



 Select a hardware type: DVD/CD-ROM drives. Then, click "Next."



5. Select your hardware disk and then click "Have Disk..."



Insert the installation disk and make sure the selected drive is correct.

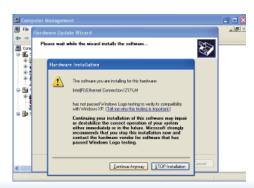


(For 32-bit, the file name is "e1d5132.inf".)

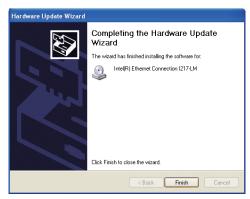
7. Select the device driver you want to install for this hardware and then click "Next."



8. Check the software you are installing, Then, click "Continue Anyway" to start the installation.



9. Click "Finish" to close the wizard. Hardware Update Wizard



 After completing the installation, the Network adapters "Intel(R) Ethernet Connection 1217LM" will appear on the computer management list.



Intel LAN Drivers (For Windows 7/8)

To install the driver, click "Intel LAN Drivers" on the main menu.

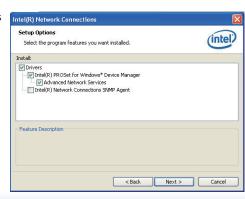
1. Setup is ready to install the driver. Click Next.



Click "I accept the terms in the license agreement" then click "Next".



Select the program featuers you want installed then click Next.



4. Click Install to begin the installation.



5. After completing installation, click Finish.



DFI Utility

DFI Utility provides information about the board, HW Health, Watchdog, DIO, and Backlight. To access the utility, click "DFI Utility" on the main menu.



Note:

If you are using Windows 7, you need to access the operating system as an administrator to be able to install the utility.

1. Setup is ready to install the DFI Utility drifer. Click Next.



Click "I accept the terms in the license agreement" and then click Next.



Enter "User Name" and "Organization" information and then click
Next



4. Click Install to begin the installation.

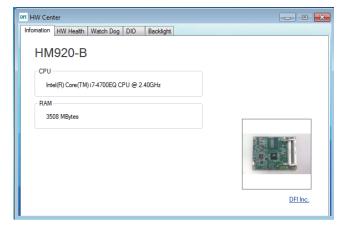


5. After completing installation, click Finish.

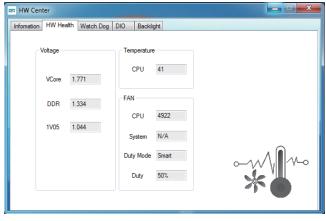


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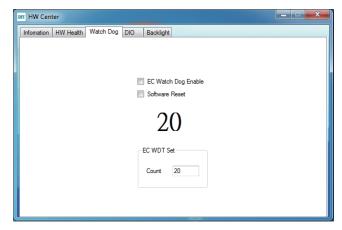
The DFI Utility icon will appear on the desktop. Double-click the icon to open the utility.



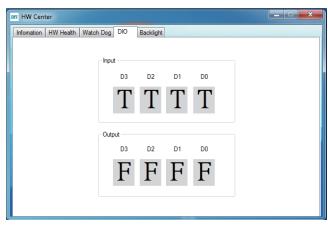
Information



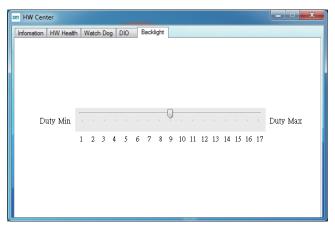
HW Health



WatchDog



DIO



Backlight

Intel Rapid Storage Technology

The Intel Rapid Storage Technology is a utility that allows you to monitor the current status of the SATA drives. It enables enhanced performance and power management for the storage subsystem.

To install the driver, click "Intel Rapid Storage Technology" on the main menu.



Note:

Windows Vista is not supported.

1. Setup is now ready to install the utility. Click Next.



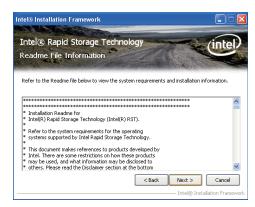
2. Read the warning then click Yes.



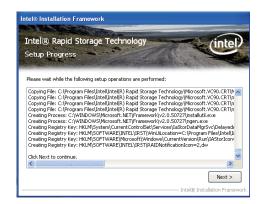
3. Read the license agreement then click Yes.



4. Go through the readme document for system requirements and installation tips then click Next.

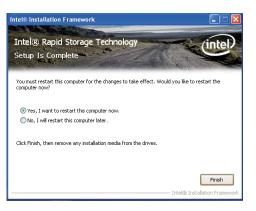


5. Setup is now installing the utility. Click Next to continue.



6. Click "Yes, I want to restart my computer now" then click Finish.

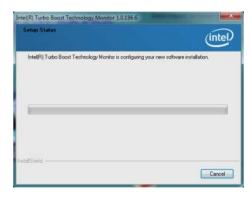
Restarting the system will allow the new software installation to take effect.



Intel Turbo Boost Monitor (For Windows 7/8)

To install the driver, click "Intel Turbo Boost Monitor" on the main menu.

1. The setup program is configuring the new software installation.



2. Click Next.



 Read the license agreement and then click "I accept the terms in the license agreement". Click Next.



4. Click Install.



5. The setup program is currently installing the software.



Click Finish.



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Intel Rapid Start Technology (For Windows 7/8)

The Intel Rapid Start Technology is a utility that allows your system to wake up and run faster.

To install the driver, click "Intel Rapid Start Technology" on the main menu.

1. Setup is now ready to install the utility. Click Next.



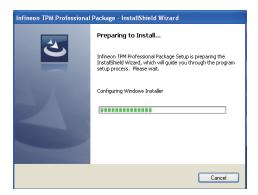
Click ON and select the Advanced Settings to enable the Intel Rapid Start Technology. Then, click Save.



Infineon TPM Driver and Tool (optional)

To install the driver, click "Infineon TPM driver and tool (option)" on the main menu.

1. The setup program is preparing to install the driver.



2. The setup program is now ready to install the utility. Click Next.



 Click "I accept the terms in the license agreement" and then click "Next".



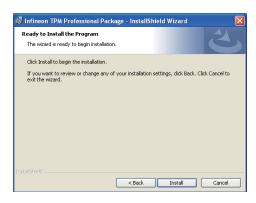
4. Enter the necessary information and then click Next.



5. Select a setup type and then click Next.



6. Click Install.



 TPM requires installing the Microsoft Visual C++ package prior to installing the utility. Click Install.



8. The setup program is currently installing the Microsoft Visual C++ package.



9. Click Finish.



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10. Click "Yes" to restart your system.

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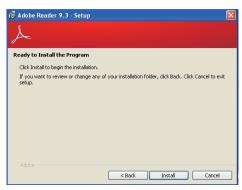
Adobe Acrobat Reader 9.3

To install the reader, click "Adobe Acrobat Reader 9.3" on the main menu.

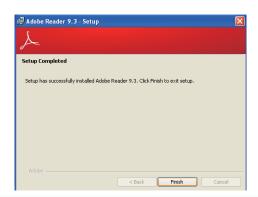
 Click Next to install or click Change Destination Folder to select another folder.



2. Click Install to begin installation.



3. Click Finish to exit installation.



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Chapter 6 - GPIO Programming Guide

Function Description

Get_EC_Data (unsigned char ucData): Read a Byte data from EC. Write_EC_Data (unsigned char ucData, unsigned char Data): Write a Byte data to EC.

Sample Code

GPIO Input Process

```
EC_DIO_Read_Input()
{
    BYTE Data;

    //Pin0-3 Input Mode
    Data = Get_EC_Data(0xBA);
    Data |= 0x80;
    Write_EC_Data(0xBA, Data);
    while(((Get_EC_Data(0xBA) >> 7)&0x01))
    {
        Data = Get_EC_Data(0xBA);
    }

    Return Data ;
}
```

GPIO Output Process

```
EC_DIO_Write_Output(unsigned char udata)

{

    //Pin4-7 Output Mode
    udata <<= 4;
    udata |= 0x01;
    Write_EC_Data(0xBB, udata);

    return 0;

EC_DIO_Read_Output()

{

    BYTE Data;

    //Pin4-7 Output Mode
    Write_EC_Data(0xBB, 0x02);
    Delay;
    Data = Get_EC_Data(0xBB);
    Data >>= 4;
    Return Data;
}
```

Chapter 7 - RAID (HM920-QM87)

The system board allows configuring RAID on Serial ATA drives. It supports RAID 0, RAID 1, RAID 5 and RAID 10.

RAID Levels

RAID 0 (Striped Disk Array without Fault Tolerance)

RAID 0 uses two new identical hard disk drives to read and write data in parallel, interleaved stacks. Data is divided into stripes and each stripe is written alternately between two disk drives. This improves the I/O performance of the drives at different channel; however it is not fault tolerant. A failed disk will result in data loss in the disk array.

RAID 1 (Mirroring Disk Array with Fault Tolerance)

RAID 1 copies and maintains an identical image of the data from one drive to the other drive. If a drive fails to function, the disk array management software directs all applications to the other drive since it contains a complete copy of the drive's data. This enhances data protection and increases fault tolerance to the entire system. Use two new drives or an existing drive and a new drive but the size of the new drive must be the same or larger than the existing drive.

RAID 5

RAID 5 stripes data and parity information across hard drives. It is fault tolerant and provides better hard drive performance and more storage capacity.

RAID 10 (Mirroring and Striping)

RAID 10 is a combination of data striping and data mirroring providing the benefits of both RAID 0 and RAID 1. Use four new drives or an existing drive and three new drives for this configuration.

Settings

To enable the RAID function, the following settings are required.

- 1. Connect the Serial ATA drives.
- Configure Serial ATA in the AMI BIOS.
- 3. Configure RAID in the RAID BIOS.
- 4. Install the RAID driver during OS installation.
- 5. Install the Intel Rapid Storage Drivers.

Step 1: Connect the Serial ATA Drives

Refer to chapter 2 for details on connecting the Serial ATA drives.



Important:

- Make sure you have installed the Serial ATA drives and connected the data cables otherwise you won't be able to enter the RAID BIOS utility.
- Treat the cables with extreme caution especially while creating RAID. A damaged cable will ruin the entire installation process and operating system. The system will not boot and you will lost all data in the hard drives. Please give special attention to this warning because there is no way of recovering back the data.

Step 2: Configure Serial ATA in the AMI BIOS

- 1. Power-on the system then press to enter the main menu of the AMI BIOS.
- 2. Configure Serial ATA in the appropriate fields.
- Save the changes in the Save & Exit menu.
- Reboot the system.

Step 3: Configure RAID in the RAID BIOS

When the system powers-up and all drives have been detected, the Intel RAID BIOS status message screen will appear. Press the <Ctrl> and <I> keys simultaneously to enter the utility. The utility allows you to build a RAID system on Serial ATA drives.

Step 4: Install the RAID Driver During OS Installation

The RAID driver must be installed during the Windows® XP or Windows® 2000 installation using the F6 installation method. This is required in order to install the operating system onto a hard drive or RAID volume when in RAID mode or onto a hard drive when in AHCI mode.

- 1. Start Windows Setup by booting from the installation CD
- 2. Press <F6> when prompted in the status line with the 'Press F6 if you need to install a third party SCSI or RAID driver' message.
- 3. Press <S> to "Specify Additional Device".
- At this point you will be prompted to insert a floppy disk containing the RAID driver. Insert the RAID driver diskette.
- 5. Locate for the drive where you inserted the diskette then select RAID or AHCI controller that corresponds to your BIOS setup. Press <Enter> to confirm.

You have successfully installed the driver. However you must continue installing the OS. Leave the floppy disk in the floppy drive until the system reboots itself because Windows setup will need to copy the files again from the floppy disk to the Windows installation folders. After Windows setup has copied these files again, remove the floppy diskette so that Windows setup can reboot as needed.

Step 5: Install the Intel Rapid Storage Technology Utility

The Intel Rapid Storage Technology Utility can be installed from within Windows. It allows RAID volume management (create, delete, migrate) from within the operating system. It will also display useful SATA device and RAID volume information. The user interface, tray icon service and monitor service allow you to monitor the current status of the RAID volume and/or SATA drives. It enables enhanced performance and power management for the storage subsystem.

- 1. Insert the provided CD into an optical drive.
- 2. Click "Intel Rapid Storage Technology Utility" on the main menu.
- 3. Setup is ready to install the utility. Click Next.



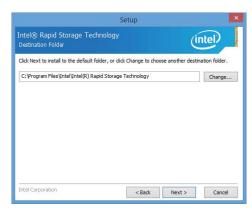
 Read the license agreement and click "I accept the terms in the License Agreement." Then, click Next.



 Go through the readme document to view system requirements and installation information then click Next.



 Click Next to install to the default folder or click change to choose another destination folder.



7. Confirm the installation and click Next.



8. Click "Yes, I want to restart this computer now" to complete the installation and then click Finish.



Chapter 8 - Intel AMT Settings (HM920-QM87)

Overview

Intel Active Management Technology (Intel® AMT) combines hardware and software solution to provide maximum system defense and protection to networked systems.

The hardware and software information are stored in non-volatile memory. With its built-in manageability and latest security applications, Intel® AMT provides the following functions.

Discover

Allows remote access and management of networked systems even while PCs are powered off; significantly reducing desk-side visits.

Repair

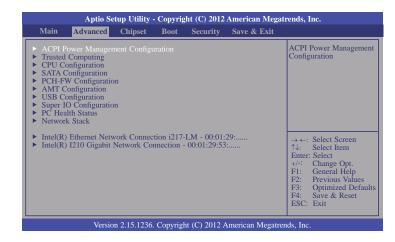
Remotely repair systems after OS failures. Alerting and event logging help detect problems quickly to reduce downtime.

Protect

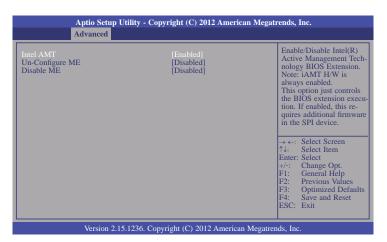
Intel AMT's System Defense capability remotely updates all systems with the latest security software. It protects the network from threats at the source by proactively blocking incoming threats, reactively containing infected clients before they impact the network, and proactively alerting when critical software agents are removed.

Enable Intel® AMT in the AMI BIOS

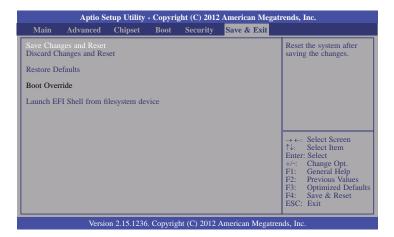
- 1. Power-on the system then press to enter the main menu of the AMI BIOS.
- 2. In the Advanced menu, select AMT Configuration.



3. In the **Advanced** menu, select **Enable** in the **AMT** field.



4. In the Save & Exit menu, select Save Changes and Reset then select OK.

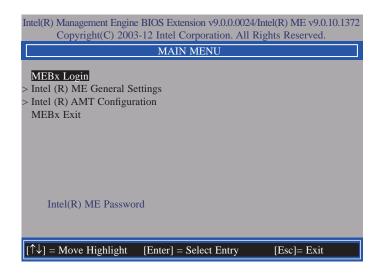


Enable Intel® AMT in the Intel® Management Engine BIOS Extension (MEBX) Screen

 When the system reboots, the following message will be displayed. Press <Ctrl-P> as soon as the message is displayed; as this message will be displayed for only a few seconds.



2. You will be prompted for a password. The default password is "admin". Enter the default password in the space provided under Intel(R) ME Password then press Enter.



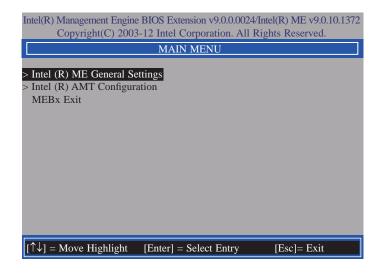
- 3. Enter a new password in the space provided under Intel(R) ME New Password then press Enter. The password must include:
 - 8-32 characters
 - Strong 7-bit ASCII characters excluding:, and " characters
 - At least one digit character (0, 1, ...9)
 - At least one 7-bit ASCII non alpha-numeric character, above 0x20, (e.g. !, \$, ;)
 - Both lower case and upper case characters



4. You will be asked to verify the password. Enter the same new password in the space provided under Verify Password then press Enter.



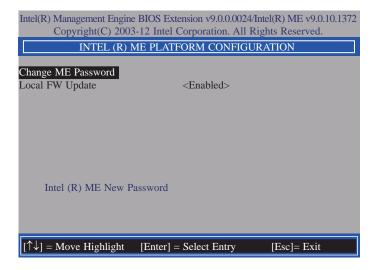
5. Select Intel(R) ME General Settings then press Enter.



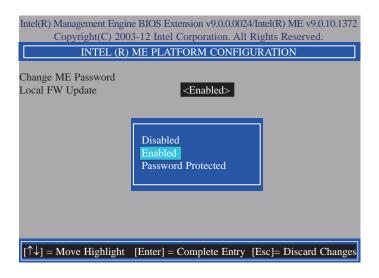
6. Select Change Intel(R) ME Password then press Enter.

You will be prompted for a password. The default password is "admin". Enter the default password in the space provided under Intel(R) ME New Password then press Enter.

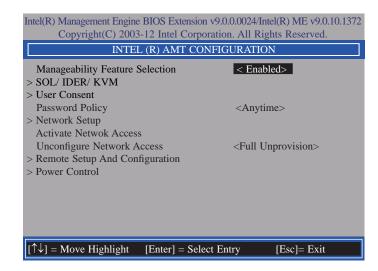
- 8-32 characters
- Strong 7-bit ASCII characters excluding:, and " characters
- At least one digit character (0, 1, ...9)
- At least one 7-bit ASCII non alpha-numeric character, above 0x20, (e.g. !, \$, ;)
- Both lower case and upper case characters



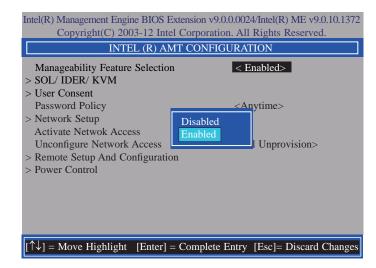
7. Select **Local FW Update** then press Enter. Select **Enabled** then press Enter.



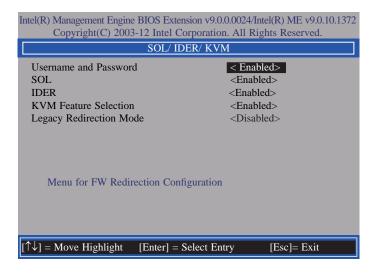
Select Previous Menu until you return to the Main Menu. Select Intel(R) AMT Configuration then press Enter.



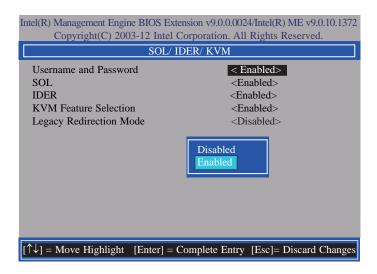
 In the Intel(R) AMT Configuration menu, select Manageability Feature Selection then press Enter. Select Disabled then press Enter.



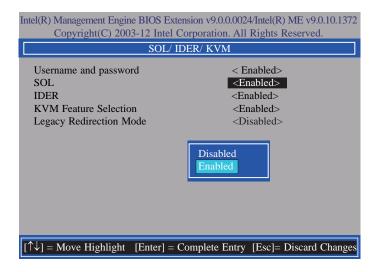
10. In the Intel(R) AMT Configuration menu, select SOL/IDER/KVM then press Enter.



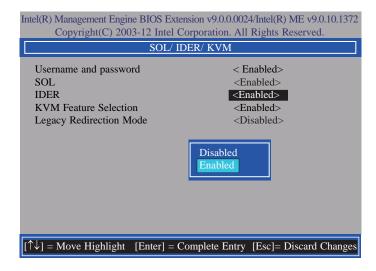
In the SOL/IDER/KVM menu, select Username and Password then press Enter.
 Select Disabled then press Enter.



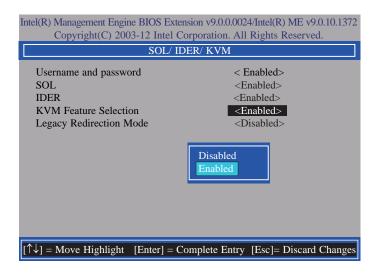
12. In the **SOL/IDER/KVM** menu, select **SOL** then press Enter. Select **Disabled** then press Enter.



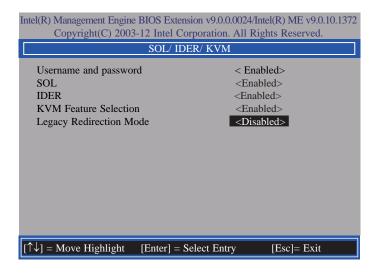
13. In the **SOL/IDER/KVM** menu, select **IDER** then press Enter. Select **Disabled** then press Enter.



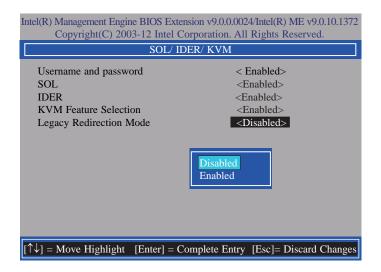
 In the SOL/IDER/KVM menu, select KVM Feature Selection then press Enter. Select Disabled then press Enter.



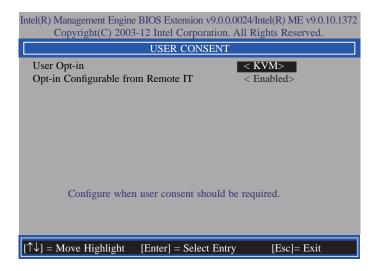
15. In the SOL/IDER/KVM menu, select Legacy Redirection Mode then press Enter.



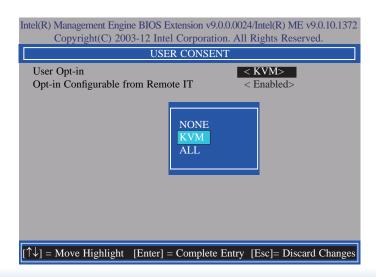
16. Select **Enabled** then press Enter.



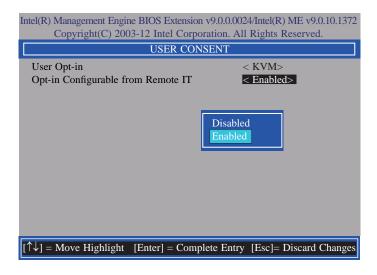
 Select Previous Menu until you return to the Intel(R) AMT Configuration menu. Select User Consent then press Enter.



18. In the **User Consent** menu, select **User Opt-in** then press Enter. Select **None** then press Enter.

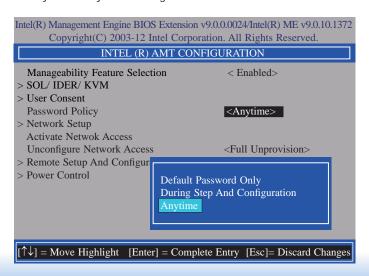


 In the User Consent menu, select Opt-in Configurable from Remote IT then press Enter. Select Disable Remote Control of KVM Opt-in Policy then press Enter.

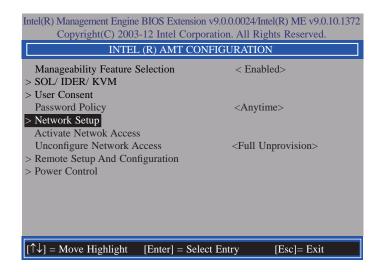


 Select Previous Menu until you return to the Intel(R) AMT Configuration menu. Select Password Policy then press Enter.

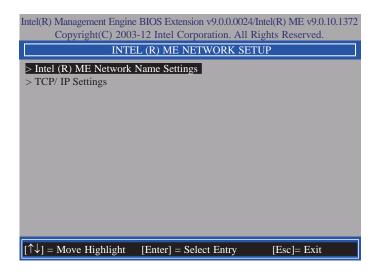
You may choose to use a password only during setup and configuration or to use a password anytime the system is being accessed.



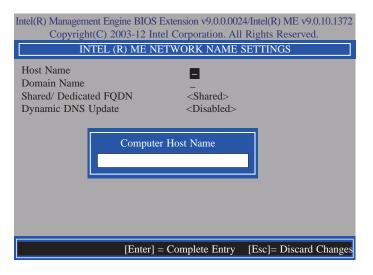
21. In the Intel(R) AMT Configuration menu, select Network Setup then press Enter.



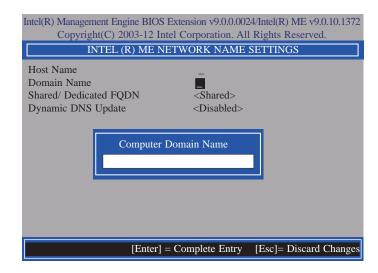
In the Intel(R) ME Network Setup menu, select Intel(R) ME Network Name Settings then press Enter.



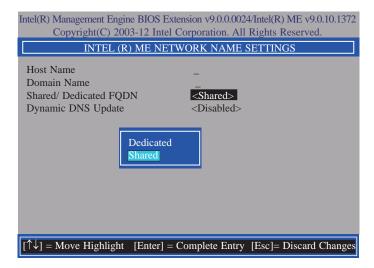
23. In the Intel(R) ME Network Name Settings menu, select Host Name then press Enter. Enter the computer's host name then press Enter.



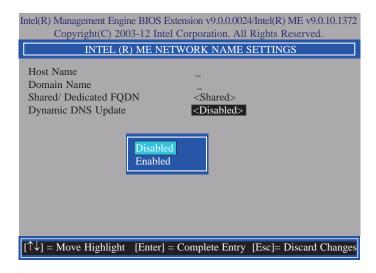
24. Select **Domain Name** then press Enter. Enter the computer's domain name then press Enter.



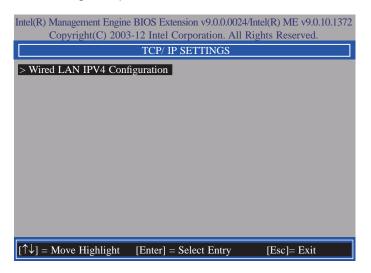
 Select Shared/Dedicated FQDN then press Enter. Select Shared or Dedicated then press Enter.



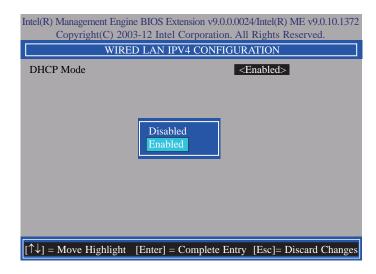
 Select Dynamic DNS Update then press Enter. Select Enabled or Disabled then press Enter.



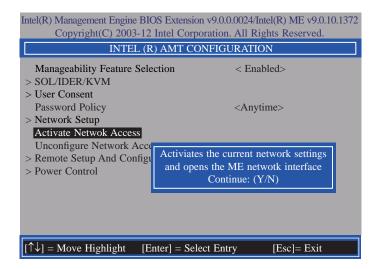
 Select Previous Menu until you return to the Intel(R) ME Network Setup menu. Select TCP/IP Settings then press Enter.



 In the TCP/IP Settings menu, select Wired LAN IPV4 Configuration then press Enter.



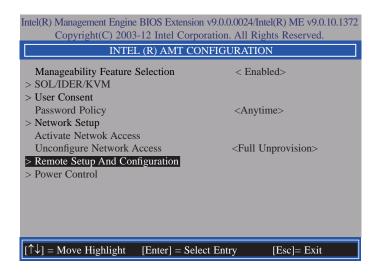
 Select Previous Menu until you return to the Intel(R) AMT Configuration menu. Select Activate Network Access then press Enter. Type Y then press Enter.



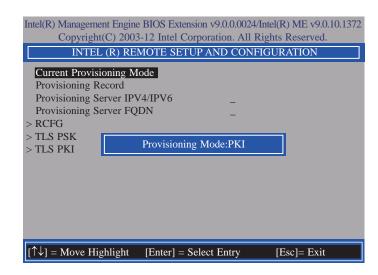
In the Intel(R) AMT Configuration menu, select Unconfigure Network Access then
press Enter.



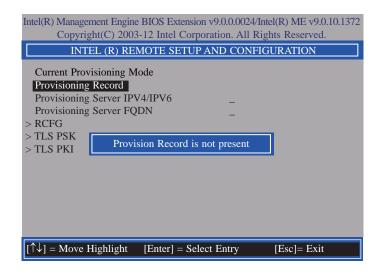
31. In the Intel(R) AMT Configuration menu, select Remote Setup And Configuration then press Enter.



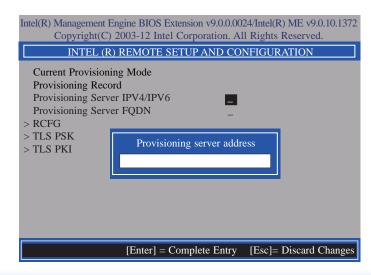
 In the Intel(R) Remote Setup And Configuration menu, select Current Provisioning Mode then press Enter.



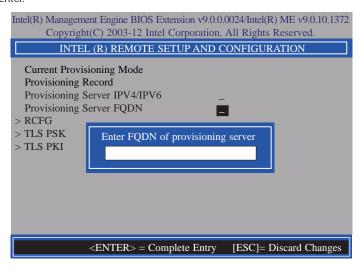
 In the Intel(R) Remote Setup And Configuration menu, select Provisioning Record then press Enter.



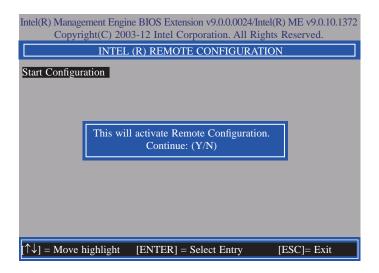
 Select Previous Menu until you return to the Intel(R) Remote Setup And Configuration menu. Select Provisioning Server IPV4/IPV6 then press Enter. Type server address then press Enter.



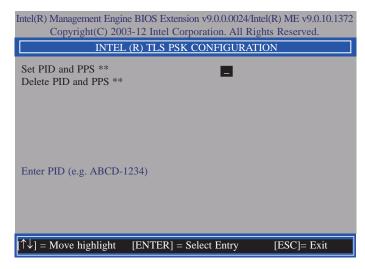
35. In the Intel(R) Remote Automated Setup And Configuration menu, select Provisioning Server FQDN then press Enter. Type FQDN of provisioning server then press Enter.



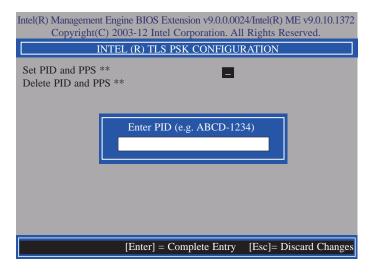
 In the Intel(R) Remote Automated Setup And Configuration menu, select RCFG then press Enter. Select Start Configuration, and type Y then press Enter.



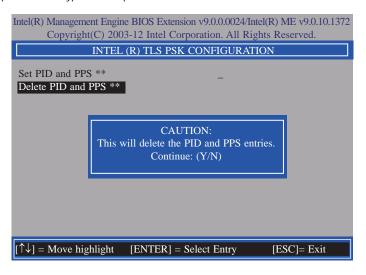
37. In the Intel(R) Remote Automated Setup And Configuration menu, select TLS PSK then press Enter.



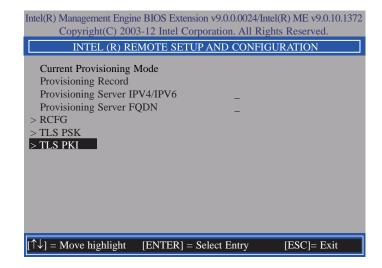
38. In the Intel(R) TLS PSK Configuration menu, select Set PID and PPS ** then press Enter. Type PID code then press Enter.



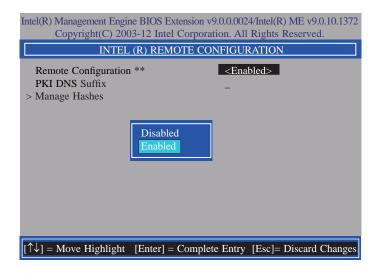
In the Intel(R) TLS PSK Configuration menu, select Delete PID and PPS ** then
press Enter. Type Y then press Enter.



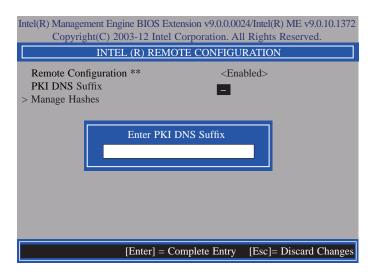
 Select Previous Menu until you return to the Intel(R) Remote Setup And Configuration menu. Select TLS PKI then press Enter.



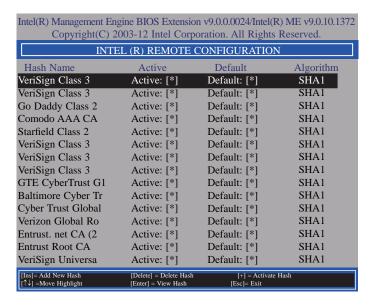
41. In the Intel(R) Remote Configuration menu, select Remote Configuration ** then press Enter. Select Disabled then press Enter.



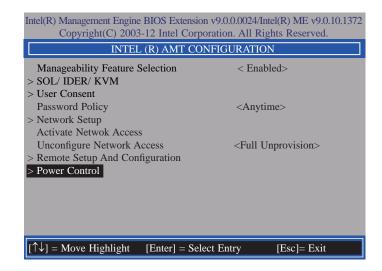
42. In the Intel(R) Remote Configuration menu, select PKI DNS Suffix then press Enter. Type PKI DNS Suffix then press Enter.



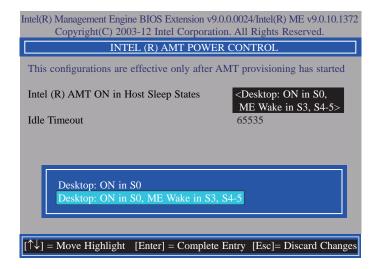
43. In the Intel(R) Remote Configuration menu, select Manage Hashes then press Enter.



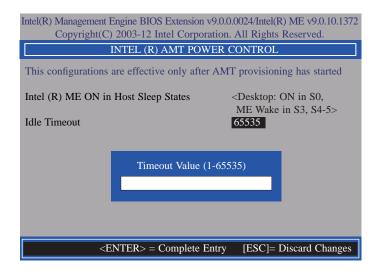
44. In the Intel(R) AMT Configuration menu, select Power Control then press Enter.



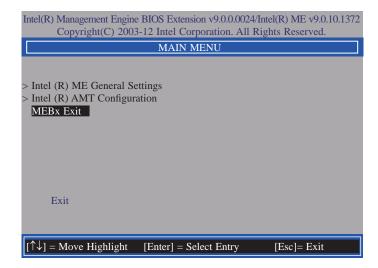
45. In the Intel(R) AMT Power Control menu, select Intel(R) AMT ON in Host Sleep States then press Enter. Select an option then press Enter.



46. In the Intel(R) AMT Power Control menu, select Idle Timeout then press Enter. Enter the timeout value (1-65535).



47. Select Previous Menu until you return to the **Main Menu**. Select **Exit** then press Enter. Type **Y** then press Enter.



Appendix A - Watchdog Sample Code

```
#include <stdio.h>
//-----
#define EC_EnablePort 0x66
#define EC DataPort 0x62
//-----
void WriteEC(char.int):
void SetWDTime(int,int);
int GetWDTime(void);
main()
 unsigned int countdown;
 unsigned int input,count_h,count_l;
 printf("Input WD Time: ");
 scanf("%d",&input);
 printf("\n");
 count_h=input>>8;
 count I=input&0x00FF;
 SetWDTime(count_h,count_l);
 while(1)
        countdown = GetWDTime();
        delay(100);
        printf("\rTime Remaining: %d ",countdown);
void SetWDTime(int count H.int count L)
 //Set Count
 WriteEC(0xB5,count_H); //High Byte
 WriteEC(0xB6,count_L); //Low Byte
 //Enable Watch Dog Timer
 WriteEC(0xB4,0x01);
```

```
int GetWDTime(void)
  int sum, data h, data 1;
  //Select EC Read Type
  outportb(EC_EnablePort,0x80);
  delay(5);
  //Get Remaining Count High Byte
  outportb(EC_DataPort,0xF4);
  delay(5);
  data_h=inportb(EC_DataPort);
  delay(5);
  //Select EC Read Type
  outportb(EC_EnablePort,0x80);
  delay(5);
  //Get Remaining Count Low Byte
  outportb(EC_DataPort,0xF5);
  delay(5);
  data_l=inportb(EC_DataPort);
  delay(5);
  data_h<<=8;
  data h&=0xFF00;
  sum=data_h|data_l;
  return sum;
void WriteEC(char EC Addr, int data)
  //Select EC Write Type
  outportb(EC_EnablePort,0x81);
  delay(5):
  outportb(EC_DataPort,EC_Addr);
  delay(5);
  outportb(EC_DataPort,data);
  delay(5);
```

Appendix B - System Error Message

When the BIOS encounters an error that requires the user to correct something, either a beep code will sound or a message will be displayed in a box in the middle of the screen and the message, PRESS F1 TO CONTINUE, CTRL-ALT-ESC or DEL TO ENTER SETUP, will be shown in the information box at the bottom. Enter Setup to correct the error.

Error Messages

One or more of the following messages may be displayed if the BIOS detects an error during the POST. This list indicates the error messages for all Awards BIOSes:

CMOS BATTERY HAS FAILED

The CMOS battery is no longer functional. It should be replaced.



Important

Danger of explosion if battery incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the battery manufacturer's instructions.

CMOS CHECKSUM ERROR

Checksum of CMOS is incorrect. This can indicate that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace if necessary.

DISPLAY SWITCH IS SET INCORRECTLY

The display switch on the motherboard can be set to either monochrome or color. This indicates the switch is set to a different setting than indicated in Setup. Determine which setting is correct, either turn off the system and change the jumper or enter Setup and change the VIDEO selection.

Appendix C - Troubleshooting

Troubleshooting Checklist

This chapter of the manual is designed to help you with problems that you may encounter with your personal computer. To efficiently troubleshoot your system, treat each problem individually. This is to ensure an accurate diagnosis of the problem in case a problem has multiple causes.

Some of the most common things to check when you encounter problems while using your system are listed below.

- 1. The power switch of each peripheral device is turned on.
- 2. All cables and power cords are tightly connected.
- 3. The electrical outlet to which your peripheral devices are connected is working. Test the outlet by plugging in a lamp or other electrical device.
- 4. The monitor is turned on.
- 5. The display's brightness and contrast controls are adjusted properly.
- 6. All add-in boards in the expansion slots are seated securely.
- 7. Any add-in board you have installed is designed for your system and is set up correctly.

Monitor/Display

If the display screen remains dark after the system is turned on:

- 1. Make sure that the monitor's power switch is on.
- 2. Check that one end of the monitor's power cord is properly attached to the monitor and the other end is plugged into a working AC outlet. If necessary, try another outlet.
- 3. Check that the video input cable is properly attached to the monitor and the system's display adapter.
- 4. Adjust the brightness of the display by turning the monitor's brightness control knob.

The picture seems to be constantly moving.

- 1. The monitor has lost its vertical sync. Adjust the monitor's vertical sync.
- 2. Move away any objects, such as another monitor or fan, that may be creating a magnetic field around the display.
- 3. Make sure your video card's output frequencies are supported by this monitor.

The screen seems to be constantly wavering.

1. If the monitor is close to another monitor, the adjacent monitor may need to be turned off. Fluorescent lights adjacent to the monitor may also cause screen wavering.

Power Supply

When the computer is turned on, nothing happens.

- 1. Check that one end of the AC power cord is plugged into a live outlet and the other end properly plugged into the back of the system.
- 2. Make sure that the voltage selection switch on the back panel is set for the correct type of voltage you are using.
- 3. The power cord may have a "short" or "open". Inspect the cord and install a new one if necessary.

Appendix C Troubleshooting www.dfi.com

Hard Drive

Hard disk failure.

- 1. Make sure the correct drive type for the hard disk drive has been entered in the BIOS.
- 2. If the system is configured with two hard drives, make sure the bootable (first) hard drive is configured as Master and the second hard drive is configured as Slave. The master hard drive must have an active/bootable partition.

Excessively long formatting period.

If your hard drive takes an excessively long period of time to format, it is likely a cable connection problem. However, if your hard drive has a large capacity, it will take a longer time to format.

Serial Port

The serial device (modem, printer) doesn't output anything or is outputting garbled

characters.

- 1. Make sure that the serial device's power is turned on and that the device is on-line.
- 2. Verify that the device is plugged into the correct serial port on the rear of the computer.
- 3. Verify that the attached serial device works by attaching it to a serial port that is working and configured correctly. If the serial device does not work, either the cable or the serial device has a problem. If the serial device works, the problem may be due to the onboard I/O or the address setting.
- 4. Make sure the COM settings and I/O address are configured correctly.

Keyboard

Nothing happens when a key on the keyboard was pressed.

- 1. Make sure the keyboard is properly connected.
- 2. Make sure there are no objects resting on the keyboard and that no keys are pressed during the booting process.

System Board

- 1. Make sure the add-in card is seated securely in the expansion slot. If the add-in card is loose, power off the system, re-install the card and power up the system.
- 2. Check the jumper settings to ensure that the jumpers are properly set.
- 3. Verify that all memory modules are seated securely into the memory sockets.
- 4. Make sure the memory modules are in the correct locations.
- 5. If the board fails to function, place the board on a flat surface and seat all socketed components. Gently press each component into the socket.
- 6. If you made changes to the BIOS settings, re-enter setup and load the BIOS defaults.

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