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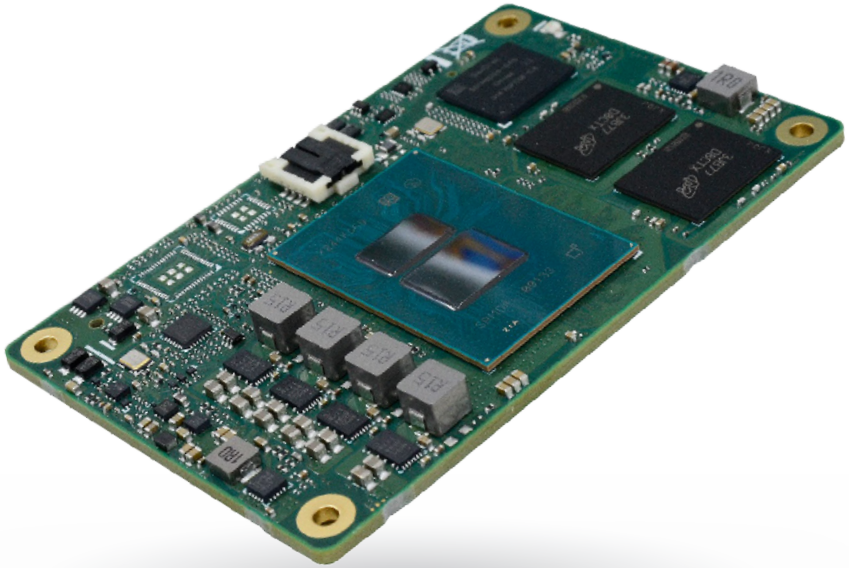

# ASL9A2

COM Express Mini Module
User's Manual

© March 05, 2025 DFI Inc.

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## COM Express Specification Reference

PICMG® COM Express® Module Base Specification.
http://www.picmg.org/

## FCC and DOC Statement on Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio TV technician for help.

## Notice:

- The changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.
- Shielded interface cables must be used in order to comply with the emission limits.

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## About this Manual

This manual can be downloaded from the website.

The manual is subject to change and update without notice, and may be based on editions that do not resemble your actual products. Please visit our website or contact our sales representatives for the latest editions.

## Warranty

- Warranty does not cover damages or failures that occur from misuse of the product, inability to use the product, unauthorized replacement or alteration of components and product specifications.
- The warranty is void if the product has been subjected to physical abuse, improper installation, modification, accidents or unauthorized repair of the product.
- Unless otherwise instructed in this user's manual, the user may not, under any circumstances, attempt to perform service, adjustments or repairs on the product, whether in or out of warranty. It must be returned to the purchase point, factory or authorized service agency for all such work.
- We will not be liable for any indirect, special, incidental or consequential damages to the product that has been modified or altered.

## Static Electricity Precautions

It is quite easy to inadvertently damage your PC, system board, components or devices even before installing them in your system unit. Static electrical discharge can damage computer components without causing any signs of physical damage. You must take extra care in handling them to ensure against electrostatic build-up.

- To prevent electrostatic build-up, leave the system board in its anti-static bag until you are ready to install it.
- Wear an antistatic wrist strap.
- Do all preparation work on a static-free surface.
- Hold the device only by its edges. Be careful not to touch any of the components, contacts or connections.
- Avoid touching the pins or contacts on all modules and connectors. Hold modules or connectors by their ends.

**Important:**
Electrostatic discharge (ESD) can damage your processor, disk drive and other components. Perform the upgrade instruction procedures described at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

## Safety Measures

- To avoid damage to the system, use the correct AC input voltage range.
- To reduce the risk of electric shock, unplug the power cord before removing the system chassis cover for installation or servicing. After installation or servicing, cover the system chassis before plugging the power cord.

## About the Package

The package contains the following items. If any of these items are missing or damaged, please contact your dealer or sales representative for assistance.

The accessories in the package may not come similar to the information listed below. This may differ in accordance with the sales region or models in which it was sold. For more information about the standard package in your region, please contact your dealer or sales representative.

- Heat Sink (For Pentium & Celeron)
- Cooler (For Atom x6000 Series)

## Optional Items

The board and accessories in the package may not come similar to the information listed above. This may differ in accordance with the sales region or models in which it was sold. For more information about the standard package in your region, please contact your dealer or sales representative.

- Heat Spreader
- COM335 Carrier Board Kit

## Before Using the System Board

Before using the system board, prepare basic system components.
If you are installing the system board in a new system, you will need at least the following internal components.

- Storage devices such as hard disk drive, etc.

You will also need external system peripherals you intend to use which will normally include at least a keyboard, a mouse and a video display monitor.

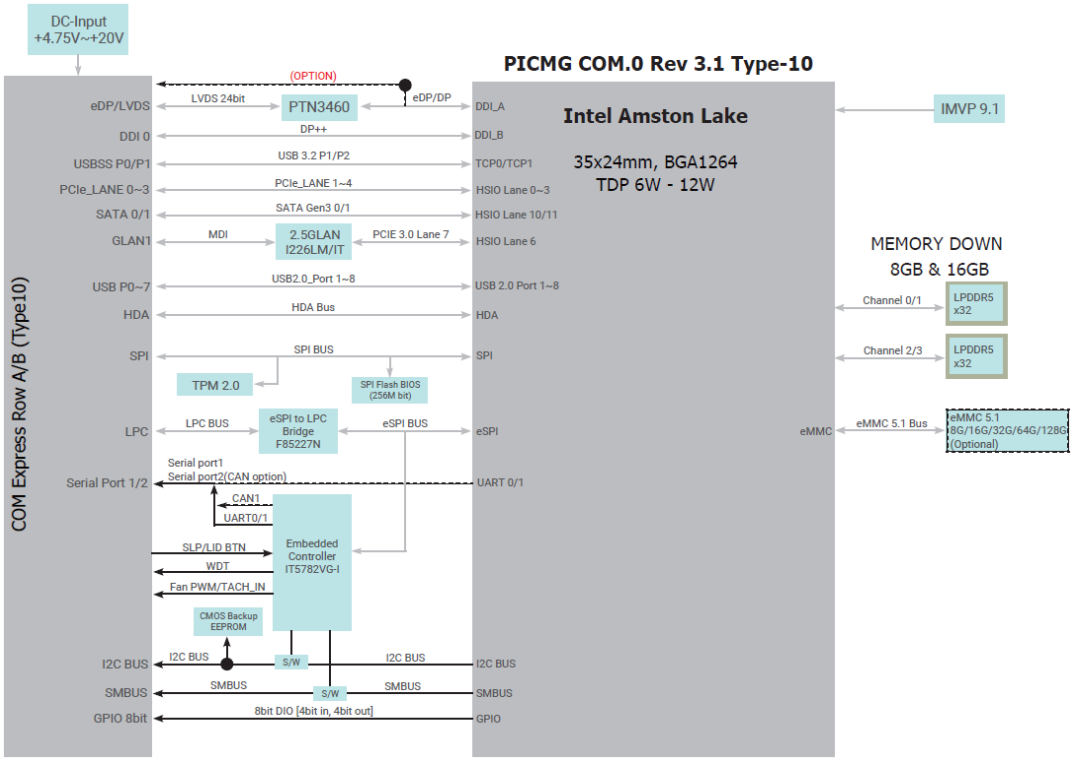
# Chapter 1 - Introduction

## ▶ Specification

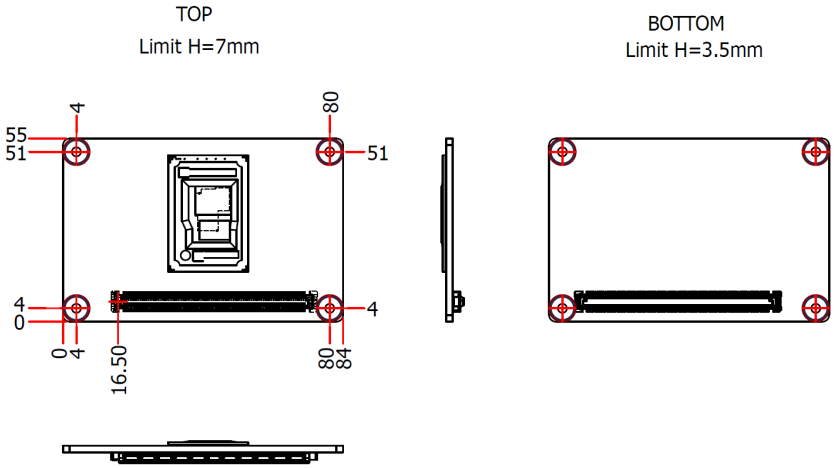
| | | |
|---|---|---|
| **SYSTEM** | Processor | Intel® Atom x7000RE series processors (Code Name : Amston Lake)<br>Intel® Atom Processor x7835RE, 8 Cores, 1.3~3.6GHz, 12W<br>Intel® Atom Processor x7433RE, 4 Cores, 1.5~3.4GHz, 9W<br>Intel® Atom Processor x7211RE, 2 Cores, 1.0~3.2GHz, 6W |
| | Memory | LPDDR5 up to 16GB<br>LPDDR5 4800MHz<br>**Note:**<br>**• 8GB/16GB supported by project basis.**<br>**• In-band ECC (IBECC) Supported by all CPU SKUs.** |
| | BIOS | AMI SPI 256Mbit |
| **GRAPHICS** | Controller | Intel® UHD |
| | Feature | Open GL 4.6, DirectX 12.1 Vulkan 1.2 (Windows)<br>Mesa 3D, Open GL 4.6, Vulkan 1.2 (Linux)<br>HW Decode: 4K60 10b 4:2:0, 4:4:4 HEVC/VP9/SCC, 4K60 10b 4:2:0 AV1<br>HW Encode: 4K60 10b 4:2:0, 4:4:4 HEVC/VP9/SCC |
| | Display | 1 x DDI<br>1 x LVDS/eDP<br>LVDS: single channel 24-bit, resolution up to 1920x1200 @ 60Hz<br>eDP: resolution up to 4096x2160 @ 60Hz<br>HDMI: resolution up to 4096x2160 @ 30Hz<br>DP++: resolution up to 4096x2160 @ 60Hz, 3840x2160 @60Hz |
| | Dual Displays | DDI + LVDS/eDP |
| **EXPANSION** | Interface | 4 x PCIe x1 (Gen 3)<br>1 x $I^2C$<br>1 x SMBus<br>1 x LPC<br>2 x UART (TX/RX)<br>1 x CAN bus (available upon request) |
| **AUDIO** | Interface | HD Audio |
| **ETHERNET** | Controller | 1 x Intel® I226IT / I226-LM (10/100/1000Mbps/2.5Gbps) |
| **I/O** | USB | 2 x USB 3.2 Gen2<br>8 x USB 2.0 |
| | SATA | 2 x SATA 3.0 (up to 6Gb/s) |
| | eMMC | 1 x 8GB/16GB/32GB/64GB*/128GB eMMC 5.1 (available upon request) |
| | DIO | 1 x 8-bit DIO |

| | | |
|---|---|---|
| **WATCHDOG TIMER** | Output & Interval | System Reset, Programmable via Software from 1 to 255 Seconds |
| **SECURITY** | TPM | dTPM or fTPM (Opational) |
| **Power** | Type | 4.75V~20V, 5VSB, VCC_RTC (ATX mode)<br>4.75V~20V, VCC_RTC (AT mode) |
| | Consumption | TBD |
| **OS SUPPORT** | OS Support (UEFI Only) | Windows: 11/10 IoT Enterprise 64-bit<br>Linux |
| **ENVIRONMENT** | Temperature | Operating: -40 to 85°C<br>Storage: -40 to 85°C |
| | Humidity | Operating: 5 to 90% RH<br>Storage: 5 to 90% RH |
| | MTBF | TBD |
| **MECHANICAL** | Dimensions | COM Express® Mini 84mm (3.3") x 55mm (2.16") |
| | Compliance | PICMG COM Express® R3.1, Type 10 |
| **STANDARDS AND CERTIFICATIONS** | Certification | CE, FCC |

## ▶ Block Diagram



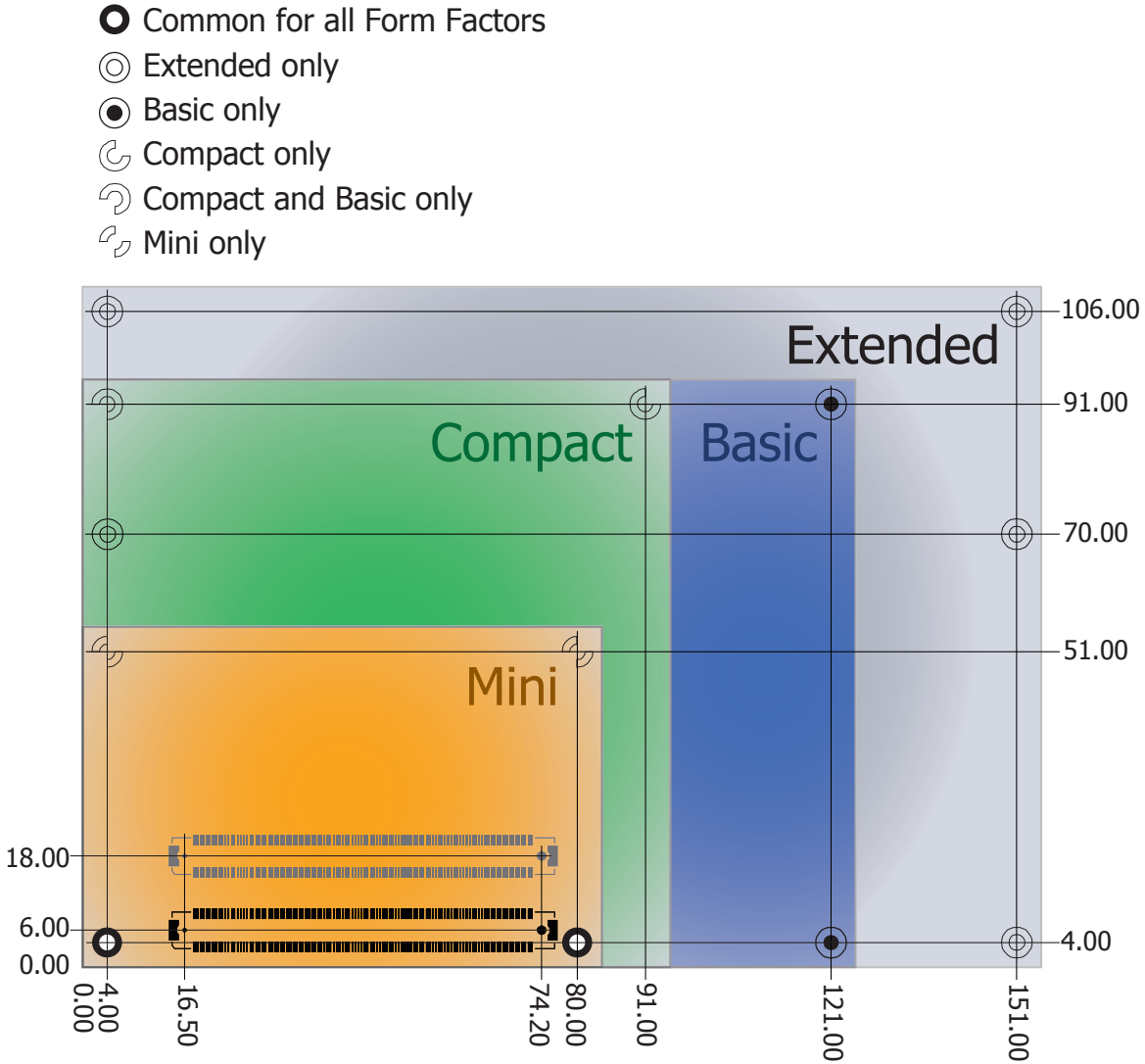

## ▶ Dimension



# Chapter 2 - Concept

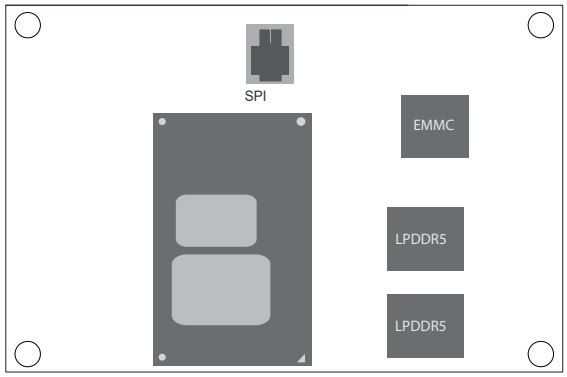
## ▶ COM Express Module Standards

The figure below shows the dimensions of the different types of COM Express modules.
ASL9A2 is a COM Express Mini. The dimension is 84mm x 55mm.

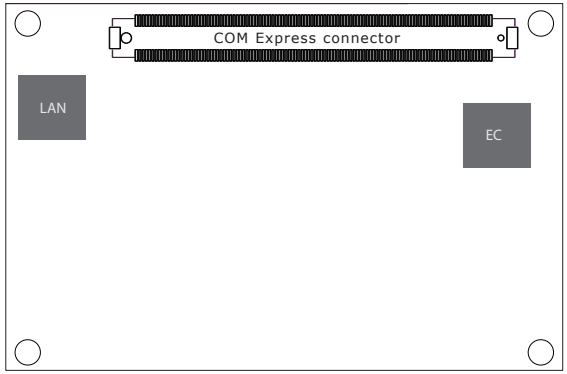


# Chapter 3 - Hardware Installation

## ▶ Board Layout



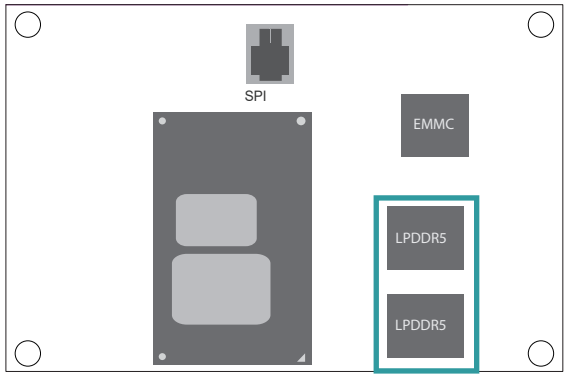

TOP VIEW




BOTTOM VIEW

## ▶ System Memory

The system board is equipped with LPDDR5 memory chips onboard.

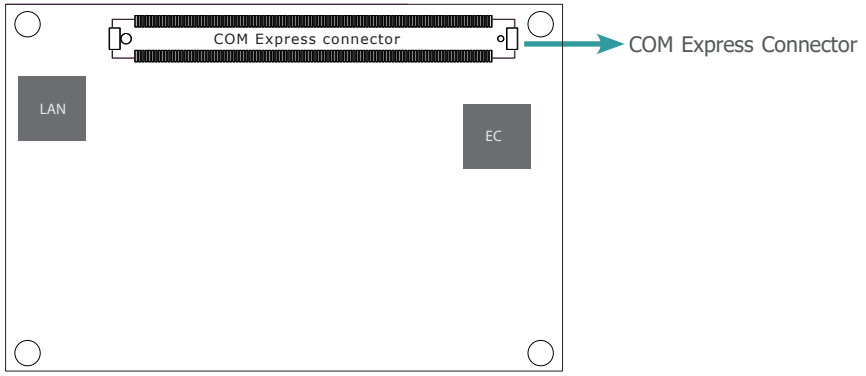



**Important:**
Boards, and other components. Perform installation procedures at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an anti-static wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

## ▶ Connector

### COM Express Connector

The COM Express connector is used to interface the ASL9A2 COM Express board to a carrier board. Connect the COM Express connector (located on the solder side of the board) to the COM Express connector on the carrier board.Refer to the following pages for the pin functions of the connector.



The table below shows the COM Express standard specifications and the corresponding specifications supported on the ASL9A2 module. Type 10 Modules support a single 24 bit LVDS panel interface, a single DDI and an eDP overlayed on LVDS Channel A.Two of the 8 USB ports can be used as USB 3.0.

| Connector | Feature | "Type 10 Min / Max" | "DFI Type 10 ASL9A2 (000G)" |
|---|---|---|---|
| • System I/O | | | |
| A-B | PCI Express Lanes 0 - 3 | 1 / 4 | 4 |
| A-B | NC-SI | NA | NA |
| A-B | 1Gb LAN Port 0 | 1 / 1 | 1 |
| A-B | DDI 0 | 0 / 1 | 1 |
| A-B | DDIs 1 - 3 | NA | NA |
| A-B | LVDS Channel A | 0 / 1 | 1 |
| A-B | LVDS Channel B | NA | NA |
| A-B | eDP on LVDS CH A pins | 0 / 1 | 1 |
| A-B | VGA Port | NA | NA |
| A-B | Serial Ports 1 - 2 | 0 / 2 | 2 |
| A-B | CAN interface on SER1 | 0 / 1 | 1 |
| A-B | SATA Ports | 1 / 2 | 2 |
| A-B | HD Audio | 0 / 1 | 1 |
| A-B | USB 2.0 Ports | 4 / 8 | 8 |
| A-B | USB0 Client | 0 / 1 | 0 |
| A-B | USB7 Client | 0 / 1 | 0 |
| A-B | USB 3.0 Ports | 0 / 2 | 2 |
| A-B | LPC Bus or eSPI | 1 / 1 | 1 LPC |
| A-B | SPI (Devices) | 1 / 2 | 1 |

| Connector | Feature | "Type 10 Min / Max" | "DFI Type 10 ASL9A2 (000G)" |
|---|---|---|---|
| • System Management | | | |
| A-B | General Purpose I/O | 8 / 8 | 8 |
| A-B | SMBus | 1 / 1 | 1 |
| A-B | I2C | 1 / 1 | 1 |
| A-B | Watchdog Timer | 0 / 1 | 1 |
| A-B | Speaker Out | 1 / 1 | 1 |
| A-B | Carrier Board BIOS Flash Support | 0 / 1 | 1 |
| A-B | Reset Functions | 1 / 1 | 1 |
| A-B | Trusted Platform Module | 0 / 1 | 1 |
| • Power Management | | | |
| A-B | Thermal Protection | 0 / 1 | 1 |
| A-B | Battery Low Alarm | 0 / 1 | 1 |
| A-B | Suspend/Wake Signals | 0 / 3 | 2 |
| A-B | Power Button Support | 1 / 1 | 1 |
| A-B | Power Good | 1 / 1 | 1 |
| A-B | VCC_5V_SBY Contacts | 4 / 4 | 4 |
| A-B[5] | Sleep Input | 0 / 1 | 1 |
| A-B[5] | Lid Input | 0 / 1 | 1 |
| A-B[5] | Carrier Board Fan Control | 0 / 1 | 1 |
| • Power | | | |
| A-B | VCC_12V Contacts | 12 / 12 | 12 |

**Note for A-B[5] :**
These signals use reclaimed VCC_12V pins. Refer to Module base specification Section 5.8 'Protecting COM.0 Pins Reclaimed from the VCC_12V Pool' for additional design considerations.

## ▶ COM Express Connector Signal Description

Pin Types
I : Input to the Module
O : Output from the Module
I/O : Bi-directional input / output signal
OD : Open drain output
RSVD : pins are reserved for future use and should be no connect. Do not tie the RSVD pins together.

**HDA Signals Descriptions**

| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | ASL9A2 PU/PD | Module Base Specification R3.1 Description | COM Express Carrier Design Guide R2.0 Description |
|---|---|---|---|---|---|---|
| HDA_RST# | A30 | O CMOS | 3.3V Suspend/3.3V | series 33Ω resistor | Reset output to CODEC, active low. | CODEC Reset. |
| HDA_SYNC | A29 | O CMOS | 3.3V/3.3V | series 33Ω resistor | Sample-synchronization signal to the CODEC(s). | Serial Sample Rate Synchronization. |
| HDA_BITCLK | A32 | I/O CMOS | 3.3V/3.3V | series 33Ω resistor | Serial data clock generated by the external CODEC(s). | 24 MHz Serial Bit Clock for HDA CODEC. |
| HDA_SDOUT | A33 | O CMOS | 3.3V/3.3V | series 33Ω resistor | Serial TDM data output to the CODEC. | Audio Serial Data Output Stream. |
| HDA_SDIN0 | B30 | I/O CMOS | 3.3V Suspend/3.3V | | Serial TDM data input from up to 3 CODECs.<br>Alternative use as SoundWire bi-directional data line | Audio Serial Data Input Stream from CODEC[0:2] or alternative use as SoundWire bi-driection clock line |
| HDA_SDIN1 | B29 | I/O CMOS | 3.3V Suspend/3.3V<br>1.8V Suspend/3.3V | | | |
| HDA_SDIN2 | B28 | I/O CMOS | 3.3V Suspend/3.3V<br>1.8V Suspend/3.3V | | | |

**Gigabit Ethernet Signals Descriptions**

| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | ASL9A2 PU/PD | Module Base Specification R3.1 Description | COM Express Carrier Design Guide R2.0 Description |
|---|---|---|---|---|---|---|
| GBE0_MDI0+ | A13 | I/O Analog | 3.3V max Suspend | | Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. Some pairs are unused in some modes, per the following:<br>1000BASE-T 100BASE-TX 10BASE-T<br>MDI[0]+/- B1_DA+/- TX+/- TX+/-<br>MDI[1]+/- B1_DB+/- RX+/- RX+/-<br>MDI[2]+/- B1_DC+/-<br>MDI[3]+/- B1_DD+/- | Media Dependent Interface (MDI) differential pair 0. |
| GBE0_MDI0- | A12 | I/O Analog | 3.3V max Suspend | | | |
| GBE0_MDI1+ | A10 | I/O Analog | 3.3V max Suspend | | | Media Dependent Interface (MDI) differential pair 1. |
| GBE0_MDI1- | A9 | I/O Analog | 3.3V max Suspend | | | |
| GBE0_MDI2+ | A7 | I/O Analog | 3.3V max Suspend | | | Media Dependent Interface (MDI) differential pair 2.<br>Only used for 1000Mbit/sec Gigabit Ethernet mode. |
| GBE0_MDI2- | A6 | I/O Analog | 3.3V max Suspend | | | |
| GBE0_MDI3+ | A3 | I/O Analog | 3.3V max Suspend | | | Media Dependent Interface (MDI) differential pair 3.<br>Only used for 1000Mbit/sec Gigabit Ethernet mode. |
| GBE0_MDI3- | A2 | I/O Analog | 3.3V max Suspend | | | |
| GBE0_ACT# | B2 | OD CMOS | 3.3V Suspend/3.3V | | Gigabit Ethernet Controller 0 activity indicator, active low. | Ethernet controller 0 activity indicator, active low. |
| GBE0_LINK# | A8 | OD CMOS | 3.3V Suspend/3.3V | Only at Pin A4 or A5 link speed the GBE0_LINK# will active low. | Gigabit Ethernet Controller 0 link indicator, active low. | Ethernet controller 0 link indicator, active low. |
| GBE0_LINK_MID# | A4 | OD CMOS | 3.3V Suspend/3.3V | LED for link speed with 1Gbps. | A speed lower than the maximum speed supported, active low. | A speed lower than the maximum speed supported, active low. |
| GBE0_LINK_MAX# | A5 | OD CMOS | 3.3V Suspend/3.3V | LED for link speed with 2.5Gbps | At the maximum link speed supported by the controller, active low. | At the maximum link speed supported by the controller, active low. |
| GBE0_CTREF | A14 | REF | GND min, 3.3V max | NC | Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V.<br>The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be limited to 250 mA or less. | Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. |
| GBE0_SDP | A49 | I/O | 3.3V Suspend/3.3V | | Gigabit Ethernet Controller 0 Software-Definable Pin.<br>Can also be used for IEEE1588 support such as a 1pps signal. | |

**SATA Signals Descriptions**

| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | ASL9A2 PU/PD | Module Base Specification R3.1 Description | COM Express Carrier Design Guide R2.0 Description |
|---|---|---|---|---|---|---|
| SATA0_TX+ | A16 | O SATA | AC coupled on Module | AC Coupling capacitor | Serial ATA or SAS Channel 0 transmit differential pair. | Serial ATA channel 0<br>Transmit output differential pair. |
| SATA0_TX- | A17 | O SATA | AC coupled on Module | AC Coupling capacitor | | |
| SATA0_RX+ | A19 | I SATA | AC coupled on Module | AC Coupling capacitor | Serial ATA or SAS Channel 0 receive differential pair. | Serial ATA channel 0<br>Receive input differential pair. |
| SATA0_RX- | A20 | I SATA | AC coupled on Module | AC Coupling capacitor | | |
| SATA1_TX+ | B16 | O SATA | AC coupled on Module | AC Coupling capacitor | Serial ATA or SAS Channel 1 transmit differential pair. | Serial ATA channel 1<br>Transmit output differential pair. |
| SATA1_TX- | B17 | O SATA | AC coupled on Module | AC Coupling capacitor | | |
| SATA1_RX+ | B19 | I SATA | AC coupled on Module | AC Coupling capacitor | Serial ATA or SAS Channel 1 receive differential pair. | Serial ATA channel 1<br>Receive input differential pair. |
| SATA1_RX- | B20 | I SATA | AC coupled on Module | AC Coupling capacitor | | |
| (S)ATA_ACT# | A28 | I/O CMOS | 3.3V / 3.3V | Single buffer | Serial ATA (activity indicator), active low. | Serial ATA activity LED. Open collector output pin driven during SATA command activity. |

## ▶ COM Express Connector Signal Description

| PCI Express Lanes Signals Descriptions | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | ASL9A2 PU/PD | Module Base Specification R3.1 Description | COM Express Carrier Design Guide R2.0 Description |
| PCIE_TX0+ | A68 | O PCIE | AC coupled on Module | AC Coupling capacitor | PCI Express Differential Transmit Pairs 0 | PCIe channel 0. Transmit Output differential pair. |
| PCIE_TX0- | A69 | | | AC Coupling capacitor | | |
| PCIE_RX0+ | B68 | I PCIE | AC coupled off Module | | PCI Express Differential Receive Pairs 0 | PCIe channel 0. Receive Input differential pair. |
| PCIE_RX0- | B69 | | | | | |
| PCIE_TX1+ | A64 | O PCIE | AC coupled on Module | AC Coupling capacitor | PCI Express Differential Transmit Pairs 1 | PCIe channel 1. Transmit Output differential pair. |
| PCIE_TX1- | A65 | | | AC Coupling capacitor | | |
| PCIE_RX1+ | B64 | I PCIE | AC coupled off Module | | PCI Express Differential Receive Pairs 1 | PCIe channel 1. Receive Input differential pair. |
| PCIE_RX1- | B65 | | | | | |
| PCIE_TX2+ | A61 | O PCIE | AC coupled on Module | AC Coupling capacitor | PCI Express Differential Transmit Pairs 2 | PCIe channel 2. Transmit Output differential pair. |
| PCIE_TX2- | A62 | | | AC Coupling capacitor | | |
| PCIE_RX2+ | B61 | I PCIE | AC coupled off Module | | PCI Express Differential Receive Pairs 2 | PCIe channel 2. Receive Input differential pair. |
| PCIE_RX2- | B62 | | | | | |
| PCIE_TX3+ | A58 | O PCIE | AC coupled on Module | AC Coupling capacitor | PCI Express Differential Transmit Pairs 3 | PCIe channel 3. Transmit Output differential pair. |
| PCIE_TX3- | A59 | | | AC Coupling capacitor | | |
| PCIE_RX3+ | B58 | I PCIE | AC coupled off Module | | PCI Express Differential Receive Pairs 3 | PCIe channel 3. Receive Input differential pair. |
| PCIE_RX3- | B59 | | | | | |
| PCIE_CLK_REF+ | A88 | O PCIE | PCIE | | Reference clock output for all PCI Express and PCI Express Graphics lanes. | PCIe Reference Clock for all COM Express PCIe lanes, and for PEG lanes. |
| PCIE_CLK_REF- | A89 | | | | | |
| PCIE_CLK_REQ1_BTB# | B52 | COMS | 3.3V/3.3V | | Reserved Pin | NC |

**Note: For PCIe device down or slot card components on the carrier board, please use the PCIe Lane0 port first.**

| USB Signals Descriptions | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | ASL9A2 PU/PD | Module Base Specification R3.1 Description | COM Express Carrier Design Guide R2.0 Description |
| USB0+ | A46 | I/O USB | 3.3V Suspend/3.3V | | USB differential pairs, channel 0. If implemented, shall be host ports. | USB Port 0, data + or D+ |
| USB0- | A45 | | | | | USB Port 0, data - or D- |
| USB1+ | B46 | I/O USB | 3.3V Suspend/3.3V | | USB differential pairs, channel 1. If implemented, shall be host ports. | USB Port 1, data + or D+ |
| USB1- | B45 | | | | | USB Port 1, data - or D- |
| USB2+ | A43 | I/O USB | 3.3V Suspend/3.3V | | USB differential pairs, channel 2. If implemented, shall be host ports. | USB Port 2, data + or D+ |
| USB2- | A42 | | | | | USB Port 2, data - or D- |
| USB3+ | B43 | I/O USB | 3.3V Suspend/3.3V | | USB differential pairs, channel 3. If implemented, shall be host ports. | USB Port 3, data + or D+ |
| USB3- | B42 | | | | | USB Port 3, data - or D- |
| USB4+ | A40 | I/O USB | 3.3V Suspend/3.3V | | USB differential pairs, channel 4. If implemented, shall be host ports. | USB Port 4, data + or D+ |
| USB4- | A39 | | | | | USB Port 4, data - or D- |
| USB5+ | B40 | I/O USB | 3.3V Suspend/3.3V | | USB differential pairs, channel 5. If implemented, shall be host ports. | USB Port 5, data + or D+ |
| USB5- | B39 | | | | | USB Port 5, data - or D- |
| USB6+ | A37 | I/O USB | 3.3V Suspend/3.3V | | USB differential pairs, channel 6. If implemented, shall be host ports. | USB Port 6, data + or D+ |
| USB6- | A36 | | | | | USB Port 6, data - or D- |
| USB7+ | B37 | I/O USB | 3.3V Suspend/3.3V | | USB differential pairs, channel 7. If implemented, shall be host ports. | USB Port 7, data + or D+ |
| USB7- | B36 | | | | | USB Port 7, data - or D- |
| USB_0_1_OC# | B44 | I CMOS | 3.3V Suspend/3.3V | PU 10KΩ to 3.3V Suspend | USB over-current sense, USB channels 0 and 1.<br>A pull-up for this line shall be present on the Module.<br>An open drain driver from a USB current monitor on the Carrier Board may drive this line low.<br>Do not pull this line high on the Carrier Board. | USB over-current sense, USB ports 0 and 1.<br>Do not pull up these lines to 3.3V on the Carrier Board – this shall be done on the Module. |

## ▶ COM Express Connector Signal Description

| | | | | | | |
|---|---|---|---|---|---|---|
| USB_2_3_OC# | A44 | I CMOS | 3.3V Suspend/3.3V | PU 10KΩ to 3.3V Suspend | USB over-current sense, USB channels 2 and 3.<br>A pull-up for this line shall be present on the Module.<br>An open drain driver from a USB current monitor on the Carrier Board may drive this line low.<br>Do not pull this line high on the Carrier Board. | USB over-current sense, USB ports 2 and 3.<br>Do not pull up these lines to 3.3V on the Carrier Board – this shall be done on the Module. |
| USB_4_5_OC# | B38 | I CMOS | 3.3V Suspend/3.3V | PU 10KΩ to 3.3V Suspend | USB over-current sense, USB channels 4 and 5.<br>A pull-up for this line shall be present on the Module.<br>An open drain driver from a USB current monitor on the Carrier Board may drive this line low.<br>Do not pull this line high on the Carrier Board. | USB over-current sense, USB ports 4 and 5.<br>Do not pull up these lines to 3.3V on the Carrier Board – this shall be done on the Module. |
| USB_6_7_OC# | A38 | I CMOS | 3.3V Suspend/3.3V | PU 10KΩ to 3.3V Suspend | USB over-current sense, USB channels 6 and 7.<br>A pull-up for this line shall be present on the Module.<br>An open drain driver from a USB current monitor on the Carrier Board may drive this line low.<br>Do not pull this line high on the Carrier Board. | USB over-current sense, USB ports 6 and 7.<br>Do not pull up these lines to 3.3V on the Carrier Board – this shall be done on the Module. |
| USB_SSTX0+ | B23 | O PCIE | AC coupled on Module | AC Coupling capacitor | Additional transmit signal differential pairs for the SuperSpeed USB data path. | USB Port 0, SuperSpeed TX + |
| USB_SSTX0- | B22 | | | AC Coupling capacitor | | USB Port 0, SuperSpeed TX - |
| USB_SSRX0+ | A23 | I PCIE | AC coupled off Module | | Additional receive signal differential pairs for the SuperSpeed USB data path. | USB Port 0, SuperSpeed RX + |
| USB_SSRX0- | A22 | | | | | USB Port 0, SuperSpeed RX - |
| USB_SSTX1+ | B26 | O PCIE | AC coupled on Module | AC Coupling capacitor | Additional transmit signal differential pairs for the SuperSpeed USB data path. | USB Port 1, SuperSpeed TX + |
| USB_SSTX1- | B25 | | | AC Coupling capacitor | | USB Port 1, SuperSpeed TX - |
| USB_SSRX1+ | A26 | I PCIE | AC coupled off Module | | Additional receive signal differential pairs for the SuperSpeed USB data path. | USB Port 1, SuperSpeed RX + |
| USB_SSRX1- | A25 | | | | | USB Port 1, SuperSpeed RX - |
| USB0_HOST_PRSNT | B48 | I CMOS | 3.3V Suspend/3.3V | N.C. | Module USB client may detect the presence of a USB host on USB0. A high value indicates that a host is present. | |
| USB7_HOST_PRSNT | B96 | I CMOS | 3.3V Suspend/3.3V | N.C. | Module USB client may detect the presence of a USB host on USB7. A high value indicates that a host is present. | |

| **LVDS Signals Descriptions** | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | ASL9A2 PU/PD | Module Base Specification R3.1 Description | COM Express Carrier Design Guide R2.0 Description |
| LVDS_A0+/eDP_TX2+ | A71 | O LVDS | LVDS<br>EDP: AC coupled off Module | | LVDS Channel A differential pairs<br>eDP: eDP differential pairs | LVDS channel A differential signal pair 0<br>eDP lane 2, TX± differential signal pair |
| LVDS_A0-/eDP_TX2- | A72 | | | | | |
| LVDS_A1+/eDP_TX1+ | A73 | O LVDS | LVDS<br>EDP: AC coupled off Module | | | LVDS channel A differential signal pair 1<br>eDP lane 1, TX± differential signal pair |
| LVDS_A1-/eDP_TX1- | A74 | | | | | |
| LVDS_A2+/eDP_TX0+ | A75 | O LVDS | LVDS<br>EDP: AC coupled off Module | | | LVDS channel A differential signal pair 2<br>eDP lane 0, TX± differential signal pair |
| LVDS_A2-/eDP_TX0- | A76 | | | | | |
| LVDS_A3+ | A78 | O LVDS | LVDS<br>EDP: AC coupled off Module | | | LVDS channel A differential signal pair 3 |
| LVDS_A3- | A79 | | | | | |
| LVDS_A_CK+/eDP_TX3+ | A81 | O LVDS | LVDS<br>EDP: AC coupled off Module | | LVDS Channel A differential clock<br>eDP: eDP differential pairs | LVDS channel A differential clock pair<br>eDP lane 3, TX± differential pair |
| LVDS_A_CK-/eDP_TX3- | A82 | | | | | |

## ▶ COM Express Connector Signal Description

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|---|---|---|---|---|---|---|
| LVDS_VDD_EN/eDP_VDD_EN | A77 | O CMOS | 3.3V / 3.3V | PD 100KΩ to GND | LVDS panel / eDP power enable | LVDS flat panel power enable. eDP power enable |
| LVDS_BKLT_EN/eDP_BKLT_EN | B79 | O CMOS | 3.3V / 3.3V | PD 100KΩ to GND | LVDS panel / eDP backlight enable | LVDS flat panel backlight enable high active signal eDP backlight enable |
| LVDS_BKLT_CTRL/eDP_BKLT_CTRL | B83 | O CMOS | 3.3V / 3.3V | PD 100KΩ to GND | LVDS panel / eDP backlight brightness control | LVDS flat panel backlight brightness control EDP backlight brightness control |
| LVDS_I2C_CK/eDP_AUX+ | A83 | I/O OD CMOS | 3.3V / 3.3V | PU 4.7KΩ to 3.3V | I2C clock output for LVDS display use / eDP AUX+ | DDC I2C clock signal used for flat panel detection and control. eDP auxiliary lane + |
| LVDS_I2C_DAT/eDP_AUX- | A84 | I/O OD CMOS | 3.3V / 3.3V | PU 4.7KΩ to 3.3V | I2C data line for LVDS display use / eDP AUX- | DDC I2C data signal used for flat panel detection and control. eDP auxiliary lane - |
| RSVD/eDP_HPD | A87 | I CMOS | 3.3V / 3.3V | eDP: PD 100KΩ to GND | eDP_HPD:Detection of Hot Plug / Unplug and notification of the link layer | eDP_HPD: Detection of Hot Plug / Unplug and notification of the link layer |
| **LPC Signals Descriptions** | | | | | | |
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | ASL9A2 PU/PD **(LPC mode only.)** | Module Base Specification R3.1 Description | COM Express Carrier Design Guide R2.0 Description |
| LPC_AD0/ESPI_IO_0 | B4 | I/O CMOS | LPC: 3.3V / 3.3V<br>ESPI: 1.8V Suspend / 1.8V | | LPC mode: LPC multiplexed address, command and data bus.<br>ESPI mode: eSPI Master Data Input / Outputs These are bi-directional input/output pins used to transfer data between master and slaves. | LPC multiplexed command, address and data. |
| LPC_AD1/ESPI_IO_1 | B5 | | | | | |
| LPC_AD2/ESPI_IO_2 | B6 | | | | | |
| LPC_AD3/ESPI_IO_3 | B7 | | | | | |
| LPC_FRAME#/ESPI_CS0# | B3 | O CMOS | LPC: 3.3V / 3.3V<br>ESPI: 1.8V Suspend / 1.8V | | LPC mode: LPC frame indicates the start of an LPC cycle.<br>ESPI Mode: eSPI Master Chip Select Outputs Driving Chip Select0#.<br>A low selects a particular eSPI slave for the transaction.<br>Each of the eSPI slaves is connected to a dedicated Chip Selectn# pin. | LPC frame indicates start of a new cycle or termination of a broken cycle. |
| LPC_DRQ0#/ESPI_ALERT0# | B8 | I CMOS | LPC: 3.3V / 3.3V<br>ESPI: 1.8V Suspend / 1.8V | PU 10K to 3.3V, not used. | LPC mode: LPC serial DMA request<br>ESPI Mode: eSPI pins used by eSPI slave to request service from the eSPI master. | LPC encoded DMA/Bus master request. |
| LPC_DRQ1#/ESPI_ALERT1# | B9 | | | PU 10K to 3.3V, not used. | | |
| LPC_SERIRQ/ESPI_CS1# | A50 | I/O CMOS<br>O CMOS | LPC: 3.3V / 3.3V<br>ESPI: 1.8V Suspend / 1.8V | PU 10K to 3.3V | LPC mode: LPC serial interrupt<br>ESPI Mode: eSPI Master Chip Select Outputs Driving Chip Select# A low selects a particular eSPI slave for the transaction.<br>Each of the eSPI slaves is connected to a dedicated Chip Selectn# pin. | LPC serialized IRQ. |
| LPC_CLK/ESPI_CK | B10 | O CMOS | LPC: 3.3V / 3.3V<br>ESPI: 1.8V Suspend / 1.8V | series 33Ω resistor (32MHz) | LPC mode: LPC clock output - 33MHz nominal<br>ESPI Mode: eSPI Master Clock Output This pin provides the reference timing for all the serial input and output operations. | LPC clock output 33MHz. |
| SUS_STAT#/ESPI_RESET# | B18 | O CMOS | LPC: 3.3V / 3.3V<br>ESPI: 1.8V Suspend / 1.8V | N.C. | LPC Mode: SUS_STAT# indicates imminent suspend operation. It is used to notify LPC devices that a low power state will be entered soon.<br>ESPI Mode: eSPI Reset Reset the eSPI interface for both master and slaves. eSPI Reset# is typically driven from eSPI master to eSPI slaves. | Suspend status signal to indicate that the system will be entering a low power state soon. It can be used by other peripherals on the Carrier Board as an indication that they should go into power-down mode. |
| ESPI_EN# | B47 | I CMOS | NA | N.C. | This signal is used by the Carrier to indicate the operating mode of the LPC/eSPI bus.<br>If left unconnected on the carrier, LPC mode (default) is selected.<br>If pulled to GND on the carrier, eSPI mode is selected.<br>This signal is pulled to a logic high on the module through a resistor.<br>The Carrier should only float this line or pull it low. | |

## ▶ COM Express Connector Signal Description

| DDI Signals Descriptions | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | ASL9A2 PU/PD | Module Base Specification R3.1 Description | COM Express Carrier Design Guide R2.0 Description |
| DDI0_PAIR0+ | B71 | O PCIE | AC coupled off Module | | DDI for Display Port: DP0_LANE 0 differential pairs<br>Uni-directional main link for the transport of isochronous streams and secondary data packets.<br>DDI for HDMI/DVI: TMDS0_DATA lanes 2 differential pairs | DP1_LANE0+ for DP / TMDS1_DATA2+ for HDMI or DVI |
| DDI0_PAIR0- | B72 | | | | | DP1_LANE0- for DP / TMDS1_DATA2- for HDMI or DVI |
| DDI0_PAIR1+ | B73 | OPCIE | AC coupled off Module | | DDI for Display Port: DP0_LANE 1 differential pairs<br>Uni-directional main link for the transport of isochronous streams and secondary data packets.<br>DDI for HDMI/DVI: TMDS0_DATA lanes 1 differential pairs | DP1_LANE1+ for DP / TMDS1_DATA1+ for HDMI or DVI |
| DDI0_PAIR1- | B74 | | | | | DP1_LANE1- for DP / TMDS1_DATA1- for HDMI or DVI |
| DDI0_PAIR2+ | B75 | O PCIE | AC coupled off Module | | DDI for Display Port: DP0_LANE 2 differential pairs<br>Uni-directional main link for the transport of isochronous streams and secondary data packets.<br>DDI for HDMI/DVI: TMDS0_DATA lanes 0 differential pairs | DP1_LANE2+ for DP / TMDS1_DATA0+ for HDMI or DVI |
| DDI0_PAIR2- | B76 | | | | | DP1_LANE2- for DP / TMDS1_DATA0- for HDMI or DVI |
| DDI0_PAIR3+ | B81 | O PCIE | AC coupled off Module | | DDI for Display Port: DP0_LANE 3 differential pairs<br>Uni-directional main link for the transport of isochronous streams and secondary data packets.<br>DDI for HDMI/DVI: TMDS0_CLK differential pairs | DP1_LANE3+ for DP / TMDS1_CLK+ |
| DDI0_PAIR3- | B82 | | | | | DP1_LANE3- for DP / TMDS1_CLK- |
| DDI0_PAIR4+ | B77 | I PCIE | AC coupled off Module | NC | | NA |
| DDI0_PAIR4- | B78 | | | NC | | NA |
| DDI0_PAIR5+ | B91 | I PCIE | AC coupled off Module | NC | | NA |
| DDI0_PAIR5- | B92 | | | NC | | NA |
| DDI0_PAIR6+ | B93 | I PCIE | AC coupled off Module | NC | | NA |
| DDI0_PAIR6- | B94 | | | NC | | NA |
| DDI0_CTRLCLK_AUX+ | B98 | I/O PCIE | AC coupled on Module | PD 100KΩ to GND<br>**(S/W IC between Rpu/PCH)** | DDI for Display Port: DP0_AUX+ Differetial pairs<br>(DP AUX+ function if DDI0_DDC_AUX_SEL is no connect)<br>Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access | DP1_AUX+ for DP |
| | | I/O OD CMOS | 3.3V / 3.3V | PU 2.2KΩ to 3.3V, PD 100KΩ to GND<br>**(S/W IC between AB Rpu/Rpd resistor)** | DDI for HDMI/DVI: HDMI0_CTRL_CLK<br>(HDMI/DVI I2C CTRLCLK if DDI0_DDC_AUX_SEL is pulled high) | HDMI1_CTRLCLK for HDMI or DVI |
| DDI0_CTRLCLK_AUX- | B99 | I/O PCIE | AC coupled on Module | PU 100KΩ to 3.3V<br>**(S/W IC between Rpu/PCH)** | DDI for Display Port: DP0_AUX- Differetial pairs<br>(DP AUX- function if DDI0_DDC_AUX_SEL is no connect)<br>Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access | DP1_AUX- for DP |
| | | I/O OD CMOS | 3.3V / 3.3V | PU 2.2KΩ to 3.3V/PU 100KΩ to 3.3V<br>**(S/W IC between AB Rpu/Rpd resistor)** | DDI for HDMI/DVI: HDMI0_CTRL_DATA<br>(HDMI/DVI I2C CTRLDATA if DDI0_DDC_AUX_SEL is pulled high) | HDMI1_CTRLDATA for HDMI or DVI |
| DDI0_HPD | B89 | I CMOS | 3.3V / 3.3V | PD 100KΩ to GND | DDI for Display Port: DP0_HPD (Detection of Hot Plug / Unplug and notification of the link layer)<br>DDI for HDMI/DVI: HDMI0_HPD (HDMI/DVI Hot-Plug Detect) | DP1_HPD for DP / HDMI1_HPD for HDMI or DVI.<br>When carriers that support TMDS(HDMI/DVI), the Carrier shall include a blocking FET on DDI0_HPD to prevent back-drive current from damaging the Module. |
| DDI0_DDC_AUX_SEL | B95 | I CMOS | 3.3V / 3.3V | PD 1MΩ to GND | Selects the function of DDI0_CTRLCLK_AUX+ and DDI0_CTRLDATA_AUX-.<br>This pin shall have a 1M pull-down to logic ground on the Module.<br>If this input is unconnected the AUX pair is used for the DP AUX+/- signals.<br>If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals. | Selects the function of DP1 AUX±(Low) or HDMI1 DDC CLK/DATA(High)<br>The DDC_AUX_SEL pin should be routed to pin 13 of the DisplayPort connector, to enable Dual-Mode DisplayPort interface.<br>When HDMI/DVI is directly done on the Carrier Board, this pin shall be pulled to 3.3V with a 100k Ohm resistor to configure the DDI[0]_AUX pairs as DDC channels. |

## ▶ COM Express Connector Signal Description

| **Serial Interface Signals Descriptions** | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | ASL9A2 PU/PD | Module Base Specification R3.1 Description | COM Express Carrier Design Guide R2.0 Description |
| SER0_TX | A98 | O CMOS | 3.3V/12V | | General purpose serial port 0 transmitter | Transmit Line for Serial Port 0 ; PD 4.7KΩ |
| SER0_RX | A99 | I CMOS | 3.3V/12V | PU 10KΩ to 3.3V | General purpose serial port 0 receiver | Receive Line for Serial Port 0 |
| SER1_TX /CAN_TX | A101 | O CMOS | 3.3V/12V | | General purpose serial port 1 transmitter | Transmit Line for Serial Port 1 ; PD 4.7KΩ |
| SER1_RX/CAN_RX | A102 | I CMOS | 3.3V/12V | PU 10KΩ to 3.3V for UART | General purpose serial port 1 receiver | Receive Line for Serial Port 1 |
| **I2C Signal Descriptions** | | | | | | |
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | ASL9A2 PU/PD | Module Base Specification R3.1 Description | COM Express Carrier Design Guide R2.0 Description |
| I2C_CK | B33 | I/O OD CMOS | 3.3V Suspend/3.3V | PU 2.2K to 3.3V Suspend | General purpose I2C port clock output | General Purpose I2C Clock output |
| I2C_DAT | B34 | I/O OD CMOS | 3.3V Suspend/3.3V | PU 2.2K to 3.3V Suspend | General purpose I2C port data I/O line | General Purpose I2C data I/O line. |
| **Miscellaneous Signal Descriptions** | | | | | | |
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | ASL9A2 PU/PD | Module Base Specification R3.1 Description | COM Express Carrier Design Guide R2.0 Description |
| SPKR | B32 | O CMOS | 3.3V / 3.3V | | Output for audio enunciator - the "speaker" in PC-AT systems. This port provides the PC beep signal and is mostly intended for debugging purposes. | Output used to control an external FET or a logic gate to drive an external PC speaker. |
| WDT | B27 | O CMOS | 3.3V / 3.3V | | Output indicating that a watchdog time-out event has occurred. | Output indicating that a watchdog time-out event has occurred. |
| FAN_PWMOUT | B101 | O CMOS | 3.3V / 12V | RSV PD 100KΩ to GND | Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM. | Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM. |
| FAN_TACHIN | B102 | I OD CMOS | 3.3V / 12V | PU 47KΩ to 3.3V | Fan tachometer input for a fan with a two pulse output. | Fan tachometer input for a fan with a two pulse output. |
| TPM_PP | A96 | I CMOS | 3.3V / 3.3V | PD 10KΩ to GND. | Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM. | Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. Thissignal is used to indicate Physical Presence to the TPM. |

## ▶ COM Express Connector Signal Description

| Power and System Management Signals Descriptions | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | ASL9A2 PU/PD | Module Base Specification R3.1 Description | COM Express Carrier Design Guide R2.0 Description |
| PWRBTN# | B12 | I CMOS | 3.3V Suspend/3.3V | PU 10KΩ to 3.3V Suspend | A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off and other suspend states, as well as powering the system down. | Power button low active signal used to wake up the system from S5 state (soft off). This signal is triggered on the falling edge. |
| SYS_RESET# | B49 | I CMOS | 3.3V Suspend/3.3V | PU 10KΩ to 3.3V Suspend | Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used. | Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used. |
| CB_RESET# | B50 | O CMOS | 3.3V Suspend/3.3V | AND gate out with series 33Ω resistor | Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software. | Reset output signal from Module to Carrier Board. This signal may be driven low by the Module to reset external components located on the Carrier Board. |
| PWR_OK | B24 | I CMOS | 3.3V / 3.3V | PU 10KΩ to 5V and PD 20KΩ that divide to 3.3V. | Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGAs or other configurable devices time to be programmed. | Power OK status signal generated by the ATX power supply to notify the Module that the DC operating voltages are within the ranges required for proper operation. |
| SUS_STAT# | B18 | O CMOS | 3.3V Suspend/3.3V | N.C | Indicates imminent suspend operation; used to notify LPC devices. | Suspend status signal to indicate that the system will be entering a low power state soon. It can be used by other peripherals on the Carrier Board as an indication that they should go into power-down mode. |
| SUS_S3# | A15 | O CMOS | 3.3V Suspend/3.3V | PD 100KΩ to GND | Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board may be used to enable the non-standby power on a typical ATX supply. | S3 Sleep control signal indicating that the system resides in S3 state (Suspend to RAM). |
| SUS_S4# | A18 | O CMOS | 3.3V Suspend/3.3V | PD 100KΩ to GND | Indicates system is in Suspend to Disk state. Active low output. | S4 Sleep control signal indicating that the system resides in S4 state (Suspend to Disk). |
| SUS_S5# | A24 | O CMOS | 3.3V Suspend/3.3V | PD 100KΩ to GND | Indicates system is in Soft Off state. | S5 Sleep Control signal indicating that the system resides in S5 State (Soft Off). |
| WAKE0# | B66 | I CMOS | 3.3V Suspend/3.3V | PU 10KΩ to 3.3V Suspend | PCI Express wake up signal. | PCI Express wake-up event signal. |
| WAKE1# | B67 | I CMOS | 3.3V Suspend/3.3V | PU 10KΩ to 3.3V Suspend | General purpose wake up signal. May be used to implement wake-up on PS2 keyboard or mouse activity. | General purpose wake-up signal. |
| BATLOW# | A27 | I CMOS | 3.3V Suspend/ 3.3V | PU 10KΩ to 3.3V Suspend | Indicates that external battery is low. This port provides a battery-low signal to the Module for orderly transitioning to power saving or power cut-off ACPI modes. | Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low. It also can be used to signal some other external power management event. |
| LID# | A103 | I OD CMOS | 3.3V Suspend/12V | PU 47KΩ to 3.3V Suspend | LID switch. Low active signal used by the ACPI operating system for a LID switch. | LID switch.<br>Low active signal used by the ACPI operating system for a LID switch. |
| SLEEP# | B103 | I OD CMOS | 3.3V Suspend/12V | PU 47KΩ to 3.3V Suspend | Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again. | Sleep button.<br>Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again. |

| Thermal Protection Signals Descriptions | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | ASL9A2 PU/PD | Module Base Specification R3.1 Description | COM Express Carrier Design Guide R2.0 Description |
| THRM# | B35 | I CMOS | 3.3V / 3.3V | PU 10KΩ to 3.3V | Input from off-Module temp sensor indicating an over-temp situation. | Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling. |
| THRMTRIP# | A35 | O CMOS | 3.3V / 3.3V | PU 10KΩ to 3.3V | Active low output indicating that the CPU has entered thermal shutdown. | Thermal Trip indicates an overheating condition of the processor. If 'THRMTRIP#' goes active the system immediately transitions to the S5 State (Soft Off). |

## ▶ COM Express Connector Signal Description

| SMBUS Signals Descriptions | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | ASL9A2 PU/PD | Module Base Specification R3.1 Description | COM Express Carrier Design Guide R2.0 Description |
| SMB_CK | B13 | I/O OD CMOS | 3.3V Suspend/3.3V | PU 2.2KΩ to 3.3V Suspend | System Management Bus bidirectional clock line. | System Management Bus bidirectional clock line |
| SMB_DAT | B14 | I/O OD CMOS | 3.3V Suspend/3.3V | PU 2.2KΩ to 3.3V Suspend | System Management Bus bidirectional data line. | System Management bidirectional data line. |
| SMB_ALERT# | B15 | I CMOS | 3.3V Suspend/3.3V | PU 2.2KΩ to 3.3V Suspend | System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system. | System Management Bus Alert |

| GPIO Signals Descriptions | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | ASL9A2 PU/PD | Module Base Specification R3.1 Description | COM Express Carrier Design Guide R2.0 Description |
| GPO0 | A93 | O CMOS | 3.3V / 3.3V | | GPIO: General purpose output pins. Upon a hardware reset, these outputs should be low.<br>SDIO: SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs.<br>This signal has maximum frequency of 48 MHz. Maps to GPO0. | General Purpose Outputs for system specific usage. |
| GPO1 | B54 | O CMOS | | | GPIO: General purpose output pins. Upon a hardware reset, these outputs should be low.<br>SDIO: SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.<br>Maps to GPO1. | |
| GPO2 | B57 | O CMOS / I CMOS | | | GPIO: General purpose output pins. Upon a hardware reset, these outputs should be low.<br>SDIO: SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.<br>Maps to GPO2; used as an input when used for SD card support. | |
| GPO3 | B63 | O CMOS / I CMOS | | | GPIO: General purpose output pins. Upon a hardware reset, these outputs should be low.<br>SDIO: SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.<br>Maps to GPO3; used as an input when used for SD card support. | |
| GPI0 | A54 | I CMOS / IO CMOS | 3.3V / 3.3V | PU 10KΩ to 3.3V @GPI | GPIO: General purpose input pins. Pulled high internally on the Module.<br>SDIO: SDIO Data lines. These signals operate in push-pull mode. Maps to GPI[0:3]. | General Purpose Input for system specific usage. The signals are pulled up by the Module. |
| GPI1 | A63 | I CMOS / IO CMOS | | PU 10KΩ to 3.3V @GPI | | |
| GPI2 | A67 | I CMOS / IO CMOS | | PU 10KΩ to 3.3V @GPI | | |
| GPI3 | A85 | I CMOS / IO CMOS | | PU 10KΩ to 3.3V @GPI | | |

## ▶ COM Express Connector Signal Description

| **Power and GND Signal Descriptions** | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | ASL9A2 PU/PD | Module Base Specification R3.1 Description | COM Express Carrier Design Guide R2.0 Description |
| VCC_12V | A104~A109<br>B104~B109 | Power | | | Primary power input supports wide range 4.75V ~ 20V voltage input.<br>All available VCC_12V pins on the connector(s) shall be used. | |
| VCC_5V_SBY | B84~B87 | Power | | | Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if<br>these functions are not used in the system design. | |
| VCC_RTC | A47 | Power | | | Real-time clock circuit-power input. Nominally +3.0V. | Battery cells must be protected against a reverse current going to the cell.<br>For revision 2.0 Carrier Boards, a protection low leakage diode and/or a series resistor shall be placed on the Carrier Board. |
| GND | A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1, B11, B21 ,B31, B41, B51, B60, B70, B80, B90, B100, B110 | Power | | | Ground - DC power and signal and AC signal return path.<br>All available GND connector pins shall be used and tied to Carrier Board GND plane. | |

| **Module type Signal Descriptions** | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | ASL9A2 PU/PD | Module Base Specification R3.1 Description | COM Express Carrier Design Guide R2.0 Description |
| TYPE10# | A97 | PDS | | PD 47K | Dual use pin. Indicates to the Carrier Board that a Type 10 Module is installed. Indicates to the Carrier that a Rev 1.0/2.0 Module is installed<br>TYPE10#<br>NC Pin-out R2.0<br>PD Pin-out Type 10 pull down to ground with 47K resistor<br>12V Pin-out R1.0<br>This pin is reclaimed from the VCC_12V pool. In R1.0 Modules this pin will connect to other VCC_12V pins. In R2.0 this pin is defined as a no connect for types 1-6. A Carrier can detect a R1.0 Module by the presence of 12V on this pin. R2.0 Module types 1-6 will no connect this pin. Type 10 Modules shall pull this pin to ground through a 47K resistor. | Indicates to the Carrier Board that a Type 10 Module is installed. Indicates to the Carrier Board, that a Rev 1.0/2.0 Module is installed.<br>TYPE10#<br>NC Pin-out R2.0<br>PD Pin-out Type 10 pull down to ground with 47k<br>12V Pin-out R1.0 |

## ▶ COM Express Pin Assignments

### Pin List for Pin-Out Type 10

The table below is a comprehensive list of all signal pins supported on the single 220-pin COM Express connectors as defined for Type 10 in the PICMG COM.0 R3.1 specification.

| Pin | Row A | "ASL9A2 Difference" | Row B | "ASL9A2 Difference" |
|---|---|---|---|---|
| 1 | GND (FIXED) | | GND (FIXED) | |
| 2 | GBE0_MDI3- | | GBE0_ACT# | |
| 3 | GBE0_MDI3+ | | LPC_FRAME# | |
| 4 | GBE0_LINKMID# | GBE1_LED1000# | LPC_AD0 | |
| 5 | GBE0_LINKMAX# | GBE1_LED2500# | LPC_AD1 | |
| 6 | GBE0_MDI2- | | LPC_AD2 | |
| 7 | GBE0_MDI2+ | | LPC_AD3 | |
| 8 | GBE0_LINK# | | LPC_DRQ0# | PU 10K to 3.3V |
| 9 | GBE0_MDI1- | | LPC_DRQ1# | PU 10K to 3.3V |
| 10 | GBE0_MDI1+ | | LPC_CLK | |
| 11 | GND (FIXED) | | GND (FIXED) | |
| 12 | GBE0_MDI0- | | PWRBTN# | |
| 13 | GBE0_MDI0+ | | SMB_CK | |
| 14 | GBE0_CTREF | NC | SMB_DAT | |
| 15 | SUS_S3# | | SMB_ALERT# | |
| 16 | SATA0_TX+ | | SATA1_TX+ | |
| 17 | SATA0_TX- | | SATA1_TX- | |
| 18 | SUS_S4# | | SUS_STAT# | NC |
| 19 | SATA0_RX+ | | SATA1_RX+ | |
| 20 | SATA0_RX- | | SATA1_RX- | |
| 21 | GND (FIXED) | | GND (FIXED) | |
| 22 | USB_SSRX0- | | USB_SSTX0- | |
| 23 | USB_SSRX0+ | | USB_SSTX0+ | |
| 24 | SUS_S5# | | PWR_OK | |
| 25 | USB_SSRX1- | | USB_SSTX1- | |
| 26 | USB_SSRX1+ | | USB_SSTX1+ | |
| 27 | BATLOW# | | WDT | |
| 28 | (S)ATA_ACT# | | HDA_SDN2 | |
| 29 | HDA_SYNC | | HDA_SDIN1 | |
| 30 | HDA_RST# | | HDA_SDIN0 | |
| 31 | GND (FIXED) | | GND (FIXED) | |
| 32 | HDA_BITCLK | | SPKR | |
| 33 | HDA_SDOUT | | I2C_CK | |
| 34 | BIOS_DIS0# | | I2C_DAT | |
| 35 | THRMTRIP# | | THRM# | |
| 36 | USB6- | | USB7- | |
| 37 | USB6+ | | USB7+ | |
| 38 | USB_6_7_OC# | | USB_4_5_OC# | |
| 39 | USB4- | | USB5- | |
| 40 | USB4+ | | USB5+ | |
| 41 | GND (FIXED) | | GND (FIXED) | |
| 42 | USB2- | | USB3- | |
| 43 | USB2+ | | USB3+ | |
| 44 | USB_2_3_OC# | | USB_0_1_OC# | |
| 45 | USB0- | | USB1- | |
| 46 | USB0+ | | USB1+ | |
| 47 | VCC_RTC | | ESPI_EN# | NC |
| 48 | RSVD | | USB0_HOST_PRSNT | NC |
| 49 | GBE0_SDP | | SYS_RESET# | |
| 50 | LPC_SERIRQ | | CB_RESET# | |
| 51 | GND (FIXED) | | GND (FIXED) | |
| 52 | RSVD | CLKOUT_PCIE2_P_BTB | RSVD | PCIE_CLK_REQ1_BTB# |
| 53 | RSVD | CLKOUT_PCIE2_N_BTB | RSVD | NC |
| 54 | GPI0 | | GPO1 | |
| 55 | GP_SPI_CS# | | GP_SPI_MISO | NC |
| 56 | GP_SPI_CK | | GP_SPI_MOSI | NC |

| Pin | Row A | "ASL9A2 Difference" | Row B | "ASL9A2 Difference" |
|---|---|---|---|---|
| 57 | GND | | GPO2 | |
| 58 | PCIE_TX3+ | | PCIE_RX3+ | |
| 59 | PCIE_TX3- | | PCIE_RX3- | |
| 60 | GND (FIXED) | | GND (FIXED) | |
| 61 | PCIE_TX2+ | | PCIE_RX2+ | |
| 62 | PCIE_TX2- | | PCIE_RX2- | |
| 63 | GPI1 | | GPO3 | |
| 64 | PCIE_TX1+ | | PCIE_RX1+ | |
| 65 | PCIE_TX1- | | PCIE_RX1- | |
| 66 | GND | | WAKE0# | |
| 67 | GPI2 | | WAKE1# | |
| 68 | PCIE_TX0+ | | PCIE_RX0+ | |
| 69 | PCIE_TX0- | | PCIE_RX0- | |
| 70 | GND (FIXED) | | GND (FIXED) | |
| 71 | LVDS_A0+/eDP_TX2+** | | DDI0_PAIR0+ | |
| 72 | LVDS_A0-/eDP_TX2-** | | DDI0_PAIR0- | |
| 73 | LVDS_A1+/eDP_TX1+** | | DDI0_PAIR1+ | |
| 74 | LVDS_A1-/eDP_TX1-** | | DDI0_PAIR1- | |
| 75 | LVDS_A2+/eDP_TX0+** | | DDI0_PAIR2+ | |
| 76 | LVDS_A2-/eDP_TX0-** | | DDI0_PAIR2- | |
| 77 | LVDS_VDD_EN/ eDP_VDD_EN** | | DDI0_PAIR4+ | NC |
| 78 | LVDS_A3+ | | DDI0_PAIR4- | NC |
| 79 | LVDS_A3- | | LVDS_BKLT_EN/ eDP_BKLT_EN** | |
| 80 | GND (FIXED) | | GND (FIXED) | |
| 81 | LVDS_A_CK+/ eDP_TX3+** | | DDI0_PAIR3+ | |
| 82 | LVDS_A_CK-/ eDP_TX3-** | | DDI0_PAIR3- | |
| 83 | LVDS_I2C_CK/ eDP_AUX+** | | LVDS_BKLT_TRL/ eDP_BKLT_CTRL** | |
| 84 | LVDS_I2C_DAT/ eDP_AUX-** | | VCC_5V_SBY | |
| 85 | GPI3 | | VCC_5V_SBY | |

| Pin | Row A | "ASL9A2 Difference" | Row B | "ASL9A2 Difference" |
|---|---|---|---|---|
| 86 | RSVD | | VCC_5V_SBY | |
| 87 | eDP_HPD** | | VCC_5V_SBY | |
| 88 | PCIE_CLK_REF+ | | BIOS_DIS1# | |
| 89 | PCIE_CLK_REF- | | DDI0_HPD | |
| 90 | GND(FIXED) | | GND(FIXED) | |
| 91 | SPI_POWER | | DDI0_PAIR5+ | NC |
| 92 | SPI_MISO | | DDI0_PAIR5- | NC |
| 93 | GPO0 | | DDI0_PAIR6+ | NC |
| 94 | SPI_CLK | | DDI0_PAIR6- | NC |
| 95 | SPI_MOSI | | DDI0_DDC_AUX_SEL | |
| 96 | TPM_PP | | USB7_HOST_PRSNT | NC |
| 97 | TYPE10# | | SPI_CS# | |
| 98 | SER0_TX | | DDI0_CTRLCLK_AUX+ | |
| 99 | SER0_RX | | DDI0_CTRLDATA_AUX- | |
| 100 | GND (FIXED) | | GND (FIXED) | |
| 101 | SER1_TX | | FAN_PWMOUT | |
| 102 | SER1_RX | | FAN_TACHIN | |
| 103 | LID# | | SLEEP# | |
| 104 | VCC_12V | | VCC_12V | |
| 105 | VCC_12V | | VCC_12V | |
| 106 | VCC_12V | | VCC_12V | |
| 107 | VCC_12V | | VCC_12V | |
| 108 | VCC_12V | | VCC_12V | |
| 109 | VCC_12V | | VCC_12V | |
| 110 | GND(FIXED) | | GND(FIXED) | |

**Note:**
1. ** eDP (in place of LVDS) is BOM option supported by project basis.
2. ASL9A2 (Mini module) allows wide range input voltage wtih 4.75V to 20V from VCC_12V power pins.
3. For PCIe device down components on the carrier board, please use and place on the PCIe Lane0 port first.

## ▶ Module Feature Fill Order

### Feature Fill Order

COM Express allows a variable number of ports to be implemented for several interfaces,

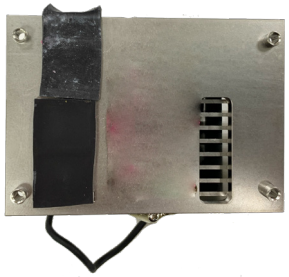
| Feature | Number of Ports | Fill Order |
|---|---|---|
| **LAN** | 1 | GbE channel 0 |
| **LVDS** | Single Channel | LVDS channel A |
| **SATA** | 2 | SATA channels 0,1 |
| **USB 2.0 Host** | 4 | USB channels 0,1,2,3 |
| | 5 | USB channels 0,1,2,3,4 |
| | 6 | USB channels 0,1,2,3,4,5 |
| | 7 | USB channels 0,1,2,3,4,5,6 |
| | 8 | USB channels 0,1,2,3,4,5,6,7 |
| **USB 2.0 Client** | 1 | USB Channel 7 only<br>(Option for static changing, select the USB2.0 port client port in the BIOS setup and reset the BIOS) |
| **USB 3.0 SuperSpeed²** | 1 | USB channel 0 |
| | 2 | USB channels 0,1 |
| **DDI** | 1 | DDI 1 |

## ▶ Cooling Option

### Heat Sink

The COM Express connector is used to interface the ASL9A2 COM Express board to a carrier board. Connect the COM Express connector (located on the solder side of the board) to the COM Express connector on the carrier board.

Top View of the Heat Sink



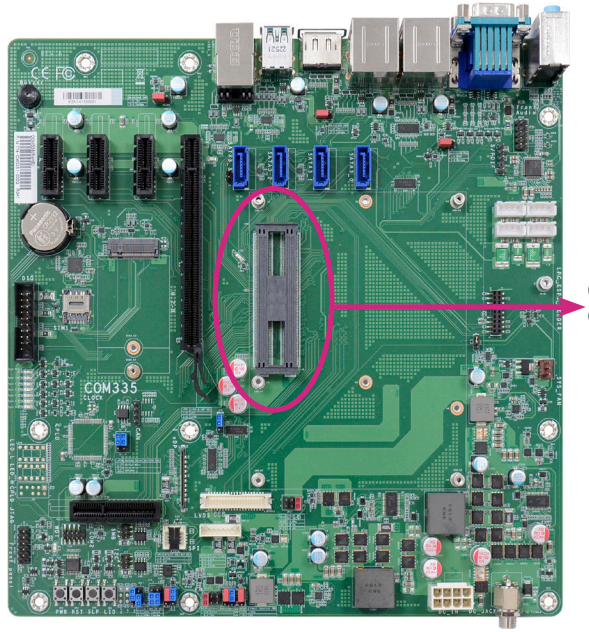
Bottom View of the Heat Sink

**Important:**
Remove the plastic covering from the thermal pads prior to mounting the heat sink onto board.

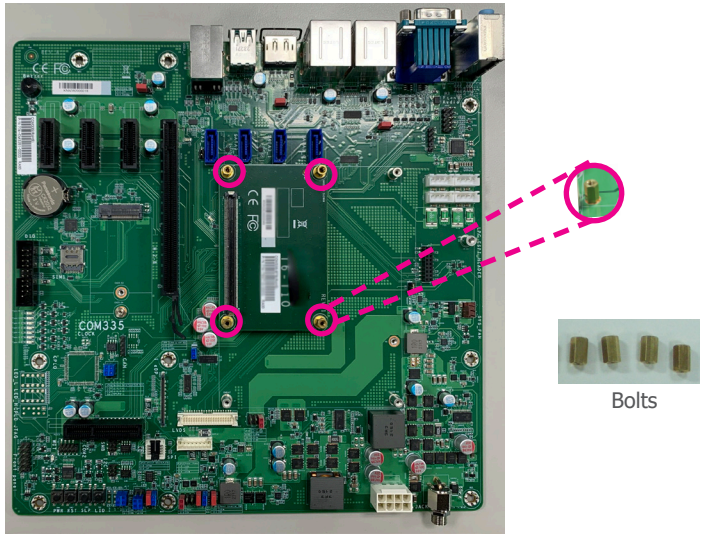
## ▶ Installing ASL9A2 onto a Carrier Board

**Important:**
The carrier board (COM335) used in this section is for reference purpose only and may not resemble your carrier board. These illustrations are mainly to guide you on how to install ASL9A2 onto the carrier board of your choice.

1. Grasp T6 transfer T10 card by its edges and position it on top of the carrier board with its COM Express connector aligned with the COM Express connector on the carrier board. This will also help align the mountings holes of T6 transfer T10 card with the standoffs on the carrier board.



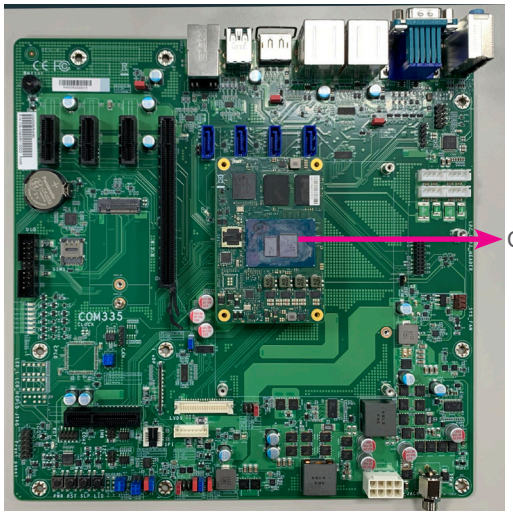
2. Fasten bolts with mounting screws through mounting holes to be fixed in place.



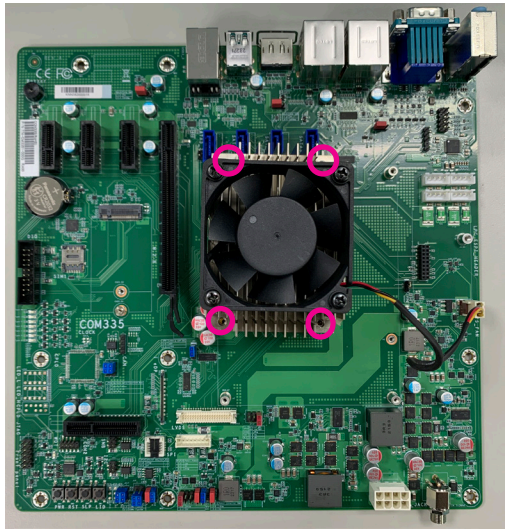


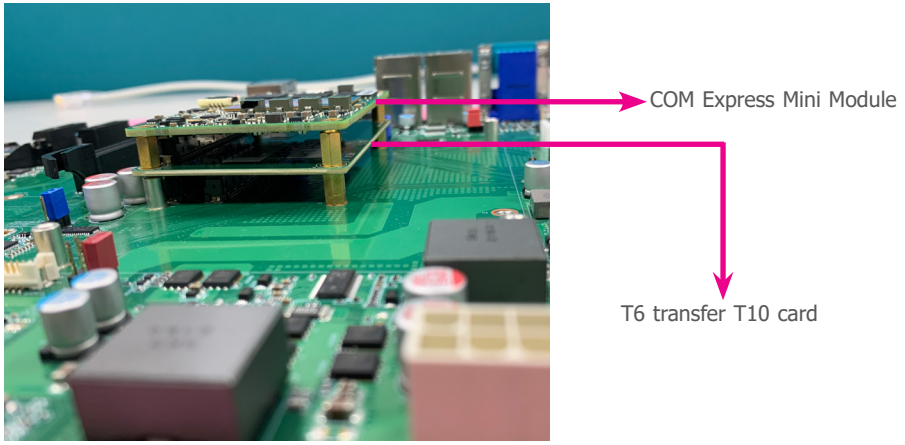

Bolts

3. Apply firm even pressure to the side with the COM Express connector first and push down the entire module. Be careful when pressing the module to avoid damaging it. You will hear a distinctive “click”, indicating the module is correctly locked into position.




4. Align the mounting holes of the heatsink with the mounting holes of the module. Use the provided mounting screws to install the heat sink onto the module.



# Chapter 4 - BIOS Setup

## Overview

The BIOS is a program that takes care of the basic level of communication between the CPU and peripherals. It contains codes for various advanced features found in this system board. The BIOS allows you to configure the system and save the configuration in a battery-backed CMOS so that the data retains even when the power is off. In general, the information stored in the CMOS RAM of the EEPROM will stay unchanged unless a configuration change has been made such as a hard drive replaced or a device added.

It is possible that the CMOS battery will fail causing CMOS data loss. If this happens, you need to install a new CMOS battery and reconfigure the BIOS settings.

**Note:**
The BIOS is constantly updated to improve the performance of the system board; therefore the BIOS screens in this chapter may not appear the same as the actual one. These screens are for reference purpose only.

## Default Configuration

Most of the configuration settings are either predefined according to the Load Optimal Defaults settings which are stored in the BIOS or are automatically detected and configured without requiring any actions. There are a few settings that you may need to change depending on your system configuration.

## Entering the BIOS Setup Utility

The BIOS Setup Utility can only be operated from the keyboard and all commands are keyboard commands. The commands are available at the right side of each setup screen.
The BIOS Setup Utility does not require an operating system to run. After you power up the system, the BIOS message appears on the screen and the memory count begins. After the memory test, the message “Press DEL to run setup” will appear on the screen. If the message disappears before you respond, restart the system or press the “Reset” button. You may also restart the system by pressing the <Ctrl> <Alt> and <Del> keys simultaneously.

## Legends

| KEYs | Function |
|---|---|
| Right and Left Arrows | Moves the highlight left or right to select a menu. |
| Up and Down Arrows | Moves the highlight up or down between submenus or fields. |
| <Esc> | Exits to the BIOS setup utility |
| + (plus key) | Scrolls forward through the values or options of the hightlighted field. |
| - (minus key) | Scolls backward through the values or options of the hightlighted field. |
| <F1> | Displays general help |
| <F2> | Displays previous values |
| <F9> | Optimized defaults |
| <F10> | Saves and reset the setup program. |
| <Enter> | Press <Enter> to enter the highlighted submenu |

## Scroll Bar

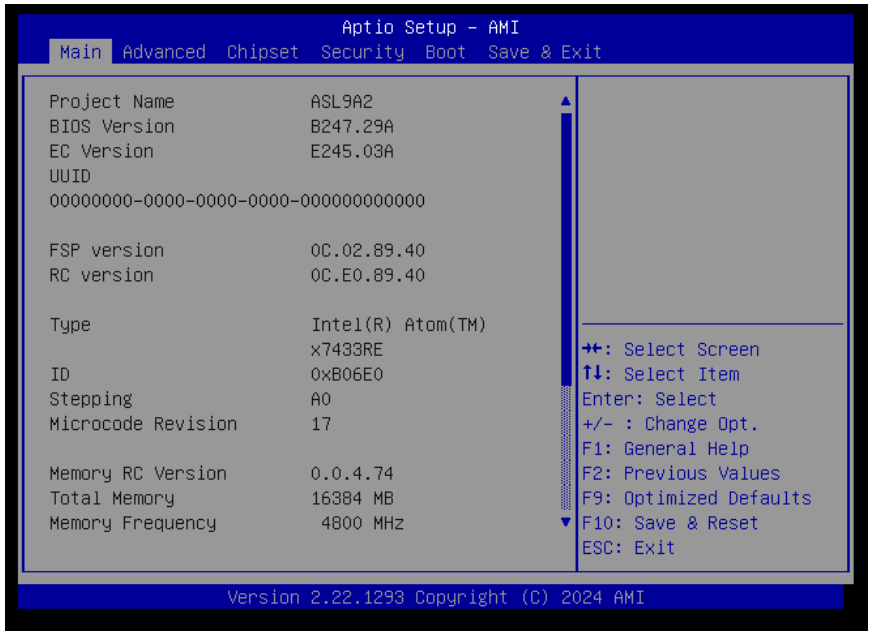
When a scroll bar appears to the right of the setup screen, it indicates that there are more available fields not shown on the screen. Use the up and down arrow keys to scroll through all the available fields.

## Submenu

When “▶” appears on the left of a particular field, it indicates that a submenu which contains additional options are available for that field. To display the submenu, move the highlight to that field and press <Enter>.

## ▶ Main

The Main menu is the first screen that you will see when you enter the BIOS Setup Utility.




### System Date

The date format is <month>, <date>, <year>. Press "Tab" to switch to the next field and press "-" or "+" to modify the value.

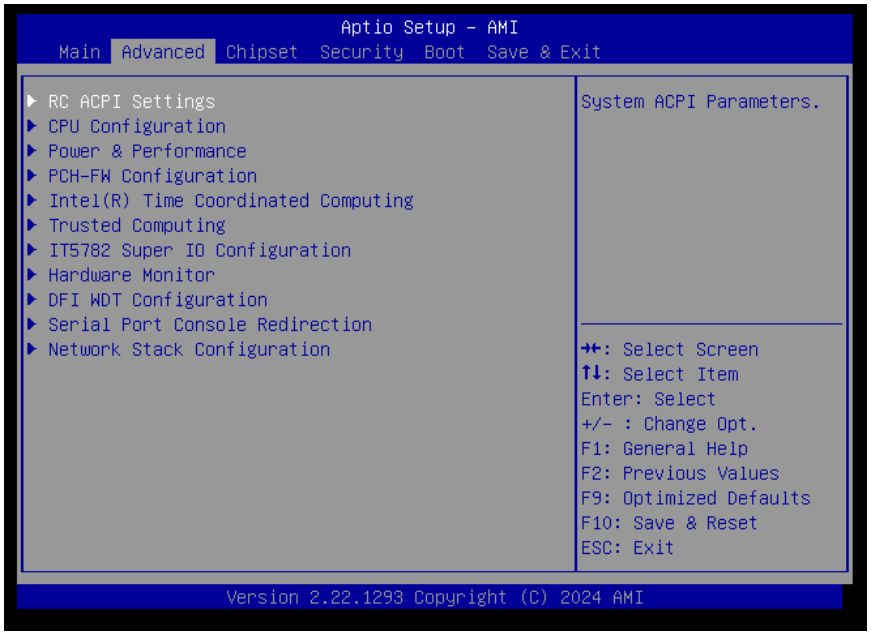
### System Time

The time format is <hour>, <minute>, <second>. The time is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Hour displays hours from 00 to 23. Minute displays minutes from 00 to 59. Second displays seconds from 00 to 59.

## ▶ Advanced

The Advanced menu allows you to configure your system for basic operation. Some entries are defaults required by the system board, while others, if enabled, will improve the performance of your system or let you set some features according to your preference.

**Important:**
Setting incorrect field values may cause the system to malfunction.



▶ Advanced

## RC ACPI Configuration

### Wake system from S5 via RTC

When Enabled, the system will automatically power up at a designated time every day. Once it's switched to [Enabled], please set up the time of day — hour, minute, and second — for the system to wake up.

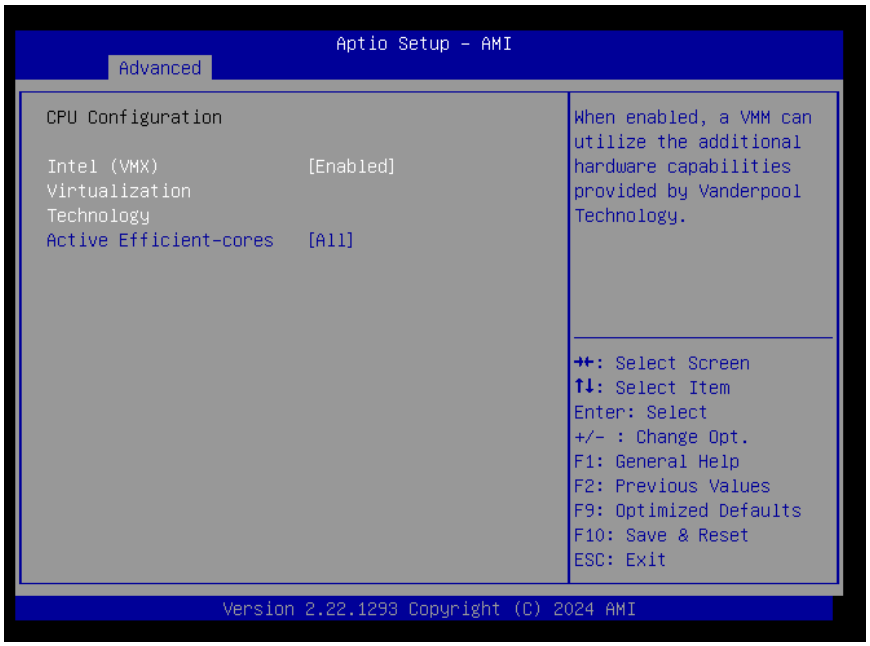
### State After G3

Select between S0 State, and S5 State. This field is used to specify what state the system is set to return to when power is re-applied after a power failure (G3 state).

- **S0 State** The system automatically powers on after power failure.
- **S5 State** The system enter soft-off state after power failure. Power-on signal input is required to power up the system.
- **Last State** The system returns to the last state right before power failure.

▶ Advanced

## CPU Configuration




### Intel (VMX) Virtualization Technology

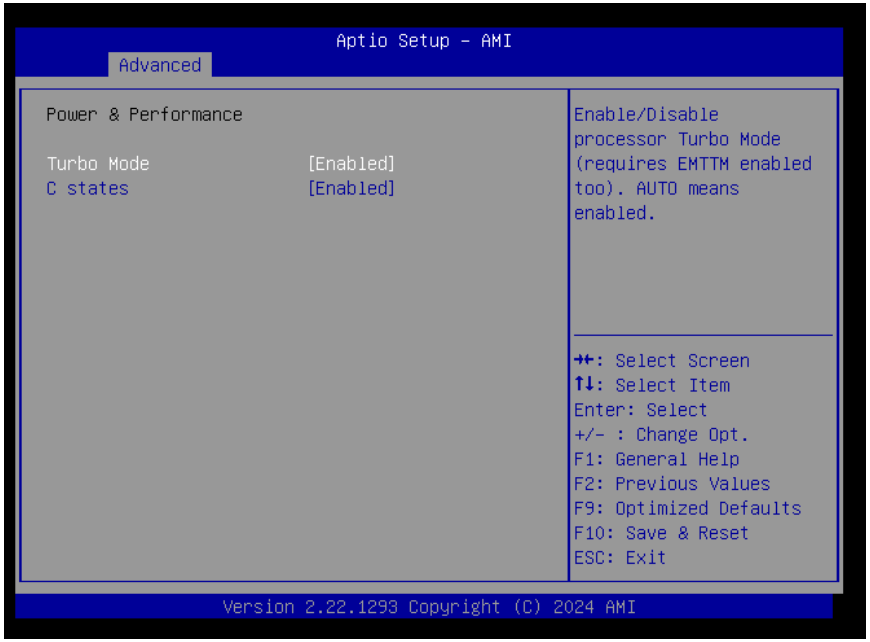
When this field is set to Enabled, the VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

### Active Processor Cores

Select number of cores to enable in each processor package.

▶ Advanced

## Power & Performance




### Turbo Mode

Enable or disable turbo mode of the processor.
This field will only be displayed when EIST is enabled.

### C states

Enable or disable CPU Power Management. It allows CPU to enter "C states" when it's idle and nothing is executing.

▶ Advanced

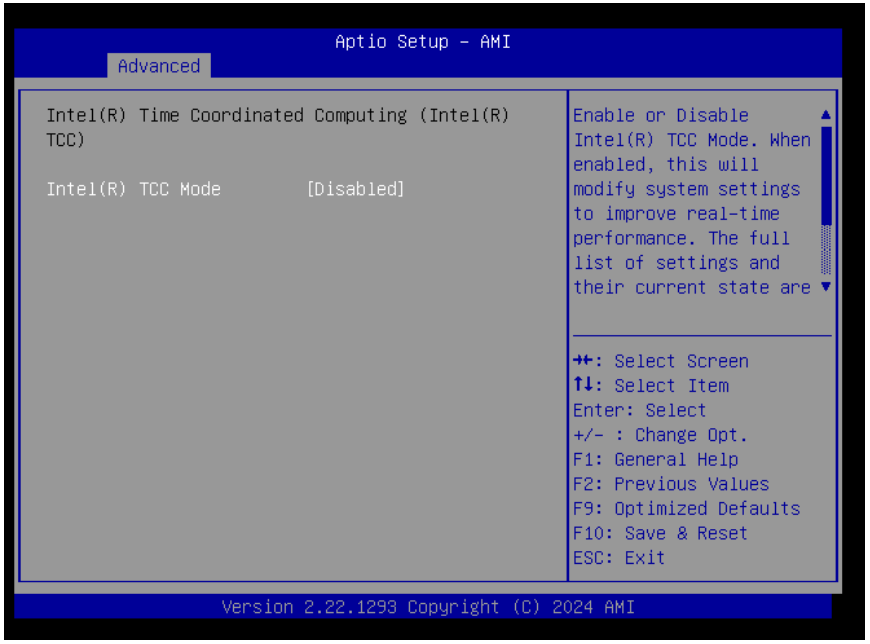
## PCH-FW Configuration

### ME FW Image Re-Flash

Enable / Disable Me FW Image Re-Flash function.

▶ Advanced

## Intel(R) Time Coordinated Computing




Enable or Disable Intel(R) TCC Mode. When enbaled, this will modify system settings to improve real-time performance.

▶ Advanced

## Trusted Computing

**Security Device Support**

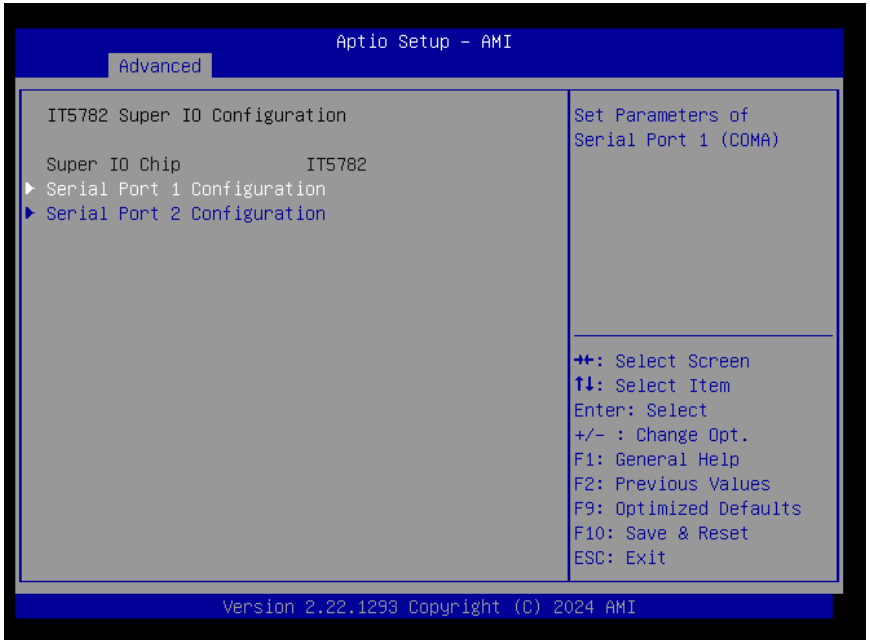
This field is used to enable or disable BIOS support for the security device such as an TPM 2.0 to achieve hardware-level security via cryptographic keys.

**Pending operation**

To clear the existing TPM encryption, select "TPM Clear" and restart the system. This field is not available when "Security Device Support" is disabled.

▶ Advanced

## IT5782 Super IO Configuration




**Serial Port Configuration**
Set Parameters of Serial Ports. See next page.

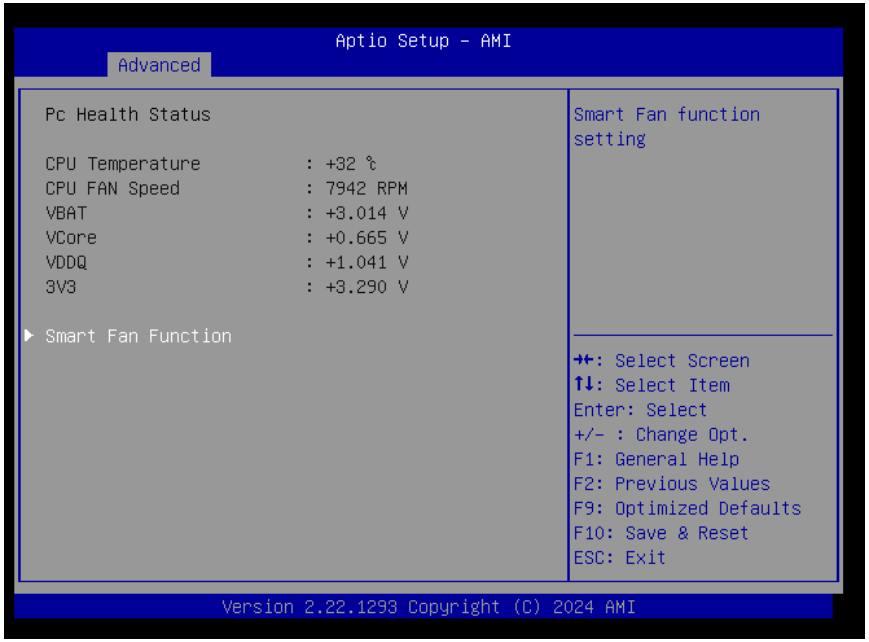
▶ Advanced

## IT5782 Super IO Configuration ▶ Serial Port 1, 2 Configuration

**Serial Port**
Enable or disable serial port.

▶ Advanced

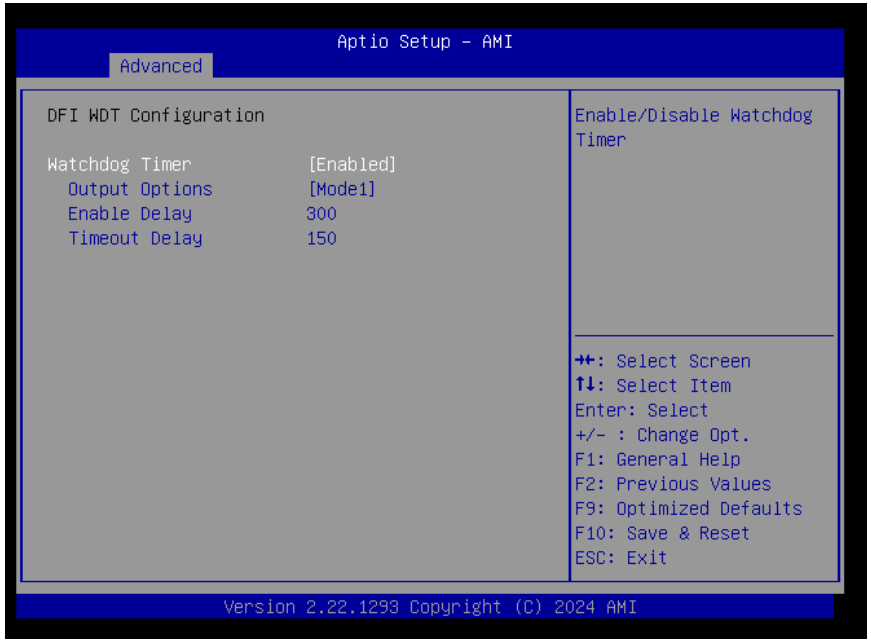
## Hardware Monitor




Lists voltage, termperature, and fan speed.

▶ Advanced

## DFI WDT Configuration




**Watchdog Timer**

Enable or disable watchdog timer.

**Output Options**

Mode1 = A Watchdog timeout causes the system to be reset.
Mode2 = WDT pin goes high upon timeout of the watchdog timer.
Mode3 = Generate NMI upon timeout of the watchdog timer.

**Enable Delay**

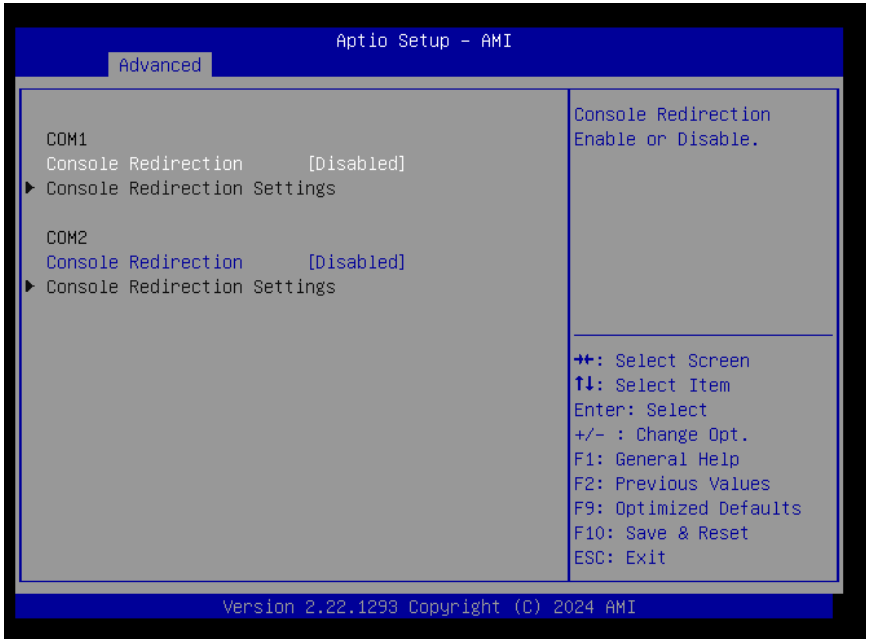
The enable delay allows time for the OS to boot and the application to load and initialize. The unit is 1 sec.

**Timeout Delay**

The timeout delay allows time for period of the watchdog timer. The unit is 0.1 sec.

▶ Advanced

## Serial Port Console Redirection

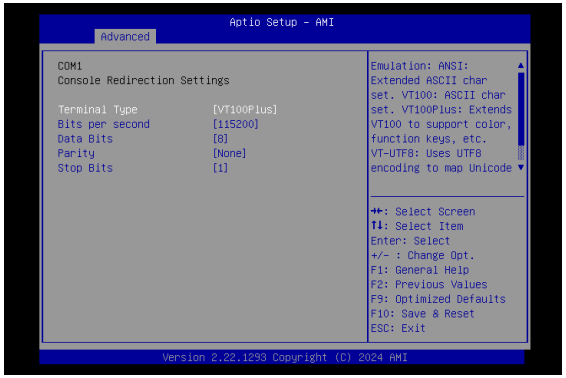



**Console Redirection**
Console Redirection Enable or Disable.

**Console Redirection Settings**
See following pages.

▶ Advanced

## Serial Port Console Redirection ▶ Console Redirection Settings



Configure the serial settings of the current COM port.

**Terminal Type**
Select terminal type: VT100, VT100+, VT-UTF8 or ANSI.

**Bits per second**
Select serial port transmission speed: 9600, 19200, 38400, 57600 or 115200.

**Data Bits**
Select data bits: 7 bits or 8 bits.

**Parity**
Select parity bits: None, Even, Odd, Mark or Space.

**Stop Bits**
Select stop bits: 1 bit or 2 bits.

▶ Advanced

## Network Stack Configuration

**Network Stack**

Enable or disable (Default) UEFI network stack. The following fields will appear when this field is enabled.

**Ipv4 PXE Support** Enable or disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.

**Ipv6 PXE Support**

Enable or disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.

**PXE boot wait time**

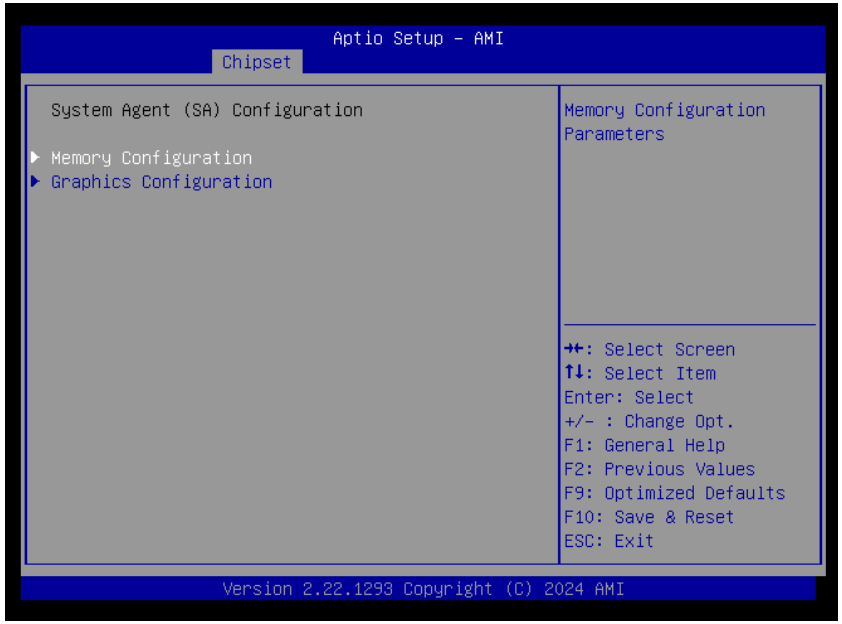
Set the wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.

**Media detect count**

Set the number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.

## ▶ Chipset

### System Agent (SA) Configuration



## System Agent (SA) Configuration ▶ Memory Configuration

### In-Band ECC

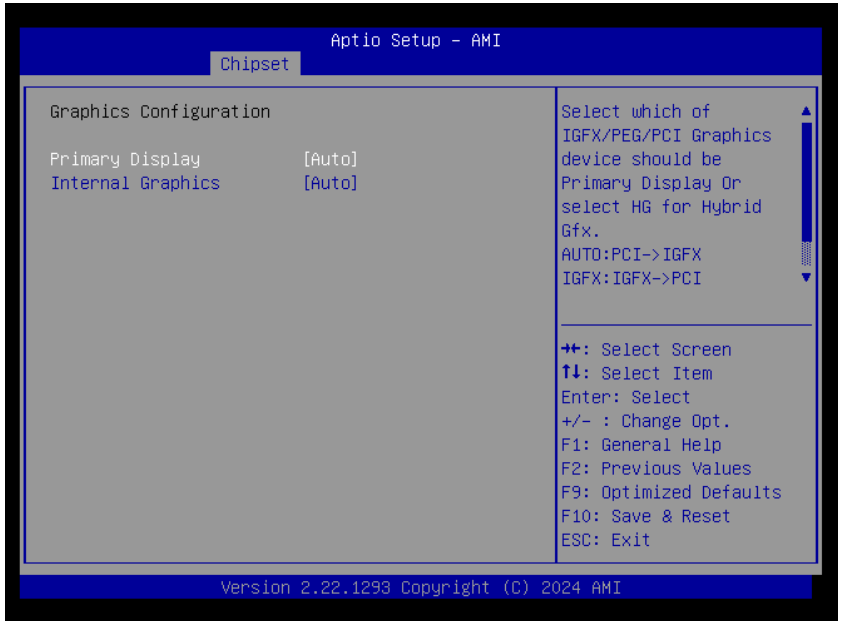
Enable/Disable (Default) In-Band ECC

### In-Band ECC Operation Mode

0: Functional Mode protects requests based on the address range,
1: Makes all requests non protected and ignore range checks,
2: Makes all requests protected and ignore range checks.



## System Agent (SA) Configuration ▶ Graphics Configuration




### Primary Display

Select which of IGFX/PCI Graphics device to be the primary display.

### Internal Graphics

Keep IGFX "Enabled" or "Disabled" based on the setup options, or select "Auto" for auto-detection.

▶ Chipset

## PCH-IO Configuration

Select one of the PCI Express channels and press enter to configure the following settings.

**PCI Express Configuration**

PCI Express Configuration Settings

**SATA And RST Configuration**

SATA Device Otpions Settings

**HD Audio Configuration**

HD Audio Subsystem Configuration Settings

**SMBus Source**

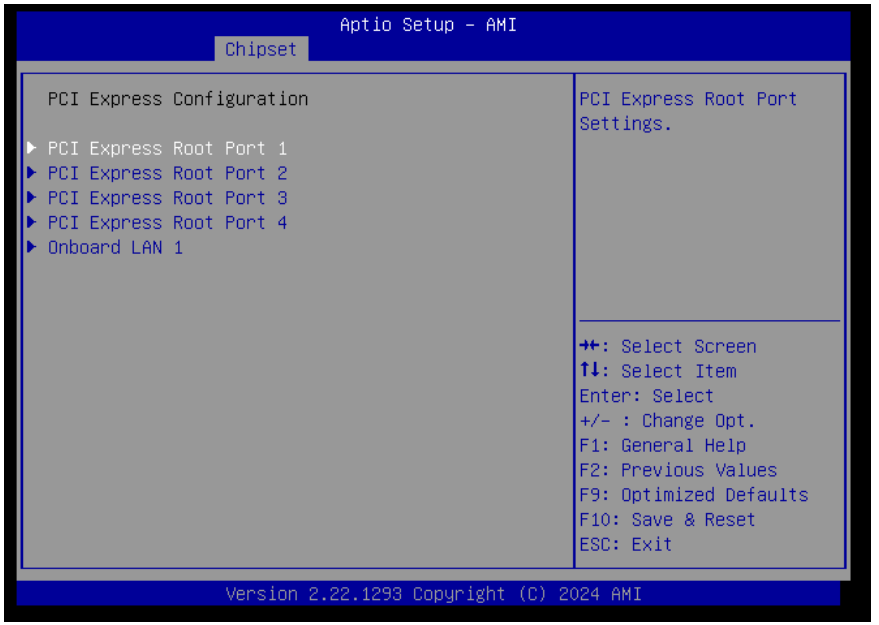
Choose where SMBus comes from.

**I2C Bus Source**

Choose where I2C Bus comes from.

▶ Chipset

## PCH-IO Configuration ▶ PCI Express Configuration




Select one of the PCI Express channels and press enter to configure the following settings.

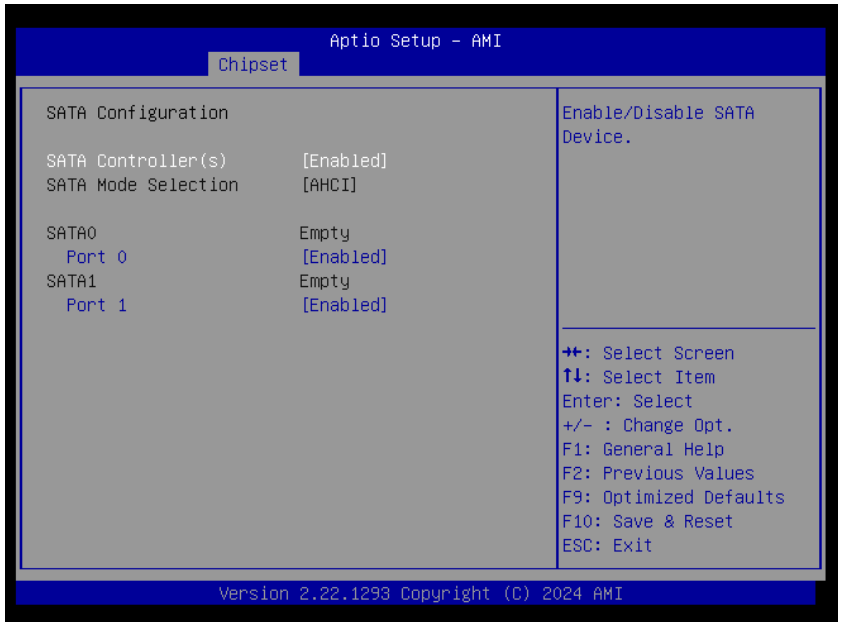
**PCIe Express Root Port 1,2,3,4**

Control the PCI Express Root Port.

**Onboard LAN1**

Control the PCI Express Root Port.

## PCH-IO Configuration ▶ SATA Configuration




### SATA Controller(s)

This field is used to enable or disable the Serial ATA controller.

### SATA Mode Selection

The mode selection determines how the SATA controller(s) operates.

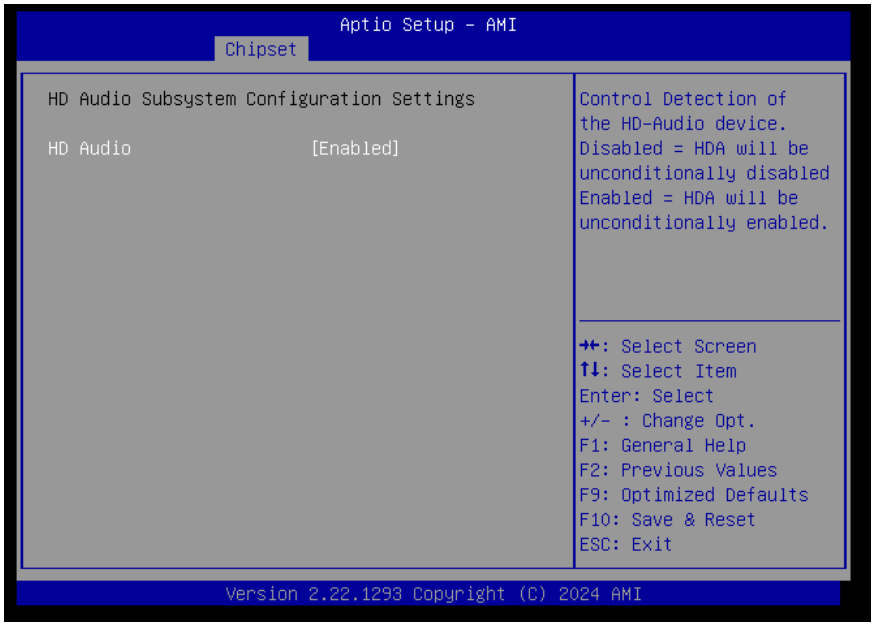
- **AHCI** This option allows the Serial ATA controller(s) to use AHCI (Advanced Host Controller Interface).

### Ports

Enable or disable the Serial ATA ports.



## PCH-IO Configuration ▶ HD Audio Configuration

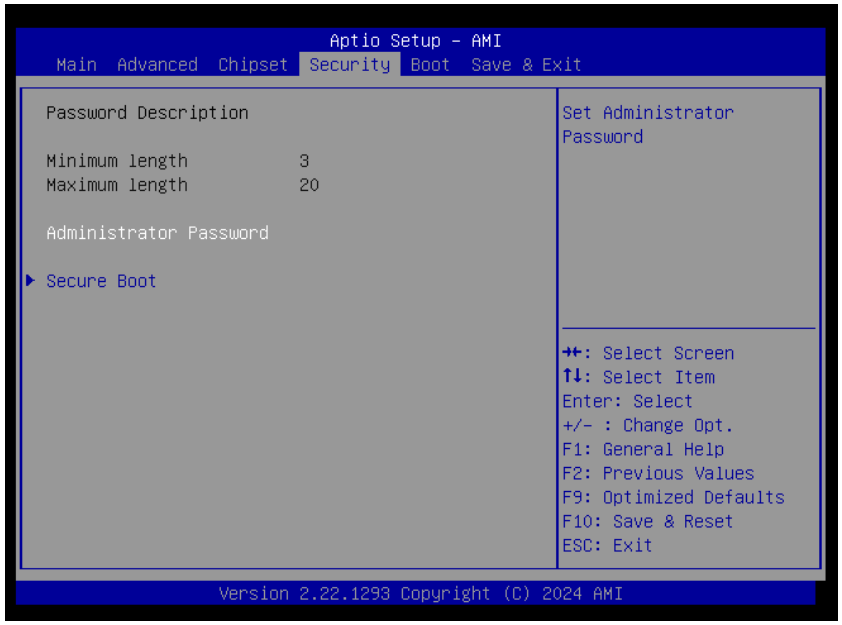



### HD Audio

Control the detection of the HD Audio device.

- **Disabled** HDA will be unconditionally disabled.
- **Enabled** HDA will be unconditionally enabled.

## ▶ Security

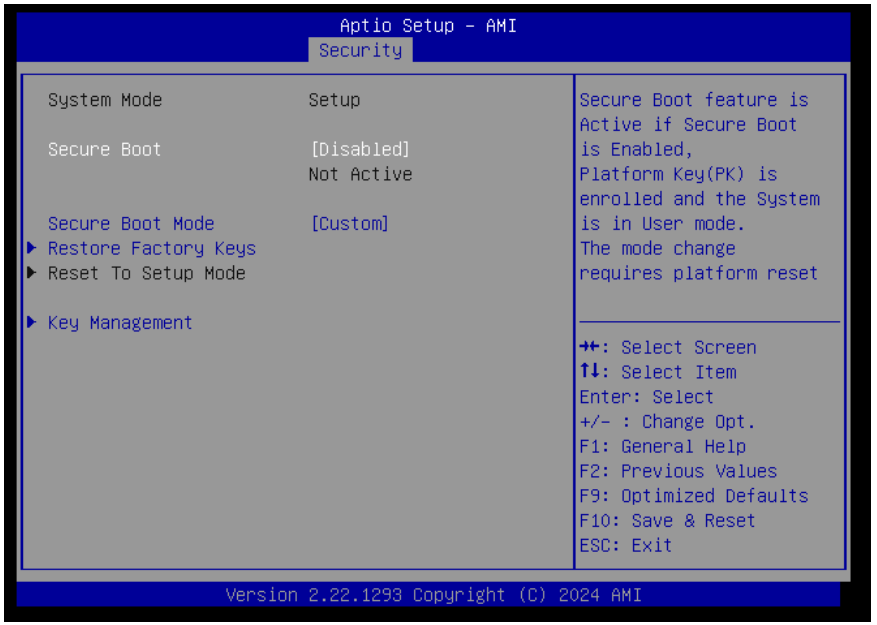



### Administrator Password

Set the administrator password. To clear the password, input nothing and press enter when a new password is asked. Administrator Password will be required when entering the BIOS.



## Secure Boot




### Secure Boot

Secure Boot feature is Active if secure Boot is Enabled, Platform Key (PK) is enrolled and the system is in user mode. The mode change requires platform reset.

### Secure Boot Mode

Select the secure boot mode — Standard or Custom. When set to Custom, the following fields will be configurable for the user to manually modify the key database.

### Restore Factory Keys

Force system to User Mode. Load OEM-defined factory defaults of keys and databases onto the Secure Boot. Press Enter and a prompt will show up for you to confirm.

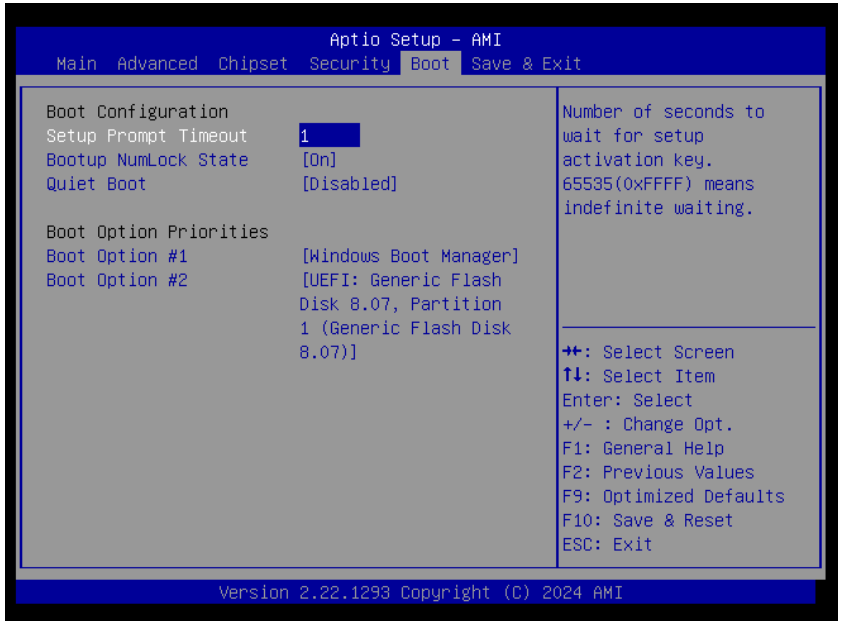
### Reset To Setup Mode

Clear the database from the NVRAM, including all the keys and signatures installed in the Key Management menu. Press Enter and a prompt will show up for you to confirm.

### Key Management

Enables expert users to modify Secure Boot Policy variables without full authentication.

## ▶ Boot




### Setup Prompt Timeout

Set the number of seconds to wait for the setup activation key. 65535 (0xFFFF) denotes indefinite waiting.

### Bootup NumLock State

Select the keyboard NumLock state: On or Off.

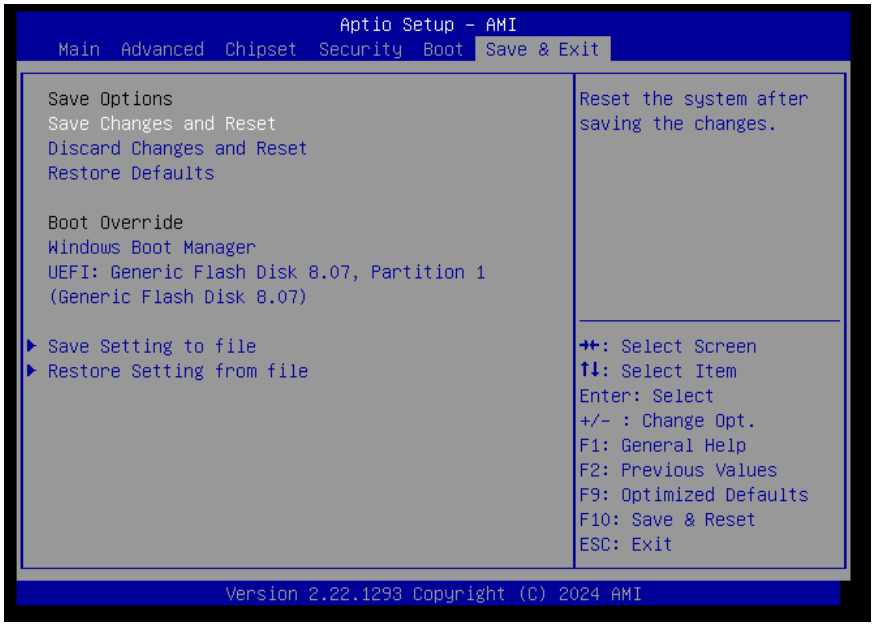
### Quiet Boot

This section is used to enable or disable quiet boot option.

### Boot Option Priorities

Rearrange the system boot order of available boot devices.

## ▶ Save & Exit




### Save Changes and Reset

To save the changes, select this field and then press <Enter>. A dialog box will appear. Select Yes to reset the system after saving all changes made.

### Discard Changes and Reset

To discard the changes, select this field and then press <Enter>. A dialog box will appear. Select Yes to reset the system setup without saving any changes.

### Restore Defaults

To restore and load the optimized default values, select this field and then press <Enter>. A dialog box will appear. Select Yes to restore the default values of all the setup options.

### Boot Override

Move the cursor to an available boot device and press Enter, and then the system will immediately boot from the selected boot device. The Boot Override function will only be effective for the current boot. The “Boot Option Priorities” configured in the Boot menu will not be changed.

### ► Save Setting to file

Select this option to save BIOS configuration settings to a USB flash device.

### ► Restore Setting from file

This field will appear only when a USB flash device is detected. Select this field to restore setting from the USB flash device.

## ▶ Updating the BIOS

To update the BIOS, you will need the new BIOS file and a flash utility. Please contact technical support or your sales representative for the files and specific instructions about how to update BIOS with the flash utility.

## ▶ Notice: BIOS SPI ROM

- 1. The Intel® Management Engine has already been integrated into this system board. Due to the safety concerns, the BIOS (SPI ROM) chip cannot be removed from this system board and used on another system board of the same model.
- 2. The BIOS (SPI ROM) on this system board must be the original equipment from the factory and cannot be used to replace one which has been utilized on other system boards.
- 3. If you do not follow the methods above, the Intel® Management Engine will not be updated and will cease to be effective.

**Note:**

a. You can take advantage of flash tools to update the default configuration of the BIOS (SPI ROM) to the latest version anytime.

b. When the BIOS IC needs to be replaced, you have to populate it properly onto the system board after the EEPROM programmer has been burned and follow the technical person's instructions to confirm that the MAC address should be burned or not.

c. After updating unique MAC Address from manufacturing, NVM will be protected immediately after power cycle.
Users cannot update NVM or MAC address.