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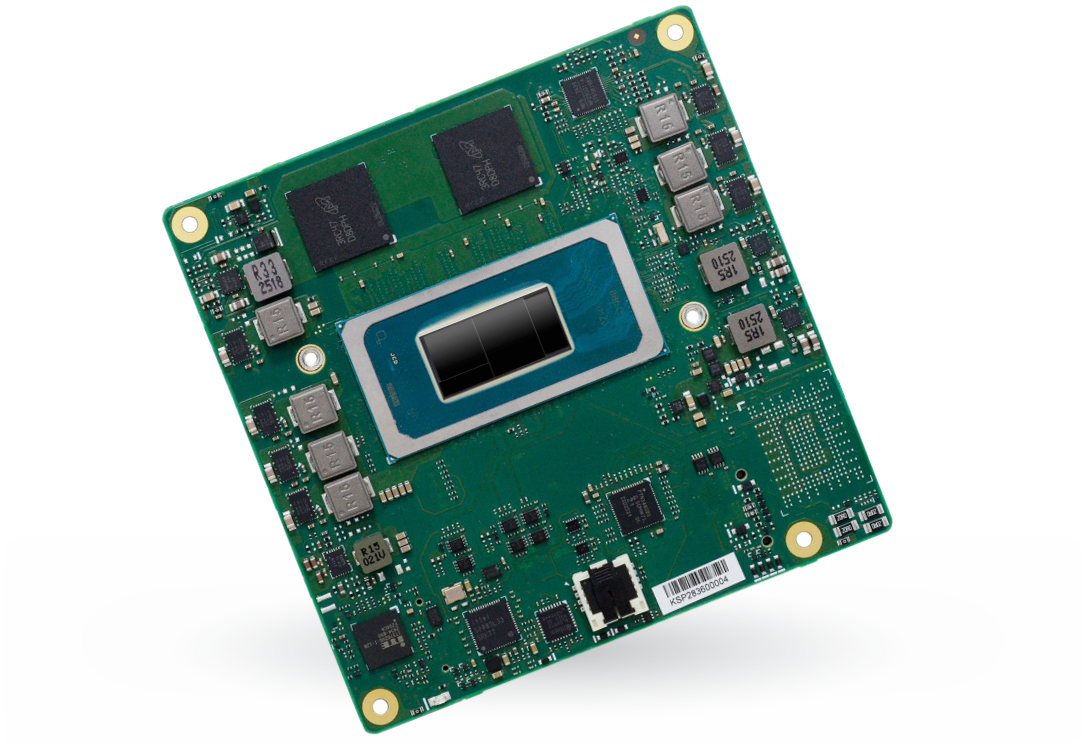

MTH966

COM Express Compact Module
User's Manual

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Changes after the publication's first release will be based on the product's revision. The website will always provide the most updated information.

Trademarks

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COM Express Specification Reference

PICMG® COM Express® Module Base Specification.
http://www.picmg.org/

FCC and DOC Statement on Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio TV technician for help.

Notice:

- The changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.
- Shielded interface cables must be used in order to comply with the emission limits.

Table of Contents

About this Manual

This manual can be downloaded from the website.

The manual is subject to change and update without notice, and may be based on editions that do not resemble your actual products. Please visit our website or contact our sales representatives for the latest editions.

Warranty

- Warranty does not cover damages or failures that occur from misuse of the product, inability to use the product, unauthorized replacement or alteration of components and product specifications.
- The warranty is void if the product has been subjected to physical abuse, improper installation, modification, accidents or unauthorized repair of the product.
- Unless otherwise instructed in this user's manual, the user may not, under any circumstances, attempt to perform service, adjustments or repairs on the product, whether in or out of warranty. It must be returned to the purchase point, factory or authorized service agency for all such work.
- We will not be liable for any indirect, special, incidental or consequential damages to the product that has been modified or altered.

Static Electricity Precautions

It is quite easy to inadvertently damage your PC, system board, components or devices even before installing them in your system unit. Static electrical discharge can damage computer components without causing any signs of physical damage. You must take extra care in handling them to ensure against electrostatic build-up.

- To prevent electrostatic build-up, leave the system board in its anti-static bag until you are ready to install it.
- Wear an antistatic wrist strap.
- Do all preparation work on a static-free surface.
- Hold the device only by its edges. Be careful not to touch any of the components, contacts or connections.
- Avoid touching the pins or contacts on all modules and connectors. Hold modules or connectors by their ends.

Important:
Electrostatic discharge (ESD) can damage your processor, disk drive and other components. Perform the upgrade instruction procedures described at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

Safety Measures

- To avoid damage to the system, use the correct AC input voltage range.
- To reduce the risk of electric shock, unplug the power cord before removing the system chassis cover for installation or servicing. After installation or servicing, cover the system chassis before plugging the power cord.

About the Package

The package contains the following items. If any of these items are missing or damaged, please contact your dealer or sales representative for assistance.

- 1 MTH966 board
- 1 Cooler

Optional Items

The board and accessories in the package may not come similar to the information listed above. This may differ in accordance with the sales region or models in which it was sold. For more information about the standard package in your region, please contact your dealer or sales representative.

Before Using the System Board

Before using the system board, prepare basic system components.
If you are installing the system board in a new system, you will need at least the following internal components.

- Storage devices such as hard disk drive, etc.

You will also need external system peripherals you intend to use which will normally include at least a keyboard, a mouse and a video display monitor.

Chapter 1 - Introduction

▶ Specifications

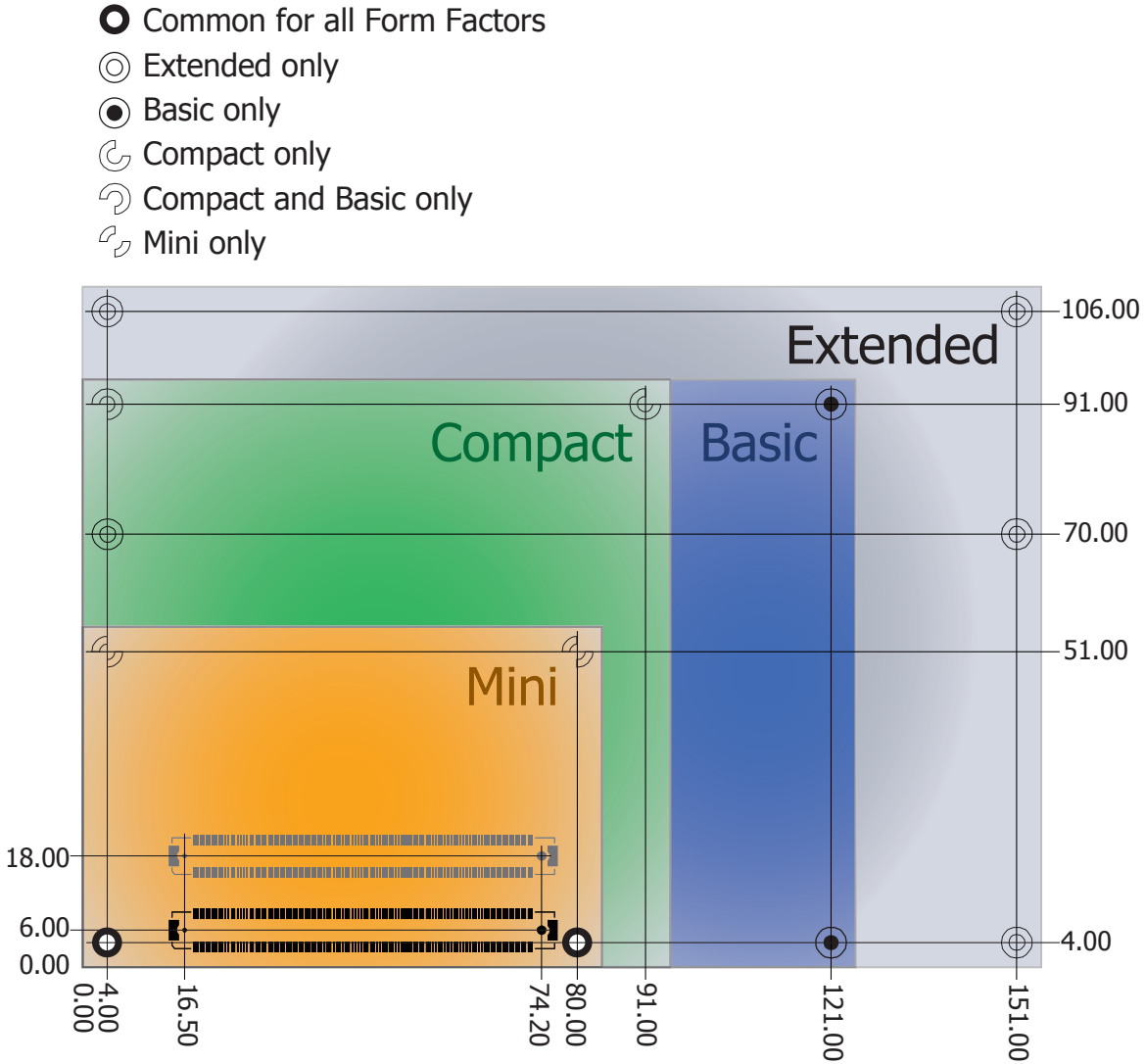
SYSTEM	Processor	Intel® Core™ Ultra Processor (Meteor Lake: U/H-series) Intel® Core™ Ultra 7 155H (6 P-Cores x 1.4 GHz, 8 E-Cores x 0.9 GHz, 24 MB cache, 28W) Intel® Core™ Ultra 5 125H (4 P-Cores x 1.2 GHz, 8 E-Cores x 0.7 GHz, 18 MB cache, 28W) Intel® Core™ Ultra 7 155U (2 P-Cores x 1.7 GHz, 8 E-Cores x 1.2 GHz, 12 MB cache, 15W) Intel® Core™ Ultra 5 125U (2 P-Cores x 1.3 GHz, 8 E-Cores x 0.8 GHz, 12 MB cache, 15W)
	Memory	Dual Channel LPDDR5 memory down up to 32GByte
	BIOS	AMI BIOS
GRAPHICS	Controller	155H/125H : Intel® Arc™ Graphics 125U/155U : Intel® Graphics
	Feature	DX12, Open GL 4.6, Vulkan 1.2 (Windows) Mesa 3D, Open GL 4.6, Vulkan 1.2 (Linux) HW Decode : 4K60 8b 4:2:0 AVC HW Encode : 4K60 10b 4:4:4 HEVC/VP9/SCC 4K60 8b 4:2:0 AVC
	Display	1 x LVDS/eDP (eDP available upon request) 3 x DDI (2 DDI option with USB4) LVDS: dual channel 24-bit, resolution up to 1920x1200 @ 60Hz eDP: resolution up to 4096x2304 @ 60Hz HDMI: resolution up to 4096x2160 @ 30Hz DP++: resolution up to 4096x2304 @ 60Hz
	Multiple Displays	LVDS + 3 DDI
EXPANSION	Interface	8 x PCIe x1 (Gen4, Lanes 6/7 by option) 1 x PCIe x8 (Gen 5, H-Line only) 2 x PCIe x4 (Gen4, PEG_LANE4-7 option with NVMe SSD) 1 x I2C 1 x SMBUS 1 x LPC/eSPI 2 x UART
AUDIO	Interface	HD Audio
ETHERNET	Controller	1 x Intel® I226 series (10/100/1000Mbps/2.5G)
I/O	USB	2 x USB 4.0 (BOM option with DDI) 4 x USB 3.2 Gen 2 8 x USB 2.0
	SATA	2 x SATA 3.0 (up to 6Gb/s), co-lay 2 PCIe x1 (available upon request)
	NVMe SSD	1 x 128GB/256GB/512GB/1024GB on board SSD (available upon request)
	DIO	1 x 8-bit DIO
WATCHDOG TIMER	Output & Interval	System Reset, Programmable via Software from 1 to 255 Seconds
SECURITY	TPM	Available Upon Request

Power	Type	8.5~20V, 5VSB, VCC_RTC (ATX mode) 8.5~20V, VCC_RTC (AT mode)
	Consumption	TBD
OS SUPPORT	Microsoft	Windows 10 IoT Enterprise 64-bit Windows 11
	Linux	Linux
ENVIRONMENT	Temperature	Operating: 0°C~60°C (For H-Series Processor) -40°C~85°C (For U-Series Processor) Storage: -40°C~85°C
	Humidity	Operating: 10 to 90% RH Storage: 10%~90% RH
	MTBF	TBD
MECHANICAL	Dimensions	COM Express® Compact 95mm (3.74") x 95mm (3.74")
	Compliance	PICMG COM Express® R3.1, Type 6
STANDARDS AND CERTIFICATIONS	Certification	CE, FCC, RoHS

Chapter 2 - Concept

▶ COM Express Module Standards

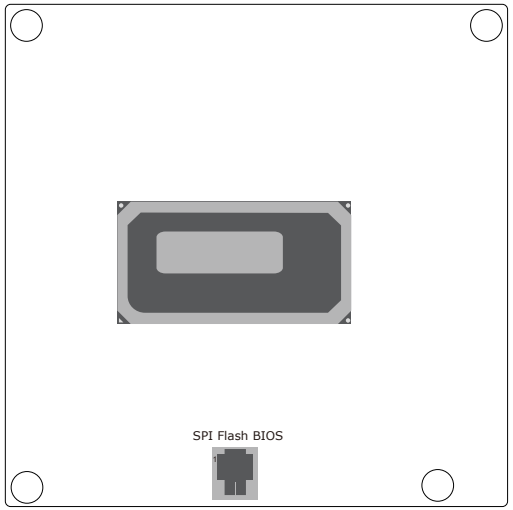
The figure below shows the dimensions of the different types of COM Express modules.
MTH966 is a COM Express Compact. The dimension is 95mm x 95mm.



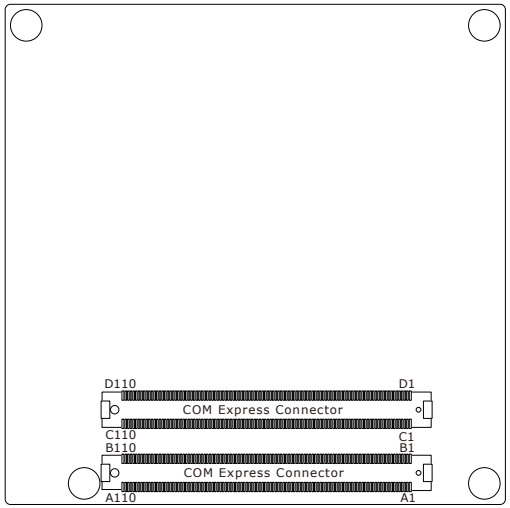
Chapter 3 - Hardware Installation

▶ Board Layout

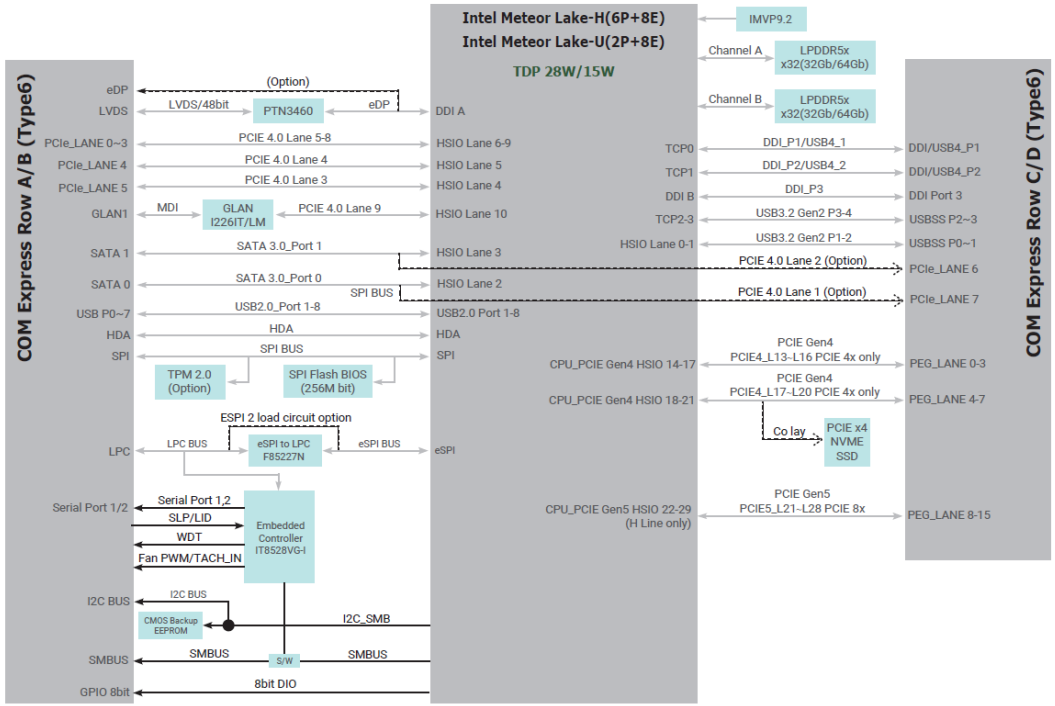
TOP



BOTTOM



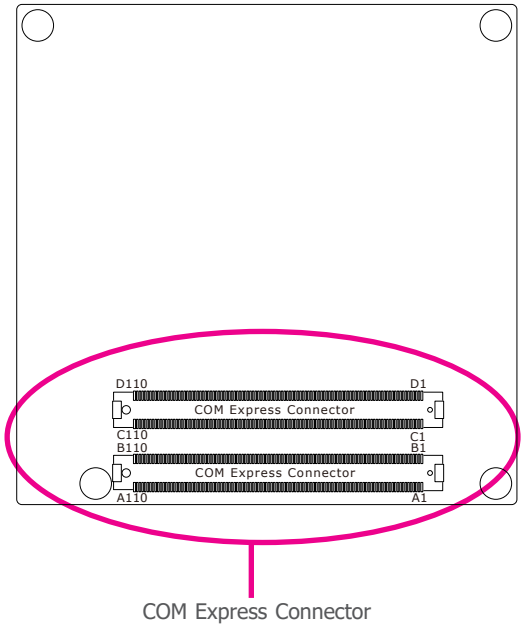
▶ Block Diagram



▶ Connector

COM Express Connector

The COM Express connector is used to interface the MTH966 COM Express board to a carrier board. Connect the COM Express connector (located on the solder side of the board) to the COM Express connector on the carrier board.



Refer to the following pages for the pin functions of the connector.

▶ COM Express Pin Assignments

Pin List for Pin-Out Type 6

The table below is a comprehensive list of all signal pins supported on the dual 220-pin COM Express connectors as defined for Type 6 in the PICMG COM.0 R3.1 specification.

Pin	Row A	MTH966 Difference	Row B	MTH966 Difference
1	GND (FIXED)		GND (FIXED)	
2	GBE0_MDI3-		GBE0_ACT#	
3	GBE0_MDI3+		LPC_FRAME#/ESPI_CS0#	LPC_FRAME# *Note1
4	GBE0_LINKMID#	GBE_LED1000#	LPC_AD0/ESPI_IO_0	LPC_AD0 *Note1
5	GBE0_LINKMAX#	GBE_LED2500#	LPC_AD1/ESPI_IO_1	LPC_AD1 *Note1
6	GBE0_MDI2-		LPC_AD2/ESPI_IO_2	LPC_AD2 *Note1
7	GBE0_MDI2+		LPC_AD3/ESPI_IO_3	LPC_AD3 *Note1
8	GBE0_LINK#		LPC_DRQ0#/ESPI_ ALERT0#	LPC_DRQ0# *Note1
9	GBE0_MDI1-		LPC_DRQ1#/ESPI_ ALERT1#	LPC_DRQ1# *Note1
10	GBE0_MDI1+		LPC_CLK/ESPI_CK	LPC_CLK *Note1
11	GND (FIXED)		GND (FIXED)	
12	GBE0_MDI0-		PWRBTN#	
13	GBE0_MDI0+		SMB_CK	
14	GBE0_CTREF	NC	SMB_DAT	
15	SUS_S3#		SMB_ALERT#	
16	SATA0_TX+		SATA1_TX+	
17	SATA0_TX-		SATA1_TX-	
18	SUS_S4#		SUS_STAT#/ESPI_RESET#	NC *Note1
19	SATA0_RX+		SATA1_RX+	
20	SATA0_RX-		SATA1_RX-	
21	GND (FIXED)		GND (FIXED)	
22	SATA2_TX+	NC	SATA3_TX+	NC
23	SATA2_TX-	NC	SATA3_TX-	NC
24	SUS_S5#		PWR_OK	
25	SATA2_RX+	NC	SATA3_RX+	NC
26	SATA2_RX-	NC	SATA3_RX-	NC
27	BATLOW#		WDT	
28	(S)ATA_ACT#		HDA_SDN2/SNDW0_CLK	HDA_SDN2 *Note2
29	HDA_SYNA		HDA_SDIN1/SNDW0_DAT	HDA_SDIN1 *Note2
30	HDA_RST#		HDA_SDIN0	
31	GND (FIXED)		GND (FIXED)	
32	HDA_BITCLK		SPKR	
33	HDA_SDOUT		I2C_CK	
34	BIOS_DIS0#/ ESPI_SAFS	BIOS_DIS0# *Note1	I2C_DAT	
35	THRMTRIP#		THRM#	
36	USB6-		USB7-	
37	USB6+		USB7+	
38	USB_6_7_OC#	USBOC_4567#	USB_4_5_OC#	USBOC_4567#
39	USB4-		USB5-	
40	USB4+		USB5+	
41	GND (FIXED)		GND (FIXED)	
42	USB2-		USB3-	
43	USB2+		USB3+	
44	USB_2_3_OC#		USB_0_1_OC#	
45	USB0-		USB1-	
46	USB0+		USB1+	
47	VCC_RTC		ESPI_EN#	PU 47Kohm to 1V8SB
48	RSMRST_OUT#		USB0_HOST_PRSNT	PD 47Kohm
49	GBE0_SDP	*Note1	SYS_RESET#	
50	LPC_SERIRQ		CB_RESET#	
51	GND (FIXED)		GND (FIXED)	
52	PCIE_TX5+		PCIE_RX5+	
53	PCIE_TX5-		PCIE_RX5-	
54	GPI0/SD_DATA0	GPI0 *Note3	GPO1/SD_CMD	GPO1 *Note3
55	PCIE_TX4+		PCIE_RX4+	
56	PCIE_TX4-		PCIE_RX4-	

Pin	Row A	MTH966 Difference	Row B	MTH966 Difference
57	GND		GPO2/SD_WP	GPO2 *Note3
58	PCIE_TX3+		PCIE_RX3+	
59	PCIE_TX3-		PCIE_RX3-	
60	GND (FIXED)		GND(FIXED)	
61	PCIE_TX2+		PCIE_RX2+	
62	PCIE_TX2-		PCIE_RX2-	
63	GPI1/SD_DATA1	GPI1 *Note3	GPO3/SD_CD#	GPO3 *Note3
64	PCIE_TX1+		PCIE_RX1+	
65	PCIE_TX1-		PCIE_RX1-	
66	GND		WAKE0#	
67	GPI2/SD_DATA2	GPI2 *Note3	WAKE1#	
68	PCIE_TX0+		PCIE_RX0+	
69	PCIE_TX0-		PCIE_RX0-	
70	GND (FIXED)		GND(FIXED)	
71	LVDS_A0+/eDP_TX2+	LVDS_A0+ *Note4	LVDS_B0+	
72	LVDS_A0-/eDP_TX2-	LVDS_A0- *Note4	LVDS_B0-	
73	LVDS_A1+/eDP_TX1+	LVDS_A1+ *Note4	LVDS_B1+	
74	LVDS_A1-/eDP_TX1-	LVDS_A1- *Note4	LVDS_B1-	
75	LVDS_A2+/eDP_TX0+	LVDS_A2+ *Note4	LVDS_B2+	
76	LVDS_A2-/eDP_TX0-	LVDS_A2- *Note4	LVDS_B2-	
77	LVDS_VDD_EN/ eDP_ VDD_EN	LVDS_VDD_EN *Note4	LVDS_B3+	
78	LVDS_A3+		LVDS_B3-	
79	LVDS_A3-		LVDS_BKLT_EN/ eDP_BKLT_EN **	LVDS_BKLT_EN *Note4
80	GND (FIXED)		GND(FIXED)	
81	LVDS_A_CK+/ eDP_TX3+	LVDS_A_CK+ *Note4	LVDS_B_CK+	
82	LVDS_A_CK-/ eDP_TX3-	LVDS_A_CK- *Note4	LVDS_B_CK-	
83	LVDS_I2C_CK/ eDP_AUX+		LVDS_BKLT_CTRL/ eDP_BKLT_CTRL	LVDS_BKLT_CTRL *Note4
84	LVDS_I2C_DAT/ eDP_ AUX-	LVDS_I2C_DAT *Note4	VCC_5V_SBY	
85	GPI3/SD_DATA3	GPI3 *Note3	VCC_5V_SBY	

Pin	Row A	MTH966 Difference	Row B	MTH966 Difference
86	GP_SPI_MOSI		VCC_5V_SBY	
87	eDP_HPD	*Note4	VCC_5V_SBY	
88	PCIE_CLK_REF+		BIOS_DIS1#	
89	PCIE_CLK_REF-		VGA_RED	NC
90	GND(FIXED)		GND(FIXED)	
91	SPI_POWER		VGA_GRN	NC
92	SPI_MISO	GPO0 *Note3	VGA_BLU	NC
93	GPO0/SD_CLK		VGA_HSYNA	NC
94	SPI_CLK		VGA_VSYNA	NC
95	SPI_MOSI		VGA_I2C_CK	NC
96	TPM_PP		VGA_I2C_DAT	NC
97	TYPE10#	NC	SPI_CS#	
98	SER0_TX		GP_SPI_MISO	
99	SER0_RX		GP_SPI_CK	
100	GND (FIXED)		GND (FIXED)	
101	SER1_TX/CAN0_TX	SER1_TX *Note5	FAN_PWMOUT	
102	SER1_RX/CAN0_RX	SER1_RX *Note5	FAN_TACHIN	
103	LID#		SLEEP#	
104	VCC_12V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
105	VCC_12V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
106	VCC_12V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
107	VCC_12V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
108	VCC_12V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
109	VCC_V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
110	GND (FIXED)		GND (FIXED)	

Note:
1. Th eAPI is BOM option supported by project basis.
2. The SoundWire function is not supported. The Pin B28 is reserved for PCIE_CLK_REQ function.
3. The SDIO function is not supported.
4. The eDP (in place of LVDS) is BOM option supported by project basis.
5. The CAN function (in place of SER) is BOM option supported by project basis.
6. For PCIe device down components on the carrier board, please use and place on the PCIe Lane0 port first.

Pin	Row C	MTH966 Difference	Row D	MTH966 Difference
1	GND (FIXED)		GND (FIXED)	
2	GND		GND	
3	USB_SSRX0-		USB_SSTX0-	
4	USB_SSRX0+		USB_SSTX0+	
5	GND		GND	
6	USB_SSRX1-		USB_SSTX1-	
7	USB_SSRX1+		USB_SSTX1+	
8	GND		GND	
9	USB_SSRX2-		USB_SSTX2-	
10	USB_SSRX2+		USB_SSTX2+	
11	GND (FIXED)		GND (FIXED)	
12	USB_SSRX3-		USB_SSTX3-	
13	USB_SSRX3+		USB_SSTX3+	
14	GND		GND	
15	USB4_1_LSTX	NC *Note7	DDI1_CTRLCLK_AUX+/ USB4_1_AUX+	DDI1_CTRLCLK_AUX+ *Note7
16	USB4_1_LSRX	NC *Note7	DDI1_CTRLDATA_AUX-/ USB4_1_AUX-	DDI1_CTRLDATA_AUX- *Note7
17	USB4_RT_ENA	NC *Note7	USB4_PD_I2C_ALERT#	*Note7
18	GND		PMCALERT#	
19	PCIE_RX6+		PCIE_TX6+	
20	PCIE_RX6-		PCIE_TX6-	
21	GND (FIXED)		GND (FIXED)	
22	PCIE_RX7+		PCIE_TX7+	
23	PCIE_RX7-		PCIE_TX7-	
24	DDI1_HPD		GND	
25	SML0_CLK		GND	
26	SML0_DAT		DDI1_PAIR0+/ USB4_1_ SSTX0+	DDI1_PAIR0+ *Note7
27	SML1_CLK		DDI1_PAIR0-/ USB4_1_ SSTX0-	DDI1_PAIR0- *Note7

Note:
7. The USB4 function is BOM option supported by project basis.

Pin	Row C	MTH966 Difference	Row D	MTH966 Difference
28	SML1_DAT		GND	
29	USB4_PD_I2C_CLK	*Note7	DDI1_PAIR1+/ USB4_1_ SSRX0+	DDI1_PAIR1+ *Note7
30	USB4_PD_I2C_DAT	*Note7	DDI1_PAIR1-/ USB4_1_SSRX0-	DDI1_PAIR1- *Note7
31	GND (FIXED)		GND(FIXED)	
32	DDI2_CTRLCLK_AUX+ / USB4_2_AUX+	DDI2_CTRLCLK_AUX+ *Note7	DDI1_PAIR2+/ USB4_1_SSTX1+	DDI1_PAIR2+ *Note7
33	DDI2_CTRLDATA_AUX-/ USB4_2_AUX-	DDI2_CTRLDATA_AUX- *Note7	DDI1_PAIR2-/ USB4_1_ SSTX1-	DDI1_PAIR2- *Note7
34	DDI2_DDC_AUX_SEL		DDI1_DDC_AUX_SEL	
35	USB4_2_LSTX	NC *Note7	USB4_2_LSRX	NC *Note7
36	DDI3_CTRLCLK_AUX+		DDI1_PAIR3+/ USB4_1_SSRX1+	DDI1_PAIR3+ *Note7
37	DDI3_CTRLDATA_AUX-		DDI1_PAIR3-/ USB4_1_SSRX1-	DDI1_PAIR3- *Note7
38	DDI3_DDC_AUX_SEL		GND	
39	DDI3_PAIR0+		DDI2_PAIR0+/ USB4_2_SSTX0+	DDI2_PAIR0+ *Note7
40	DDI3_PAIR0-		DDI2_PAIR0-/ USB4_2_SSTX0-	DDI2_PAIR0- *Note7
41	GND (FIXED)		GND(FIXED)	
42	DDI3_PAIR1+		DDI2_PAIR1+/ USB4_2_SSRX0+	DDI2_PAIR1+ *Note7
43	DDI3_PAIR1-		DDI2_PAIR1-/ USB4_2_SSRX0-	DDI2_PAIR1- *Note7
44	DDI3_HPD		DDI2_HPD	
45	GP_SPI_CS#		GND	
46	DDI3_PAIR2+		DDI2_PAIR2+/ USB4_2_ SSTX1+	DDI2_PAIR2+ *Note7
47	DDI3_PAIR2-		DDI2_PAIR2-/ USB4_2_ SSTX1-	DDI2_PAIR2- *Note7
48	RSVD		GND	
49	DDI3_PAIR3+		DDI2_PAIR3+/ USB4_2_ SSRX1+	DDI2_PAIR3+ *Note7
50	DDI3_PAIR3-		DDI2_PAIR3-/ USB4_2_ SSRX1-	DDI2_PAIR3- *Note7
51	GND (FIXED)		GND(FIXED)	
52	PEG_RX0+		PEG_TX0+	
53	PEG_RX0-		PEG_TX0-	
54	TYPE0#	NC	PEG_LANE_RV#	
55	PEG_RX1+		PEG_TX1+	

Pin	Row C	MTH966 Difference	Row D	MTH966 Difference
56	PEG_RX1-		PEG_TX1-	
57	TYPE1#	NC	TYPE2#	GND
58	PEG_RX2+		PEG_TX2+	
59	PEG_RX2-		PEG_TX2-	
60	GND (FIXED)		GND (FIXED)	
61	PEG_RX3+		PEG_TX3+	
62	PEG_RX3-		PEG_TX3-	
63	GND		GND	
64	GND		GND	
65	PEG_RX4+	*Note8	PEG_TX4+	*Note8
66	PEG_RX4-	*Note8	PEG_TX4-	*Note8
67	RAPID_SHUTDOWN		GND	
68	PEG_RX5+	*Note8	PEG_TX5+	*Note8
69	PEG_RX5-	*Note8	PEG_TX5-	*Note8
70	GND (FIXED)		GND (FIXED)	
71	PEG_RX6+	*Note8	PEG_TX6+	*Note8
72	PEG_RX6-	*Note8	PEG_TX6-	*Note8
73	GND		GND	
74	PEG_RX7+	*Note8	PEG_TX7+	*Note8
75	PEG_RX7-	*Note8	PEG_TX7-	*Note8
76	GND		GND	
77	GND		GND	
78	PEG_RX8+	*Note9	PEG_TX8+	*Note9
79	PEG_RX8-	*Note9	PEG_TX8-	*Note9
80	GND (FIXED)		GND (FIXED)	
81	PEG_RX9+	*Note9	PEG_TX9+	*Note9
82	PEG_RX9-	*Note9	PEG_TX9-	*Note9

Pin	Row C	MTH966 Difference	Row D	MTH966 Difference
83	GND		GND	
84	GND		GND	
85	PEG_RX10+	*Note9	PEG_TX10+	*Note9
86	PEG_RX10-	*Note9	PEG_TX10-	*Note9
87	GND		GND	
88	PEG_RX11+	*Note9	PEG_TX11+	*Note9
89	PEG_RX11-	*Note9	PEG_TX11-	*Note9
90	GND (FIXED)		GND (FIXED)	
91	PEG_RX12+	*Note9	PEG_TX12+	*Note9
92	PEG_RX12-	*Note9	PEG_TX12-	*Note9
93	GND		GND	
94	PEG_RX13+	*Note9	PEG_TX13+	*Note9
95	PEG_RX13-	*Note9	PEG_TX13-	*Note9
96	GND		GND	
97	GND		GND	
98	PEG_RX14+	*Note9	PEG_TX14+	*Note9
99	PEG_RX14-	*Note9	PEG_TX14-	*Note9
100	GND (FIXED)		GND (FIXED)	
101	PEG_RX15+	*Note9	PEG_TX15+	*Note9
102	PEG_RX15-	*Note9	PEG_TX15-	*Note9
103	GND		GND	
104	VCC_12V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
105	VCC_12V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
106	VCC_12V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
107	VCC_12V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
108	VCC_12V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
109	VCC_12V	VCC_8.5V~ 20V	VCC_12V	VCC_8.5V~ 20V
110	GND (FIXED)		GND (FIXED)	

Note:
8. The onboard NVME SSD (in place of PEG) is BOM option supported by project basis.
9. The PEG LANE 8~15 is supported by the H sku CPU only.

▶ COM Express Connector Signal Description

DDI / USB4 Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	MTH966	Module Base Specification R3.1
DDI1_PAIR0+/USB4_1_SSTX0+	D26	O, LV_DIFF USB_SS	AC coupled off Module		Default DDI, (Opt. USB4)	DDI1 pair 0 differential pairs. High speed USB4 data transmit pairs, pin shared with DDI1.
DDI1_PAIR0-/USB4_1_SSTX0-	D27					
DDI1_PAIR1+/USB4_1_SSRX0+	D29	O, LV_DIFF USB_SS	AC coupled off Module		Default DDI, (Opt. USB4)	DDI1 pair 1 differential pairs. High speed USB4 data receive pairs, pin shared with DDI1. For 4 lane DP Alternate Mode, these RX lines are repurposed as DP TX lines … per the USB4 specification
DDI1_PAIR1-/USB4_1_SSRX0-	D30					
DDI1_PAIR2+/USB4_1_SSTX1+	D32	O, LV_DIFF USB_SS	AC coupled off Module		Default DDI, (Opt. USB4)	DDI1 pair 2 differential pairs. High speed USB4 data transmit pairs, pin shared with DDI1.
DDI1_PAIR2-/USB4_1_SSTX1-	D33					
DDI1_PAIR3+/USB4_1_SSRX1+	D36	O, LV_DIFF USB_SS	AC coupled off Module		Default DDI, (Opt. USB4)	DDI1 pair 3 differential pairs. High speed USB4 data receive pairs, pin shared with DDI1. For 4 lane DP Alternate Mode, these RX lines are repurposed as DP TX lines … per the USB4 specification
DDI1_PAIR3-/USB4_1_SSRX1-	D37					
DDI1_CTRLCLK_AUX+/USB4_1_AUX+	D15	I/O, LV_DIFF	AC coupled on Module		PD 100K to GND, (S/W IC BTW Rpd/SOC)	DP AUX+ function if DDI1_DDC_AUX_SEL is no connect.
		I/O OD, CMOS	3.3V / 3.3V		PU 1.5K to 3.3V / PD 100K to GND. (S/W IC is placed between the two resistors.)	HDMI/DVI I2C CTRLCLK if DDI1_DDC_AUX_SEL is pulled high.
		Bi-Dir, LV_DIFF	AC coupled off Module			DisplayPort Aux pair for USB4 DP modes. Pin shared with DDI1.
DDI1_CTRLDATA_AUX-/USB4_1_AUX-	D16	I/O, LV_DIFF	AC coupled on Module		PU 100K to 3V3 (S/W IC BTW Rpu/SOC)	DP AUX- function if DDI1_DDC_AUX_SEL is no connect.
		IO OD, CMOS	3.3V / 3.3V		PU 1.5K to 3.3V/PU 100K to 3.3V. (S/W IC is placed between the two resistors.)	HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high.
		Bi-Dir, LV_DIFF	AC coupled off Module			DisplayPort Aux pair for USB4 DP modes. Pin shared with DDI1.
DDI1_DDC_AUX_SEL	D34	I CMOS	3.3V / 3.3V		PD 1M to GND	Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is unconnected the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals.
DDI1_HPD	C24	I CMOS	3.3V / 3.3V		PD 100K to GND	DDI1 Hot-Plug Detect
DDI2_PAIR0+/USB4_2_SSTX0+	D39	O LV_DIFF USB_SS	AC coupled off Module		Default DDI, (Opt. USB4)	DDI2 pair 0 differential pairs. High speed USB4 data transmit pairs, pin shared with DDI2.
DDI2_PAIR0-/USB4_2_SSTX0-	D40					
DDI2_PAIR1+/USB4_2_SSRX0+	D42	O LV_DIFF USB_SS	AC coupled off Module		Default DDI, (Opt. USB4)	DDI2 pair 1 differential pairs. High speed USB4 data receive pairs, pin shared with DDI2. For 4 lane DP Alternate Mode, these RX lines are repurposed as DP TX lines … per the USB4 specification
DDI2_PAIR1-/USB4_2_SSRX0-	D43					
DDI2_PAIR2+/USB4_2_SSTX1+	D46	O LV_DIFF USB_SS	AC coupled off Module		Default DDI, (Opt. USB4)	DDI2 pair 2 differential pairs. High speed USB4 data transmit pairs, pin shared with DDI2.
DDI2_PAIR2-/USB4_2_SSTX1-	D47					
DDI2_PAIR3+/USB4_2_SSRX1+	D49	O LV_DIFF USB_SS	AC coupled off Module		Default DDI, (Opt. USB4)	DDI2 pair 3 differential pairs. High speed USB4 data receive pairs, pin shared with DDI2. For 4 lane DP Alternate Mode, these RX lines are repurposed as DP TX lines … per the USB4 specification
DDI2_PAIR3-/USB4_2_SSRX1-	D50					
DDI2_CTRLCLK_AUX+/USB4_2_AUX+	C32	I/O, LV_DIFF	AC coupled on Module		PD 100K to GND, (S/W IC BTW Rpd/SOC)	DP AUX+ function if DDI2_DDC_AUX_SEL is no connect
		I/O OD, CMOS	3.3V / 3.3V		PU 1.5K to 3.3V / PD 100K to GND. (S/W IC is placed between the two resistors.)	HDMI/DVI I2C CTRLCLK if DDI2_DDC_AUX_SEL is pulled high
		Bi-Dir OD, CMOS	AC coupled off Module			DisplayPort Aux pair for USB4 DP modes. Pin shared with DDI2.

DDI2_CTRLDATA_AUX-/USB4_2_AUX-	C33	I/O, LV_DIFF	AC coupled on Module		PU 100K to 3V3 (S/W IC BTW Rpu/SOC)	DP AUX- function if DDI2_DDC_AUX_SEL is no connect.
		IO OD, CMOS	3.3V / 3.3V		PU 1.5K to 3.3V/PU 100K to 3.3V. (S/W IC is placed between the two resistors.)	HDMI/DVI I2C CTRLDATA if DDI2_DDC_AUX_SEL is pulled high.
		Bi-Dir OD, CMOS	AC coupled off Module			DisplayPort Aux pair for USB4 DP modes. Pin shared with DDI2.
DDI2_DDC_AUX_SEL	C34	幺	3.3V / 3.3V		PD 1M to GND	Selects the function of DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is unconnected the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals.
DDI2_HPD	D44	I CMOS	3.3V / 3.3V		PD 100K to GND	DDI2 Hot-Plug Detect
DDI3_PAIR0+	C39	O LV_DIFF USB_SS	AC coupled off Module			DDI3 pair 0 differential pairs.
DDI3_PAIR0-	C40					
DDI3_PAIR1+	C42	O LV_DIFF USB_SS	AC coupled off Module			DDI3 pair 1 differential pairs.
DDI3_PAIR1-	C43					
DDI3_PAIR2+	C46	O LV_DIFF USB_SS	AC coupled off Module			DDI3 pair 2 differential pairs.
DDI3_PAIR2-	C47					
DDI3_PAIR3+	C49	O LV_DIFF USB_SS	AC coupled off Module			DDI3 pair 3 differential pairs.
DDI3_PAIR3-	C50					
DDI3_CTRLCLK_AUX+	C36	I/O, LV_DIFF	AC coupled on Module		PD 100K to GND, (S/W IC BTW Rpd/SOC)	DP AUX+ function if DDI3_DDC_AUX_SEL is no connect.
		I/O OD, CMOS	3.3V / 3.3V		PU 1.5K to 3.3V / PD 100K to GND. (S/W IC is placed between the two resistors.)	HDMI/DVI I2C CTRLCLK if DDI3_DDC_AUX_SEL is pulled high.
DDI3_CTRLDATA_AUX-	C37	I/O, LV_DIFF	AC coupled on Module		PU 100K to 3V3 (S/W IC BTW Rpu/SOC)	DP AUX- function if DDI3_DDC_AUX_SEL is no connect.
		I/O OD, CMOS	3.3V / 3.3V		PU 1.5K to 3.3V/PU 100K to 3.3V. (S/W IC is placed between the two resistors.)	HDMI/DVI I2C CTRLDATA if DDI3_DDC_AUX_SEL is pulled high.
DDI3_DDC_AUX_SEL	C38	I CMOS	3.3V / 3.3V		PD 1M to GND	Selects the function of DDI3_CTRLCLK_AUX+ and DDI3_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is unconnected the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals.
DDI3_HPD	C44	I CMOS	3.3V / 3.3V		PD 100K to GND	DDI3 Hot-Plug Detect

eDP Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	**MTH966 (Option)**	Module Base Specification R3.1
eDP_TX0+	A75	O, LV_DIFF	AC Coupled off Module			eDP differential pairs
eDP_TX0-	A76					
eDP_TX1+	A73	O, LV_DIFF	AC Coupled off Module			eDP differential pairs
eDP_TX1-	A74					
eDP_TX2+	A71	O, LV_DIFF	AC Coupled off Module			eDP differential pairs
eDP_TX2-	A72					
eDP_TX3+	A81	O, LV_DIFF	AC Coupled off Module			eDP differential pairs
eDP_TX3-	A82					
eDP_VDD_EN	A77	O, CMOS	3.3V / 3.3V		PD 100 to GND	eDP power enable
eDP_BKLT_EN	B79	O, CMOS	3.3V / 3.3V		PD 100 to GND	eDP backlight enable
eDP_BKLT_CTRL	B83	O, CMOS	3.3V / 3.3V		PD 100 to GND	eDP backlight brightness control
eDP_AUX+	A83	I/O, LV_DIFF	AC Coupled off Module		PD 100K to GND	eDP AUX+/-
eDP_AUX-	A84				PU 100K to 3V3	
eDP_HPD	A87	I, CMOS	3.3V / 3.3V		PD 100K to GND	Detection of Hot Plug / Unplug and notification of the link layer

General Purpose PCI Express Lanes Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	MTH966	Module Base Specification R3.1
PCIE_TX0+	A68	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 0
PCIE_TX0-	A69				AC Coupling capacitor	
PCIE_RX0+	B68	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 0
PCIE_RX0-	B69					
PCIE_TX1+	A64	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 1
PCIE_TX1-	A65				AC Coupling capacitor	
PCIE_RX1+	B64	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 1
PCIE_RX1-	B65					
PCIE_TX2+	A61	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 2
PCIE_TX2-	A62				AC Coupling capacitor	
PCIE_RX2+	B61	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 2
PCIE_RX2-	B62					
PCIE_TX3+	A58	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 3
PCIE_TX3-	A59				AC Coupling capacitor	
PCIE_RX3+	B58	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 3
PCIE_RX3-	B59					
PCIE_TX4+	A55	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 4
PCIE_TX4-	A56				AC Coupling capacitor	
PCIE_RX4+	B55	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 4
PCIE_RX4-	B56					
PCIE_TX5+	A52	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 5
PCIE_TX5-	A53				AC Coupling capacitor	
PCIE_RX5+	B52	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 5
PCIE_RX5-	B53					
PCIE_TX6+	D19	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 6
PCIE_TX6-	D20				AC Coupling capacitor	
PCIE_RX6+	C19	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 6
PCIE_RX6-	C20					
PCIE_TX7+	D22	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 7
PCIE_TX7-	D23				AC Coupling capacitor	
PCIE_RX7+	C22	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 7
PCIE_RX7-	C23					
PEG_TX0+	D52	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 16
PEG_TX0-	D53				AC Coupling capacitor	These are the same lines as PEG_TX0±
PEG_RX0+	C52	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 16
PEG_RX0-	C53					These are the same lines as PEG_RX0±
PEG_TX1+	D55	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 17
PEG_TX1-	D56				AC Coupling capacitor	These are the same lines as PEG_TX1±
PEG_RX1+	C55	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 17
PEG_RX1-	C56					These are the same lines as PEG_RX1±
PEG_TX2+	D58	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 18
PEG_TX2-	D59				AC Coupling capacitor	These are the same lines as PEG_TX2±
PEG_RX2+	C58	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 18
PEG_RX2-	C59					These are the same lines as PEG_RX2±
PEG_TX3+	D61	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 19
PEG_TX3-	D62				AC Coupling capacitor	These are the same lines as PEG_TX3±
PEG_RX3+	C61	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 19
PEG_RX3-	C62					These are the same lines as PEG_RX3±
PEG_TX4+	D65	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 20
PEG_TX4-	D66				AC Coupling capacitor	These are the same lines as PEG_TX4±
PEG_RX4+	C65	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 20
PEG_RX4-	C66					These are the same lines as PEG_RX4±
PEG_TX5+	D68	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 21
PEG_TX5-	D69				AC Coupling capacitor	These are the same lines as PEG_TX5±

PEG_RX5+	C68	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 21
PEG_RX5-	C69					These are the same lines as PEG_RX5±
PEG_TX6+	D71	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 22
PEG_TX6-	D72				AC Coupling capacitor	These are the same lines as PEG_TX6±
PEG_RX6+	C71	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 22
PEG_RX6-	C72					These are the same lines as PEG_RX6±
PEG_TX7+	D74	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 23
PEG_TX7-	D75				AC Coupling capacitor	These are the same lines as PEG_TX7±
PEG_RX7+	C74	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 23
PEG_RX7-	C75					These are the same lines as PEG_RX7±
PEG_TX8+	D78	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 24
PEG_TX8-	D79				AC Coupling capacitor	These are the same lines as PEG_TX8±
PEG_RX8+	C78	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 24
PEG_RX8-	C79					These are the same lines as PEG_RX8±
PEG_TX9+	D81	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 25
PEG_TX9-	D82				AC Coupling capacitor	These are the same lines as PEG_TX9±
PEG_RX9+	C81	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 25
PEG_RX9-	C82					These are the same lines as PEG_RX9±
PEG_TX10+	D85	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 26
PEG_TX10-	D86				AC Coupling capacitor	These are the same lines as PEG_TX10±
PEG_RX10+	C85	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 26
PEG_RX10-	C86					These are the same lines as PEG_RX10±
PEG_TX11+	D88	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 27
PEG_TX11-	D89				AC Coupling capacitor	These are the same lines as PEG_TX11±
PEG_RX11+	C88	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 27
PEG_RX11-	C89					These are the same lines as PEG_RX11±
PEG_TX12+	D91	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 28
PEG_TX12-	D92				AC Coupling capacitor	These are the same lines as PEG_TX12±
PEG_RX12+	C91	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 28
PEG_RX12-	C92					These are the same lines as PEG_RX12±
PEG_TX13+	D94	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 29
PEG_TX13-	D95				AC Coupling capacitor	These are the same lines as PEG_TX13±
PEG_RX13+	C94	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 29
PEG_RX13-	C95					These are the same lines as PEG_RX13±
PEG_TX14+	D98	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 30
PEG_TX14-	D99				AC Coupling capacitor	These are the same lines as PEG_TX14±
PEG_RX14+	C98	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 30
PEG_RX14-	C99					These are the same lines as PEG_RX14±
PEG_TX15+	D101	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 31
PEG_TX15-	D102				AC Coupling capacitor	These are the same lines as PEG_TX15±
PEG_RX15+	C101	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 31
PEG_RX15-	C102					These are the same lines as PEG_RX15±
PCIE_CLK_REF+	A88	O PCIE	PCIE			Reference clock output for all PCI Express and PCI Express Graphics lanes.
PCIE_CLK_REF-	A89					
PEG_LANE_RV#	D54	I CMOS	3.3V / 3.3V		PU 20K to 3.3V	PCI Express Graphics lane reversal input strap. Pull low on the Carrier Board to reverse lane order.

Note: PEG_TX/RX[8:15] only supported by H-line SKU .

GPIO Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe Module PU/PD	MTH966 (No support SDIO)	Module Base Specification R3.1
GPO0/SD_CLK	A93	O CMOS	3.3V / 3.3V			General purpose output pins. Upon a hardware reset, these outputs **should** be low.
GPO1/SD_CMD	B54					
GPO2/SD_WP#	B57					
GPO3/SD_CD#	B63					
GPI0/SD_DATA0	A54	I CMOS	3.3V / 3.3V		PU 47KΩ to 3.3V	General purpose input pins. Pulled high internally on the Module.
GPI1/SD_DATA1	A63				PU 47KΩ to 3.3V	
GPI2/SD_DATA2	A67				PU 47KΩ to 3.3V	
GPI3/SD_DATA3	A85				PU 47KΩ to 3.3V	

Power and GND Signal Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe Module PU/PD	MTH966	Module Base Specification R3.1
VCC_12V	A104~A109 B104~B109 C104~C109 D104~D109	Power			Support 8.5V～20V	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.
VCC_5V_SBY	B84~B87	Power				Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.
VCC_RTC	A47	Power				Real-time clock circuit-power input. Nominally +3.0V.
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A75, A80, A90, A100, A110, B1, B11, B21 ,B31, B41, B51, B60, B70, B80, B90, B100, B110, C1, C2, C5, C8, C11, C14, C18, C21, C31, C41, C51, C60, C63, C64, C70, C73, C76, C77, C80, C83, C84, C87, C90, C93, C96, C97, C100,	Power				Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.

General Purpose Serial Interface Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe Module PU/PD	MTH966	Module Base Specification R3.1
SER0_TX	A98	O CMOS-T	3.3V/12V		series 300Ω to BTB	General purpose serial port 0 transmitter
SER0_RX	A99	I CMOS-T	3.3V/12V	PU	PU 47KΩ to 3.3V and series 300Ω to BTB	General purpose serial port 0 receiver
SER1_TX / CAN_TX	A101	O CMOS-T	3.3V/12V		series 300Ω to BTB	General purpose serial port 1 transmitter CAN(Controller Area Network) TX output for CAN Bus channel 0.
SER1_RX / CAN_RX	A102	I CMOS-T	3.3V/12V	PU	PU 47KΩ to 3.3V and series 300Ω to BTB	General purpose serial port 1 receiver CAN(Controller Area Network) RX input for CAN Bus channel 0.

Note: These signals use reclaimed VCC_12V pins. Refer to Section 5.8 'Protecting COM.0 Pins Reclaimed from the VCC_12V Pool' for additional design considerations.

I2C Signal Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe Module PU/PD	MTH966	Module Base Specification R3.1
I2C_CK	B33	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	PU 2.2KΩ to 3.3V Suspend	General purpose I2C port clock output
I2C_DAT	B34	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	PU 2.2KΩ to 3.3V Suspend	General purpose I2C port data I/O line

Miscellaneous Signal Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe Module PU/PD	MTH966	Module Base Specification R3.1
SPKR	B32	O CMOS	3.3V / 3.3V		PU 10KΩ to 3.3V, (D4 low)	Output for audio enunciator - the "speaker" in PC-AT systems. This port provides the PC beep signal and is mostly intended for debugging purposes.
WDT	B27	O CMOS	3.3V / 3.3V		PD 100KΩ to GND.	Output indicating that a watchdog time-out event has occurred.
FAN_PWMOUT	B101	O OD CMOS	3.3V / 12V		RSV PD 100KΩ to GND and series isolate diode.	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.
FAN_TACHIN	B102	I OD CMOS	3.3V / 12V	PU 47KΩ to 3.3V	Series isolate diode and PU 47K Ω to 3.3V	Fan tachometer input for a fan with a two pulse output.
TPM_PP	A96	I CMOS	3.3V / 3.3V	PD to GND.	PD 100KΩ to GND.	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.

Rapid Shutdown Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe Module PU/PD	MTH966	Module Base Specification R3.1
RAPID_SHUTDOWN	C67	I CMOS	5.0V Suspend / 5.0V	PD	PD 100KΩ to GND	Trigger for Rapid Shutdown. Must be driven to 5V though a <=50 ohm source impedance for ≥ 20 µs.

Thermal Protection Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe Module PU/PD	MTH966	Module Base Specification R3.1
THRM#	B35	I CMOS	3.3V / 3.3V	PU	PU 1KΩ to 3.3V	Input from off-Module temp sensor indicating an over-temp situation.
THRMTRIP#	A35	O CMOS	3.3V / 3.3V		PU 10KΩ to 3.3V and series isolate diode to BTB.	Active low output indicating that the CPU has entered thermal shutdown.

SMBUS Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe Module PU/PD	MTH966 (D4 from EC)	Module Base Specification R3.1
SMB_CK	B13	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	PU 1KΩ to 3.3V Suspend	System Management Bus bidirectional clock line.
SMB_DAT	B14	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	PU 1KΩ to 3.3V Suspend	System Management Bus bidirectional data line.
SMB_ALERT#	B15	I CMOS	3.3V Suspend/3.3V	PU 10KΩ to 3.3V Suspend	PU 10KΩ to 3.3V Suspend	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.

LPC/eSPI Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	**MTH966 (Default LPC, option eSPI)**	Module Base Specification R3.1
LPC_AD0/ESPI_IO_0	B4	I/O CMOS	3.3V / 3.3V			LPC Mode: LPC multiplexed address, command and data bus
			1.8V Suspend / 3.3V			ESPI Mode: eSPI Master Data Input / Outputs These are bi-directional input/output pins used to transfer data between master and slaves.
LPC_AD1/ESPI_IO_1	B5	I/O CMOS	3.3V / 3.3V			LPC Mode: LPC multiplexed address, command and data bus
			1.8V Suspend / 3.3V			ESPI Mode: eSPI Master Data Input / Outputs These are bi-directional input/output pins used to transfer data between master and slaves.
LPC_AD2/ESPI_IO_2	B6	I/O CMOS	3.3V / 3.3V			LPC Mode: LPC multiplexed address, command and data bus
			1.8V Suspend / 3.3V			ESPI Mode: eSPI Master Data Input / Outputs These are bi-directional input/output pins used to transfer data between master and slaves.
LPC_AD3/ESPI_IO_3	B7	I/O CMOS	3.3V / 3.3V			LPC Mode: LPC multiplexed address, command and data bus
			1.8V Suspend / 3.3V			ESPI Mode: eSPI Master Data Input / Outputs These are bi-directional input/output pins used to transfer data between master and slaves.
LPC_FRAME#/ESPI_CS0#	B3	O CMOS	3.3V / 3.3V			LPC Mode: LPC Frame indicates the start of a LPC cycle.
			1.8V Suspend / 3.3V			ESPI Mode: eSPI Master Chip Select Outputs Driving Chip Select0#. A low selects a particular eSPI slave for the transaction. Each of the eSPI slaves is connected to a dedicated Chip Selectn# pin.
LPC_CLK/ESPI_CK	B10	O CMOS	3.3V / 3.3V			LPC Mode: LPC clock output, 33MHz
			1.8V Suspend / 3.3V			ESPI Mode: eSPI Master Clock Output This pin provides the reference timing for all the serial input and output operations.
LPC_DRQ0#/ESPI_ALERT0#	B8	I CMOS	3.3V / 3.3V			LPC Mode: LPC serial DMA request
			1.8V Suspend / 3.3V	PU 1K	Option PU 10K to 1V8SB	ESPI Mode: eSPI pins used by eSPI slave to request service from the eSPI master.
LPC_DRQ1#/ESPI_ALERT1#	B9	I CMOS	3.3V / 3.3V			LPC Mode: LPC serial DMA request
			1.8V Suspend / 3.3V	PU 1K	Option PU 10K to 1V8SB	ESPI Mode: eSPI pins used by eSPI slave to request service from the eSPI master.
LPC_SERIRQ/ESPI_CS1#	A50	I/O CMOS	3.3V / 3.3V	PU 8.2K	PU 10K to 3V3	LPC Mode: LPC serial interrupt
		O CMOS	1.8V Suspend / 3.3V			ESPI Mode: eSPI Master Chip Select Outputs Driving Chip Select# A low selects a particular eSPI slave for the transaction. Each of the eSPI slaves is connected to a dedicated Chip Selectn# pin.
SUS_STAT#/ESPI_RESET#	B18	O CMOS	3.3V Suspend / 3.3V			LPC Mode: SUS_STAT# indicates imminent suspend operation. It is used to notify LPC devices that a low power state will be entered soon. LPC devices may need to preserve memory or isolate outputs during the low power state.
			1.8V Suspend / 1.8V		RSVD PD 75K to GND	ESPI Mode: eSPI Reset Reset the eSPI interface for both master and slaves. eSPI Reset# is typically driven from eSPI master to eSPI slaves.
ESPI_EN#	B47	I CMOS	1.8V Suspend / 1.8V	PU 20K	PU 47K to 1V8SB	This signal is used by the Carrier to indicate the operating mode of the LPC/eSPI bus. If left unconnected on the carrier, LPC mode (default) is selected. If pulled to GND on the carrier, eSPI mode is selected. This signal is pulled to a logic high on the module through a resistor. The Carrier should only float this line or pull it low.
BIOS_DIS0#	A34	I CMOS	3.3V Suspend / 3.3V	PU 10K	PU 10K to 3V3SB_EC	Selection strap to determine the BIOS boot device. The Carrier should only float these or pull them low.
BIOS_DIS1#	B88	I CMOS	3.3V Suspend / 3.3V	PU 10K	PU 10K to 3V3SB_EC	Selection strap to determine the BIOS boot device. The Carrier should only float these or pull them low.

LVDS Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	MTH966	Module Base Specification R3.1
LVDS_A0+	A71	O, LVDS	LVDS		Default LVDS, option eDP	LVDS Channel A differential pairs The LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/-. LVDS_A_CK+/-, LVDS_B_CK+/-) shall have 100Ω terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer on-board. Often the termination is on the LVDS panel itself.
LVDS_A0-	A72					
LVDS_A1+	A73	O, LVDS	LVDS			
LVDS_A1-	A74					
LVDS_A2+	A75	O, LVDS	LVDS			
LVDS_A2-	A76					
LVDS_A3+	A78	O, LVDS	LVDS			
LVDS_A3-	A79					
LVDS_A_CK+	A81	O, LVDS	LVDS			LVDS Channel A differential clock
LVDS_A_CK-	A82					
LVDS_B0+	B71	O, LVDS	LVDS			LVDS Channel B differential pairs The LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/-. LVDS_A_CK+/-, LVDS_B_CK+/-) shall have 100Ω terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer on-board. Often the termination is on the LVDS panel itself.
LVDS_B0-	B72		LVDS			
LVDS_B1+	B73	O, LVDS	LVDS			
LVDS_B1-	B74		LVDS			
LVDS_B2+	B75	O, LVDS	LVDS			
LVDS_B2-	B76		LVDS			
LVDS_B3+	B77	O, LVDS	LVDS			
LVDS_B3-	B78		LVDS			
LVDS_B_CK+	B81	O, LVDS	LVDS			LVDS Channel B differential clock
LVDS_B_CK-	B82		LVDS			
LVDS_VDD_EN	A77	O, CMOS	3.3V / 3.3V		PD 100K to GND	LVDS panel power enable
LVDS_BKLT_EN	B79	O, CMOS	3.3V / 3.3V		PD 100K to GND	LVDS panel backlight enable
LVDS_BKLT_CTRL	B83	O, CMOS	3.3V / 3.3V		PD 100K to GND	LVDS panel backlight brightness control
LVDS_I2C_CK	A83	I/O OD, CMOS	3.3V / 3.3V	PU 2.2K	PU 4.7K to 3V3	I2C clock output for LVDS display use
LVDS_I2C_DAT	A84	I/O OD, CMOS	3.3V / 3.3V	PU 2.2K	PU 4.7K to 3V3	I2C data line for LVDS display use

Module type Signal Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe Module PU/PD	MTH966	Module Base Specification R3.1
TYPE0#	C54	PDS			N.C.	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module. The pins are tied on the Module to either ground (GND) or are no-connects (NC). For Pin-out Type 1 and Type 10, these pins are not present (X). TYPE2# TYPE1# TYPE0# X X X Pin-out Type 10, Pin out Type 1 (deprecated) NC NC NC Pin out Type 2 (deprecated) NC NC GND Pin out Type 3 (no IDE) (deprecated) NC GND NC Pin out Type 4 (no PCI) (deprecated) NC GND GND Pin out Type 5 (no IDE、PCI) (deprecated) GND NC NC Pin out Type 6 (no IDE, no PCI) GND NC GND Pin out Type 7 * The Carrier Board should implement combinatorial logic that monitors the Module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible Module pin out type is detected. The Carrier Board logic may also
TYPE1#	C57	PDS			N.C.	
TYPE2#	D57	PDS			GND	
TYPE10#	A97	PDS			N.C.	Dual use pin. Indicates to the Carrier Board that a Type 10 Module is installed. Indicates to the Carrier that a Rev 1.0 or a Rev 2.0/3.0 Module is installed. TYPE10# NC Pin-out R2.0 PD Pin-out Type 10 pull down to ground with 47K resistor 12V Pin-out R1.0 This pin is reclaimed from the VCC_12V pool. In R1.0 Modules this pin will connect to other VCC_12V pins. In R2.0 this pin is defined as a no connect for types 1-6. In R3.0 this pin is defined as a no connect for types 6 and 7. A Carrier can detect a R1.0 Module by the presence of 12V on this pin. R2.0 Module types 1-6 will no connect this pin. R3.0 Module types 6 and 7 will no connect this pin. Type 10 Modules shall pull this

HDA and SoundWire Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	MTH966 PU/PD	Module Base Specification R3.1
HDA_RST#	A30	O CMOS	3.3V Suspend / 3.3V			Reset output to CODEC, active low.
HDA_SYNC	A29	O CMOS	3.3V / 3.3V			Sample-synchronization signal to the CODEC(s).
HDA_BITCLK	A32	I/O CMOS	3.3V / 3.3V			Serial data clock generated by the external CODEC(s).
HDA_SDOUT	A33	O CMOS	3.3V / 3.3V			Serial TDM data output to the CODEC.
HDA_SDIN0	B30	I/O CMOS	3.3V Suspend / 3.3V			Serial TDM data input from CODEC 0
HDA_SDIN1 / SNDW0_DAT	B29	I/O CMOS	3.3V Suspend / 3.3V 1.8V Suspend / 3.3V			Serial TDM data input from CODEC 1 Alternative use as SoundWire bi-directional data line
HDA_SDIN2 / SNDW0_CLK	B28	I/O CMOS	3.3V Suspend / 3.3V 1.8V Suspend / 3.3V			Serial TDM data input from CODEC 2 Alternative use as SoundWire clock line

NBASE-T ("Gigabit") Ethernet Signals

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	MTH966 PU/PD	Module Base Specification R3.1
GBE0_MDI0+	A13	I/O MDI	Less than 3.3V May be active in			Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes or in 2.5, 5.0 and 10 Gbps modes. Some pairs are unused in some modes, per the following:
GBE0_MDI0-	A12	I/O MDI	Less than 3.3V May be active in			
GBE0_MDI1+	A10	I/O MDI	Less than 3.3V May be active in			
GBE0_MDI1-	A9	I/O MDI	Less than 3.3V May be active in			
GBE0_MDI2+	A7	I/O MDI	Less than 3.3V May be active in			
GBE0_MDI2-	A6	I/O MDI	Less than 3.3V May be active in			
GBE0_MDI3+	A3	I/O MDI	Less than 3.3V May be active in			
GBE0_MDI3-	A2	I/O MDI	Less than 3.3V May be active in			
GBE0_ACT#	B2	OD CMOS	3.3V Suspend/3.3V		RSVD PU 10KΩ to 3V3DU	Gigabit Ethernet Controller 0 activity indicator, active low.
GBE0_LINK#	A8	OD CMOS	3.3V Suspend/3.3V		RSVD PU 10KΩ to 3V3DU	Gigabit Ethernet Controller 0 link indicator, active low.
GBE0_LINK_MID#	A4	OD CMOS	3.3V Suspend/3.3V		RSVD PU 10KΩ to 3V3DU	Gigabit Ethernet Controller MID Speed Link indicator. Active low. If active, the link is established but at a speed lower than the maximum speed supported by the Ethernet controller. Note that based on capabilities of the Ethernet controller used this signal might not be active for all possible lower link speeds. Was GBE0_LINK100# in COM Express Rev. 3.0.
GBE0_LINK_MAX#	A5	OD CMOS	3.3V Suspend/3.3V		RSVD PU 10KΩ to 3V3DU	Gigabit Ethernet Controller MAX Speed Link Indicator. Active low. If active, the link is established at the maximum link speed supported by the controller. Was GBE0_LINK1000# in COM Express Rev. 3.0.
GBE0_CTREF	A14	REF	GND min, 3.3V max		N.C.	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be limited to 250 mA or less.
GBE0_SDP	A49	I/O CMOS	3.3V Suspend/3.3V		RSVD PU 10KΩ	Gigabit Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1pps signal. This line should be weakly terminated on the Module silicon or hardware, to prevent a floating input.

	1000BASE-T 2.5GBASE-T 5.0GBASE-T 10GBASE-T	100BASE-TX	10BASE-T
MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-
MDI[1]+/-	B1_DB+/-	RX+/-	RX+/-
MDI[2]+/-	B1_DC+/-		
MDI[3]+/-	B1_DD+/-		

Power and System Management Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe Module PU/PD	MTH966	Module Base Specification R3.1
PWRBTN#	B12	I CMOS	3.3V Suspend/3.3V	PU 10KΩ to 3.3V Suspend	PU 10KΩ to 3.3V Suspend	A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off and other suspend states, as well as powering the system down.
SYS_RESET#	B49	I CMOS	3.3V Suspend/3.3V	PU 10KΩ to 3.3V Suspend	PU 10KΩ to 3.3V Suspend	Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used.
CB_RESET#	B50	O CMOS	3.3V Suspend/3.3V			Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software.
PWR_OK	B24	I CMOS	3.3V Suspend/3.3V	PU 10KΩ to 3.3V Suspend	PU 10KΩ to 3V3DU then plus series diode to BTB pin.	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGAs or other configurable devices time to be programmed.
SUS_STAT#	B18	O CMOS	3.3V Suspend / 3.3V		RSVD PD 75K to GND.	Indicates imminent suspend operation; used to notify LPC devices. Not used in eSPI implementations.
SUS_S3#	A15	O CMOS	3.3V Suspend/3.3V		PD 100KΩ to GND	Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board may be used to enable the non-standby power on a typical ATX supply.
SUS_S4#	A18	O CMOS	3.3V Suspend/3.3V		PD 100KΩ to GND	Indicates system is in Suspend to Disk state. Active low output.
SUS_S5#	A24	O CMOS	3.3V Suspend/3.3V		PD 100KΩ to GND	Indicates system is in Soft Off state.
WAKE0#	B66	I CMOS	3.3V Suspend/3.3V	PU 10KΩ to 3.3V Suspend	PU 1KΩ to 3.3V Suspend	PCI Express wake up signal.
WAKE1#	B67	I CMOS	3.3V Suspend/3.3V	PU 10KΩ to 3.3V Suspend	PU 2.2KΩ to 3.3V Suspend	General purpose wake up signal. May be used to implement wake-up on PS2 keyboard or mouse activity.
BATLOW#	A27	I CMOS	3.3V Suspend/ 3.3V	PU 10KΩ to 3.3V Suspend	PU 10KΩ to 3.3V Suspend	In a T6,T10 system, Indicates that external battery is low. This port provides a battery-low signal to the Module for orderly transitioning to power saving or power cut-off ACPI modes. In a type 7 system, BATLOW# can be used as a power fail indication.
LID#	A103	I OD CMOS	3.3V Suspend/12V	PU 47KΩ to 3.3V Suspend	PU 47KΩ to 3.3V Suspend & isolate by Diode	LID switch. Low active signal used by the ACPI operating system for a LID switch.
SLEEP#	B103	I OD CMOS	3.3V Suspend/12V	PU 47KΩ to 3.3V Suspend	PU 47KΩ to 3.3V Suspend & isolate by Diode	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.
RSMRST_OUT#	A48	O CMOS	3.3V Suspend/3.3V		Series a 1G125 buffer .	This is a buffered copy of the internal Module RSMRST# (Resume Reset,active low) signal. The internal Module RSMRST# signal is an input to the chipset or SOC and when it transitions from low to high it indicates that the suspend well power rails are stable. USB devices on the Carrier that are to be active in S5 / S3 / S0 should not have their 5V supply applied before RSMRST_OUT# goes high. RSMRST_OUT# shall be a 3.3V CMOS Module output, active in all power states.

SPI Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	MTH966	Module Base Specification R3.1
SPI_CS#	B97	O CMOS	3.3V Suspend or 3.3V S0 / 3.3V 1.8V Suspend or 1.8V S0 / 3.3V		through S/W IC to BTB pin	Chip select for Carrier Board SPI - may be sourced from chipset SPI0 or SPI1
SPI_MISO	A92	I CMOS	3.3V Suspend or 3.3V S0 / 3.3V 1.8V Suspend or 1.8V S0 / 3.3V		through LS NTB0104	Data in to Module from Carrier SPI
SPI_MOSI	A95	O CMOS	3.3V Suspend or 3.3V S0 / 3.3V 1.8V Suspend or 1.8V S0 / 3.3V		through LS NTB0104	Data out from Module to Carrier SPI
SPI_CLK	A94	O CMOS	3.3V Suspend or 3.3V S0 / 3.3V 1.8V Suspend or 1.8V S0 / 3.3V		through LS NTB0104	Clock from Module to Carrier SPI
SPI_POWER	A91	Power Out	3.3V Suspend or 3.3V S0 / 3.3V 1.8V Suspend or 1.8V S0 / 3.3V		3.3V Suspend	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier Board.

General Purpose SPI Interface Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	MTH966	Module Base Specification R3.1
GP_SPI_CS#	C45	O CMOS	3.3V Suspend or 3.3V S0 / 3.3V			Chip select from Module SPI Master to Carrier SPI Slave
GP_SPI_MISO	B98	I CMOS	3.3V Suspend or 3.3V S0 / 3.3V			Data in to Module SPI Master from Carrier SPI Slave "Master In Slave Out"
GP_SPI_MOSI	A86	O CMOS	3.3V Suspend or 3.3V S0 / 3.3V			Data out from Module SPI Master to Carrier SPI Slave "Master Out Slave In"
GP_SPI_CK	B99	O CMOS	3.3V Suspend or 3.3V S0 / 3.3V			Clock from Module SPI Master to Carrier SPI Slave

Note: the Carrier GP SPI device shall not be powered by the SPI_POWER pin.

VGA Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	MTH966 (Not support)	Module Base Specification R3.1
VGA_RED		O VGA	Analog Low Voltage	PD 150 ohm	N.C.	Red for monitor. Analog DAC output, designed to drive a 37.5Ω equivalent load
VGA_GRN		O VGA	Analog Low Voltage	PD 150 ohm	N.C.	Green for monitor. Analog DAC output, designed to drive a 37.5Ω equivalent load.
VGA_BLU		O VGA	Analog Low Voltage	PD 150 ohm	N.C.	Blue for monitor. Analog DAC output, designed to drive a 37.5Ω equivalent load.
VGA_HSYNC		O VGA	3.3V / 3.3V		N.C.	Horizontal sync output to VGA monitor
VGA_VSYNC		O VGA	3.3V / 3.3V		N.C.	Vertical sync output to VGA monitor
VGA_I2C_CK		I/O OD CMOS	3.3V / 3.3V	PU 2.2K	N.C.	DDC clock line (I2C port dedicated to identify VGA monitor capabilities)
VGA_I2C_DAT		I/O OD CMOS	3.3V / 3.3V	PU 2.2K	N.C.	DDC data line.

USB 2.0 and USB 3.2 Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	MTH966	Module Base Specification R3.1
USB0+	A46	I/O USB	3.3V Suspend/3.3V			USB differential pairs, USB0 may be configured as a USB client or as a host, or both at the Module designer's discretion. All other USB ports, if implemented, shall be host ports.
USB0-	A45					
USB1+	B46	I/O USB	3.3V Suspend/3.3V			USB differential pairs, channel 1.
USB1-	B45					
USB2+	A43	I/O USB	3.3V Suspend/3.3V			USB differential pairs, channel 2.
USB2-	A42					
USB3+	B43	I/O USB	3.3V Suspend/3.3V			USB differential pairs, channel 3.
USB3-	B42					
USB4+	A40	I/O USB	3.3V Suspend/3.4V			USB differential pairs, channel 4.
USB4-	A39					
USB5+	B40	I/O USB	3.3V Suspend/3.5V			USB differential pairs, channel 5.
USB5-	B39					
USB6+	A37	I/O USB	3.3V Suspend/3.6V			USB differential pairs, channel 6.
USB6-	A36					
USB7+	B37	I/O USB	3.3V Suspend/3.7V			USB differential pairs, USB7 may be configured as a USB client or as a host, or both at the Module designer's discretion. All other USB ports, if implemented, shall be host ports.
USB7-	B36					
USB_0_1_OC#	B44	I CMOS	3.3V Suspend/3.3V	PU 10KΩ	PU 10KΩ to 3V3 Suspend.	USB over-current sense, USB channels 0 and 1. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_2_3_OC#	A44	I CMOS	3.3V Suspend/3.3V	PU 10KΩ	PU 10KΩ to 3V3 Suspend.	USB over-current sense, USB channels 2 and 3. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_4_5_OC#	B38	I CMOS	3.3V Suspend/3.4V	PU 10KΩ	PU 10KΩ to 3V3 Suspend.	USB over-current sense, USB channels 4 and 5. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_6_7_OC#	A38	I CMOS	3.3V Suspend/3.5V	PU 10KΩ	PU 10KΩ to 3V3 Suspend.	USB over-current sense, USB channels 6 and 7. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_SSTX0+	D4	O USB_SS	AC coupled on Module		AC Coupling capacitor	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSTX0-	D3				AC Coupling capacitor	
USB_SSRX0+	C4	I USB_SS	AC coupled off Module			Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSRX0-	C3					
USB_SSTX1+	D7	O USB_SS	AC coupled on Module		AC Coupling capacitor	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSTX1-	D6				AC Coupling capacitor	
USB_SSRX1+	C7	I USB_SS	AC coupled off Module			Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSRX1-	C6					
USB_SSTX2+	D10	O USB_SS	AC coupled on Module		AC Coupling capacitor	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSTX2-	D9				AC Coupling capacitor	
USB_SSRX2+	C10	I USB_SS	AC coupled off Module			Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSRX2-	C9					
USB_SSTX3+	D13	O USB_SS	AC coupled on Module		AC Coupling capacitor	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSTX3-	D12				AC Coupling capacitor	
USB_SSRX3+	C13	I USB_SS	AC coupled off Module			Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSRX3-	C12					
USB0_HOST_PRSNT	B48	I CMOS	3.3V Suspend/3.3V	PD 47KΩ	PD 47KΩ to GND	Module USB client may detect the presence of a USB host on USB0. A high value indicates that a host is present.
RSMRST_OUT#	A48	O CMOS	3.3V Suspend/3.3V		Series a 1G125 buffer .	USB devices that are to be powered in the S5 / S4 / S3 Suspend states should not have their 5V VBUS power enabled before RSMRST_OUT# transitions to the hi state. RSMRST_OUT# is also described in Table of "Power and System Management signals description".

Note: USB0 may optionally be configured as a USB client on all current Module Types (T6, T7,T10). A USB0_HOSTPRSNT# signal is defined to facilitate this.

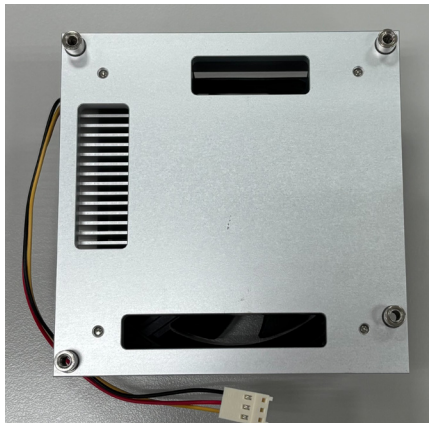
SATA Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	MTH966	Module Base Specification R3.1
SATA0_TX+	A16	O SATA	AC coupled on Module		AC Coupling capacitor	Serial ATA Channel 0 transmit differential pair.
SATA0_TX-	A17	O SATA	AC coupled on Module		AC Coupling capacitor	
SATA0_RX+	A19	I SATA	AC coupled on Module		AC Coupling capacitor	Serial ATA Channel 0 receive differential pair.
SATA0_RX-	A20	I SATA	AC coupled on Module		AC Coupling capacitor	
SATA1_TX+	B16	O SATA	AC coupled on Module		AC Coupling capacitor	Serial ATA Channel 1 transmit differential pair.
SATA1_TX-	B17	O SATA	AC coupled on Module		AC Coupling capacitor	
SATA1_RX+	B19	I SATA	AC coupled on Module		AC Coupling capacitor	Serial ATA Channel 1 receive differential pair.
SATA1_RX-	B20	I SATA	AC coupled on Module		AC Coupling capacitor	
SATA2_TX+	A22	O SATA	AC coupled on Module		N.C.	Serial ATA Channel 2 transmit differential pair.
SATA2_TX-	A23	O SATA	AC coupled on Module		N.C.	
SATA2_RX+	A25	I SATA	AC coupled on Module		N.C.	Serial ATA Channel 2 receive differential pair.
SATA2_RX-	A26	I SATA	AC coupled on Module		N.C.	
SATA3_TX+	B22	O SATA	AC coupled on Module		N.C.	Serial ATA Channel 3 transmit differential pair.
SATA3_TX-	B23	O SATA	AC coupled on Module		N.C.	
SATA3_RX+	B25	I SATA	AC coupled on Module		N.C.	Serial ATA Channel 3 receive differential pair.
SATA3_RX-	B26	I SATA	AC coupled on Module		N.C.	
(S)ATA_ACT#	A28	O CMOS	3.3V / 3.3V		AND Gate out, up to 3.3V	Serial ATA activity indicator, active low.

USB4 Sideband Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe SPEC PU/PD	MTH966	Module Base Specification R3.1
USB4_1_LSTX	C15	O CMOS	3.3V / 3.3V			Side-band TX interface for USB4 Alternate modes “Low Speed” asynchronous serial TX line
USB4_1_LSRX	C16	I CMOS	3.3V / 3.3V	See Note below table		Side-band RX interface for USB4 Alternate modes “Low Speed” asynchronous serial RX line
USB4_2_LSTX	C35	O CMOS	3.3V / 3.3V			Side-band TX interface for USB4 Alternate modes “Low Speed” asynchronous serial TX line
USB4_2_LSRX	D35	I CMOS	3.3V / 3.3V			Side-band RX interface for USB4 Alternate modes “Low Speed” asynchronous serial RX line
USB4_RT_ENA	C17	O CMOS	3.3V / 3.3V		PU 10KΩ	Power Enable for Carrier based USB Retimers. Sourced from chipset GPO. “USB Retimer Enable ” .
USB4_PD_I2C_CLK	C29	Bi-Dir OD CMOS	3.3V Suspend / 3.3V	PU 2K	PU 2.2K	I2C clock line between Module based Embedded Controller master and Carrier based USB Power Delivery Controller slave.
USB4_PD_I2C_DAT	C30	Bi-Dir OD CMOS	3.3V Suspend / 3.3V	PU 2K	PU 2.2K	I2C data line between Module based Embedded Controller master and Carrier based USB Power Delivery Controller slave.
USB4_PD_I2C_ALERT#	D17	I	3.3V Suspend / 3.3V	PU 100K	PU 100K	Active low Alert signal from USB Power Delivery Controller to the Module Embedded Controller.
SML0_DAT	C26	Bi-Dir OD CMOS	3.3V Suspend / 3.3V	PU 2K	PU 1K (w/t I226)	Data lines for I2C data based System Management Links between chipset masters and Carrier. SML0 is used to control the Carrier based USB retimers.
SML0_CLK	C25	Bi-Dir OD CMOS	3.3V Suspend / 3.3V	PU 2K	PU 1K (w/t I226)	Clock lines for System Management Links 0 and 1. SML0 is used to support Carrier USB4 retimers
SML1_DAT	C28	Bi-Dir OD CMOS	3.3V Suspend / 3.3V	PU 2K	PU 1K	Data lines for I2C data based System Management Links between chipset masters and Carrier. SML1 is used to control the Carrier based Power Delivery Controller.
SML1_CLK	C27	Bi-Dir OD CMOS	3.3V Suspend / 3.3V	PU 2K	PU 1K	Clock lines for System Management Links 0 and 1. SML1 is used to support Carrier USB Power Delivery (PD) Controller.
PMCALERT#	D18	I CMOS	3.3V / 3.3V	PU 10K	PU 10K	Active low Alert signal associated with the SML1 System Management link, from the Carrier based USB Power Delivery Controller.

▶ Cooling Option

Cooling Fan

Top View of the Heat Sink



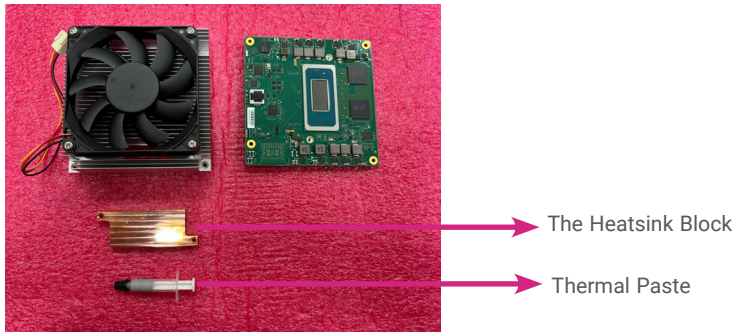
Bottom View of the Heat Sink

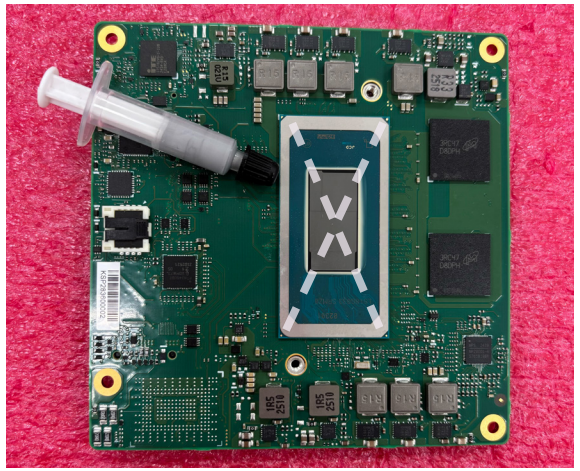
▶ Installing MTH966 onto a Carrier Board

Important:
The carrier board (COM335) used in this section is for reference purpose only and may not resemble your carrier board. These illustrations are mainly to guide you on how to install MTH966 onto the carrier board of your choice.

Step 1: Apply Thermal Paste to the CPU

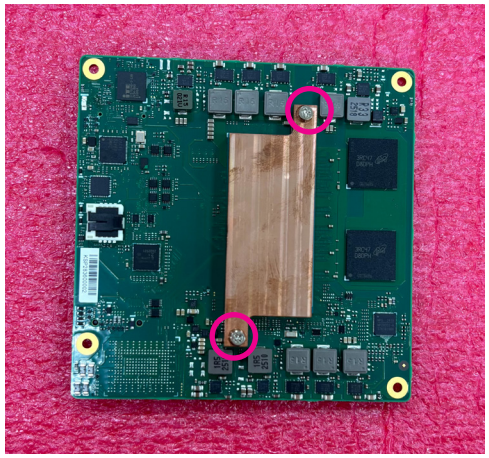
Squeeze a small amount of thermal paste onto the CPU surface.
Apply it in a diagonal "X" pattern for even coverage.





Step 2: Install the Heatsink Block

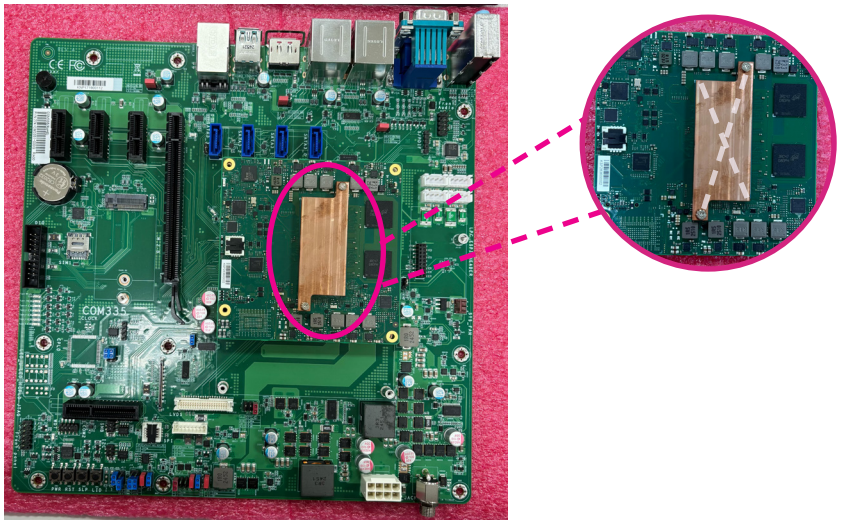
Carefully place the heatsink block on top of the CPU.
Align it properly and tighten the screws to secure it in place.



Make sure the connector is properly connected to the MTH966.

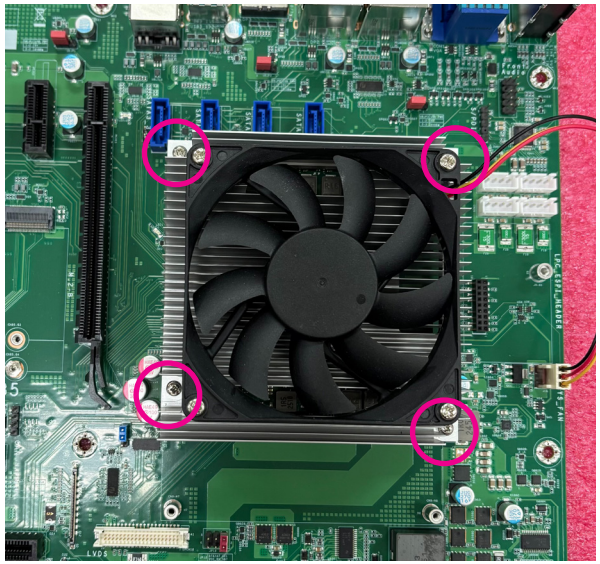
Step 3: Install MTH966 onto a Carrier Board

Mount the MTH966 onto a carrier board.
Once installed, apply thermal paste diagonally on top of the heatsink block.
Make sure the connector is properly connected to the MTH966.



Step 4: Attach the Cooling Fan

Align the cooling fan with the heatsink block.
Place it on top and secure it with screws.
Use the provided mounting screws to install the heat sink onto the module.



Chapter 4 - BIOS Settings

▶ Overview

The BIOS is a program that takes care of the basic level of communication between the CPU and peripherals. It contains codes for various advanced features found in this system board. The BIOS allows you to configure the system and save the configuration in a battery-backed CMOS so that the data retains even when the power is off. In general, the information stored in the CMOS RAM of the EEPROM will stay unchanged unless a configuration change has been made such as a hard drive replaced or a device added.
It is possible that the CMOS battery will fail causing CMOS data loss. If this happens, you need to install a new CMOS battery and reconfigure the BIOS settings.

Note:
The BIOS is constantly updated to improve the performance of the system board; therefore the BIOS screens in this chapter may not appear the same as the actual one. These screens are for reference purpose only.

Default Configuration
Most of the configuration settings are either predefined according to the Load Optimal Defaults settings which are stored in the BIOS or are automatically detected and configured without requiring any actions. There are a few settings that you may need to change depending on your system configuration.

Entering the BIOS Setup Utility
The BIOS Setup Utility can only be operated from the keyboard and all commands are keyboard commands. The commands are available at the right side of each setup screen.
The BIOS Setup Utility does not require an operating system to run. After you power up the system, the BIOS message appears on the screen and the memory count begins. After the memory test, the message “Press DEL to run setup” will appear on the screen. If the message disappears before you respond, restart the system or press the “Reset” button. You may also restart the system by pressing the <Ctrl> <Alt> and <Del> keys simultaneously.

Legends

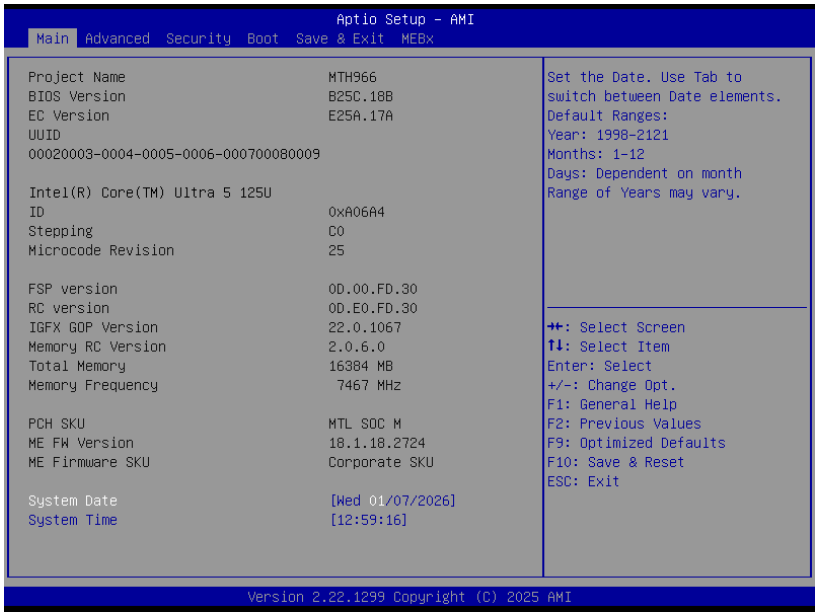
Keys	Function
Right / Left arrow	Move the highlight left or right to select a menu
Up / Down arrow	Move the highlight up or down between submenus or fields
<Enter>	Enter the highlighted submenu
+ (plus key)/F6	Scroll forward through the values or options of the highlighted field
- (minus key)/F5	Scroll backward through the values or options of the highlighted field
<F1>	Display general help
<F2>	Display previous values
<F12>	Popup Boot Device List
<F9>	Optimized defaults
<F10>	Save and Exit
<Esc>	Return to previous menu

Scroll Bar
When a scroll bar appears to the right of the setup screen, it indicates that there are more available fields not shown on the screen. Use the up and down arrow keys to scroll through all the available fields.

Submenu
When “▶” appears on the left of a particular field, it indicates that a submenu which contains additional options are available for that field. To display the submenu, move the highlight to that field and press <Enter>.

▶ Main

The Main menu is the first screen that you will see when you enter the BIOS Setup Utility.



System Date

The date format is <month>, <date>, <year>. Press "Tab" to switch to the next field and press "-" or "+" to modify the value.

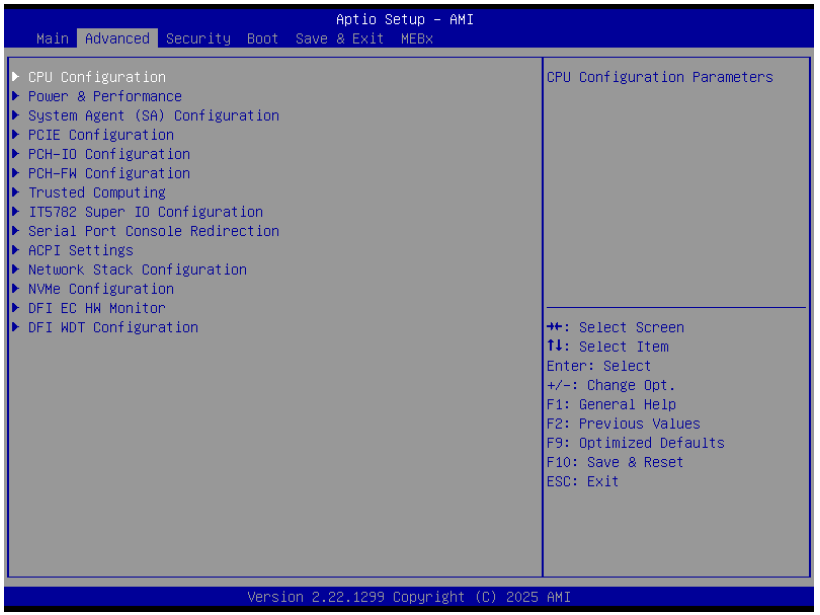
System Time

The time format is <hour>, <minute>, <second>. The time is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Hour displays hours from 00 to 23. Minute displays minutes from 00 to 59. Second displays seconds from 00 to 59.

▶ Advanced

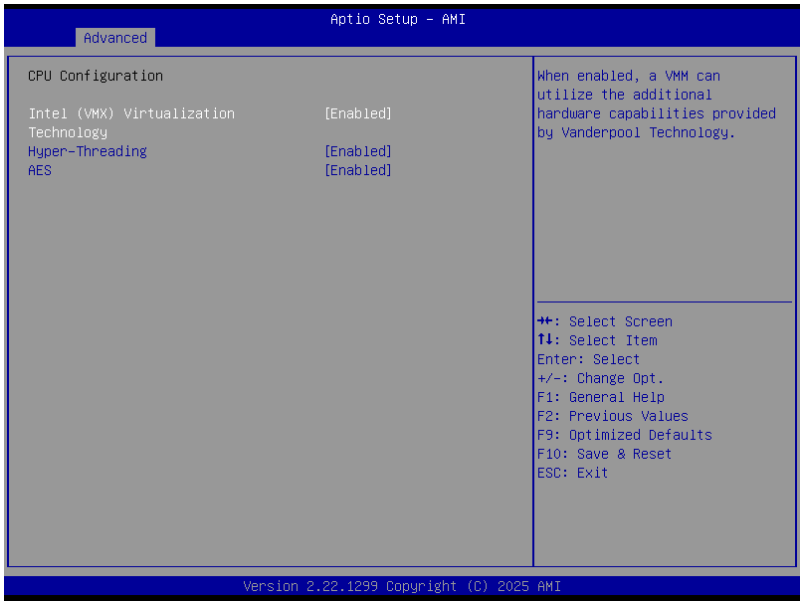
The Advanced menu allows you to configure your system for basic operation. Some entries are defaults required by the system board, while others, if enabled, will improve the performance of your system or let you set some features according to your preference.

Important:
Setting incorrect field values may cause the system to malfunction.



▶ Advanced

CPU Configuration



Intel (VMX) Virtualization Technology

When this field is set to Enabled, the VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

Hyper-threading

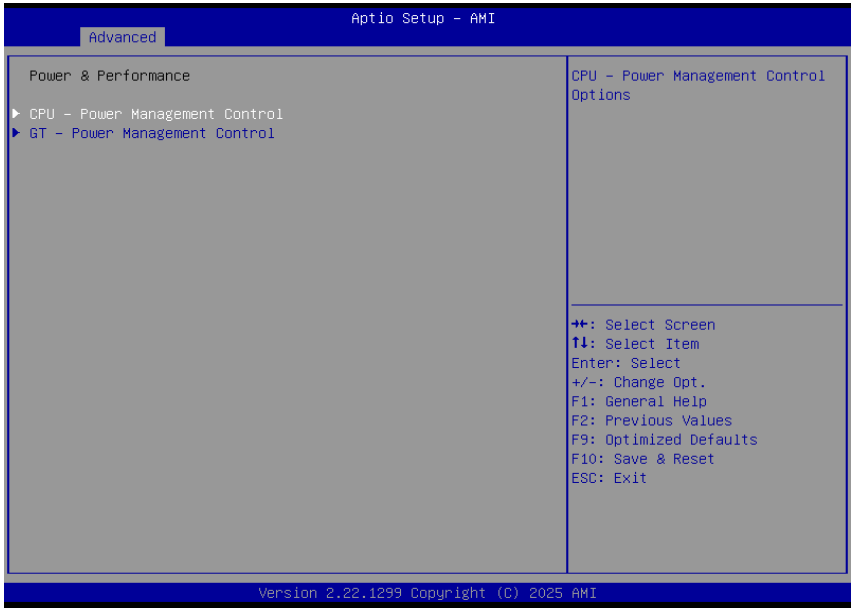
Enables this field for Windows XP and Linux which are optimized for Hyper-Threading technology. Select disabled for other OSes not optimized for Hyper-Threading technology. When disabled, only one thread per enabled core is enabled.

AES

Enable/Disable AES (Advanced Encryption Standard)

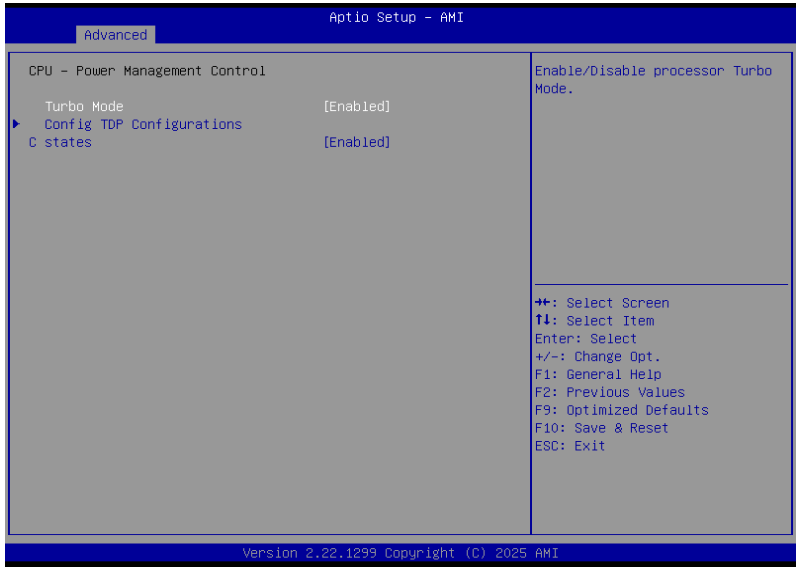
▶ Advanced

Power & Performance



▶ Advanced

Power & Performance ▶ CPU- Power Management Control



Turbo Mode

Enable or disable turbo mode of the processor. This field will only be displayed when EIST is enabled.

Config TDP Configurations

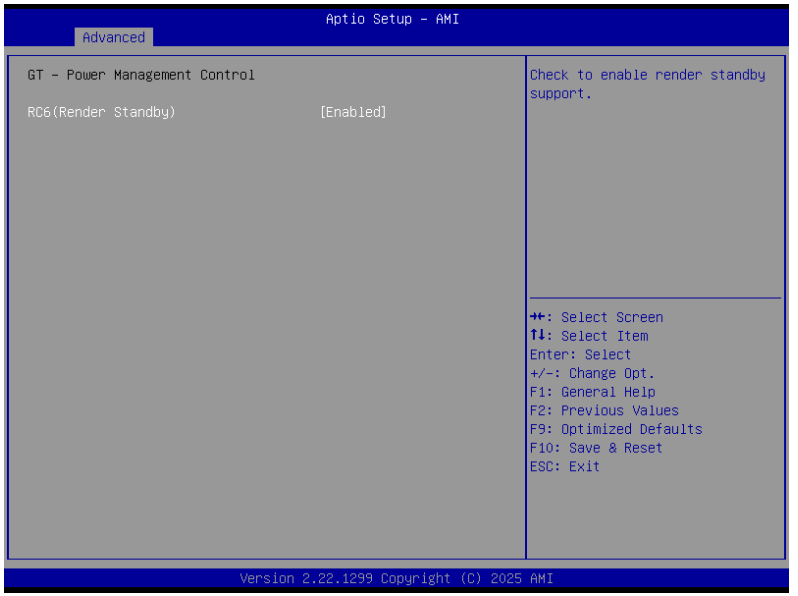
Configurable Processor Base Power (cTDP) configurations.

C states

Enable or disable CPU Power Management. It allows CPU to enter "C states" when it's not 100% utilized.

▶ Advanced

Power & Performance ▶ GT- Power Management Control

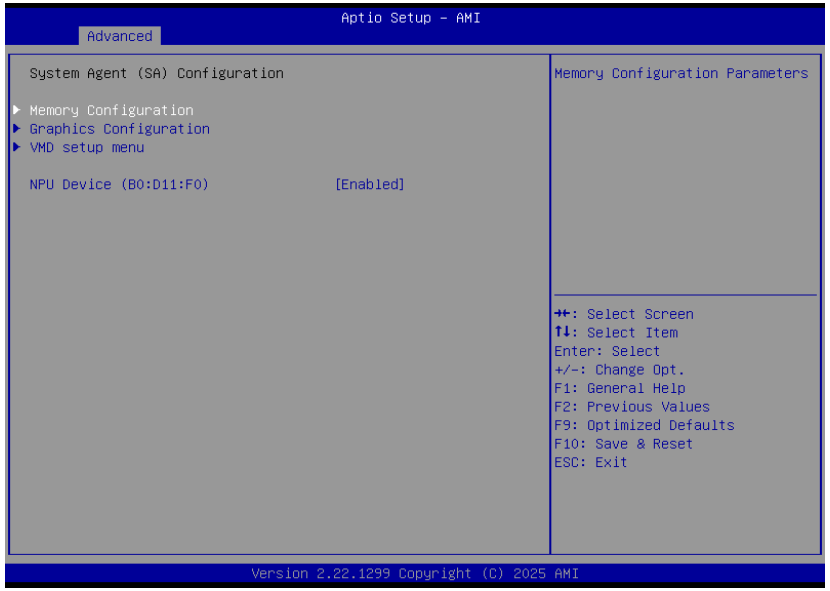


RC6 (Render Standby)

Check to enable render standby support.

▶ Advanced

System Agent (SA) Configuration



Memory Configuration

Memory Configuration Parameters.

Graphics Configuration

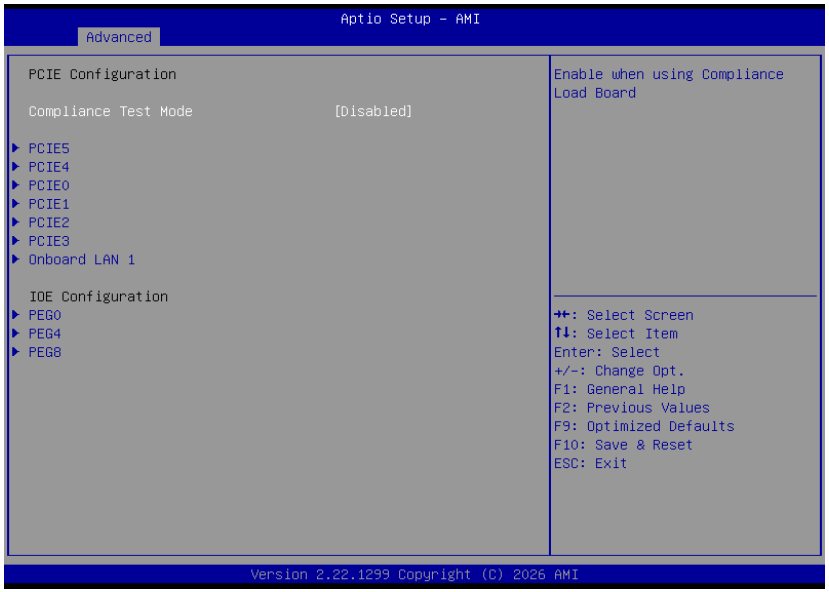
Settings about graphic.

VMD setup menu

VMD Configuration Settings

▶ Advanced

PCIE Configuration



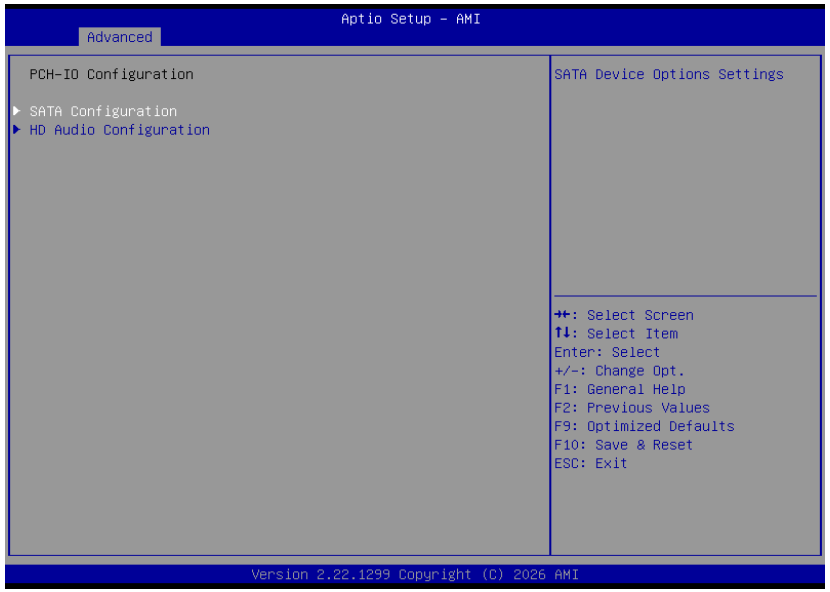
Select one of the PCI Express channels and press enter to configure the following settings.

PCIE 0, 1, 2, 3, 4, 5, & Onboard LAN1, **PEG0, 4, 8.**

Control the PCI Express Root Port.

▶ Advanced

PCH-IO Configuration



SATA Configuration

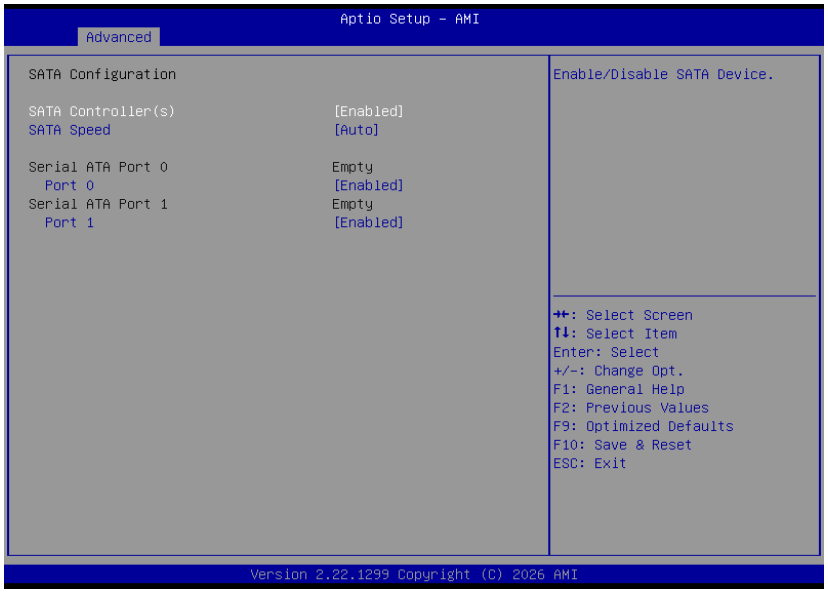
SATA Device Otpions Settings

HD Audio Configuration

HD Audio Subsystem Configuration Settings

▶ Advanced

PCH-IO Configuration▶ SATA Configuration



SATA Controller(s)

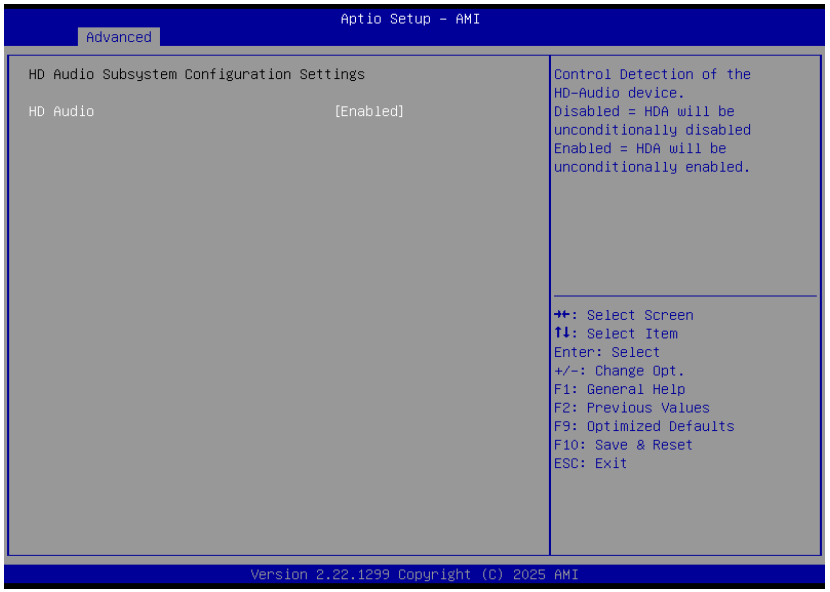
This field is used to enable or disable the Serial ATA controller.

SATA Speed

This field is used to select SATA speed generation limit: Auto, Gen1, Gen2 or Gen3.

▶ Advanced

PCH-IO Configuration▶ HD Audio Configuration



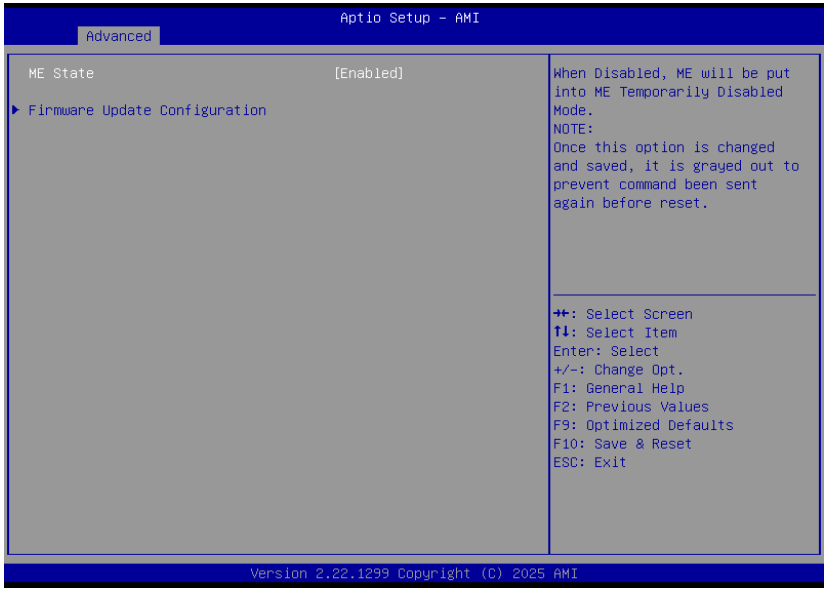
HD Audio

Control the detection of the HD Audio device.

- **Disabled** HDA will be unconditionally disabled.
- **Enabled** HDA will be unconditionally enabled.

▶ Advanced

PCH-FW Configuration



ME State

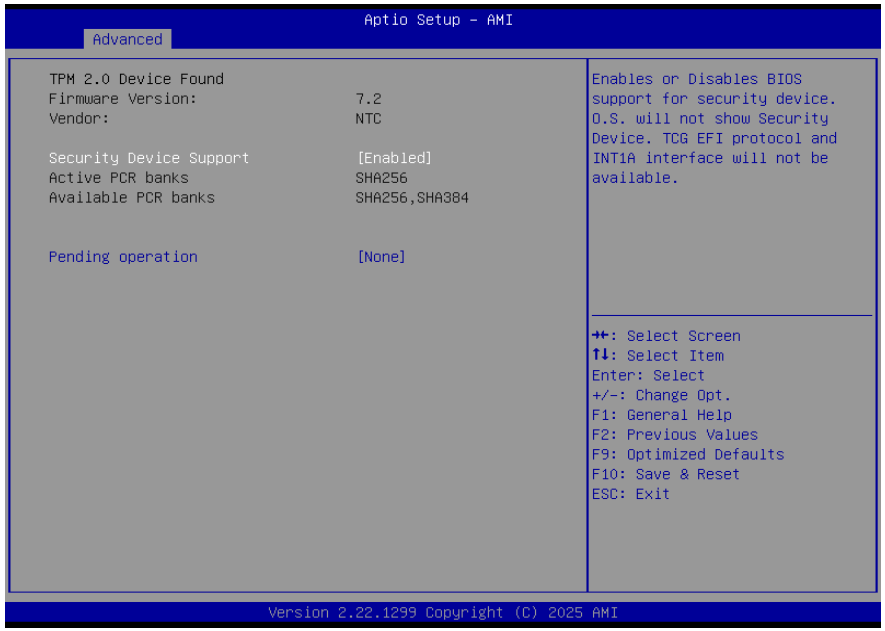
When this field is set to Disabled, ME will be put into ME Temporarily Disabled Mode.

Firmware Update Configuration

Configure Management Engine Technology Parameters.

Note:
The sub-menus are detailed in following sections.

Trusted Computing



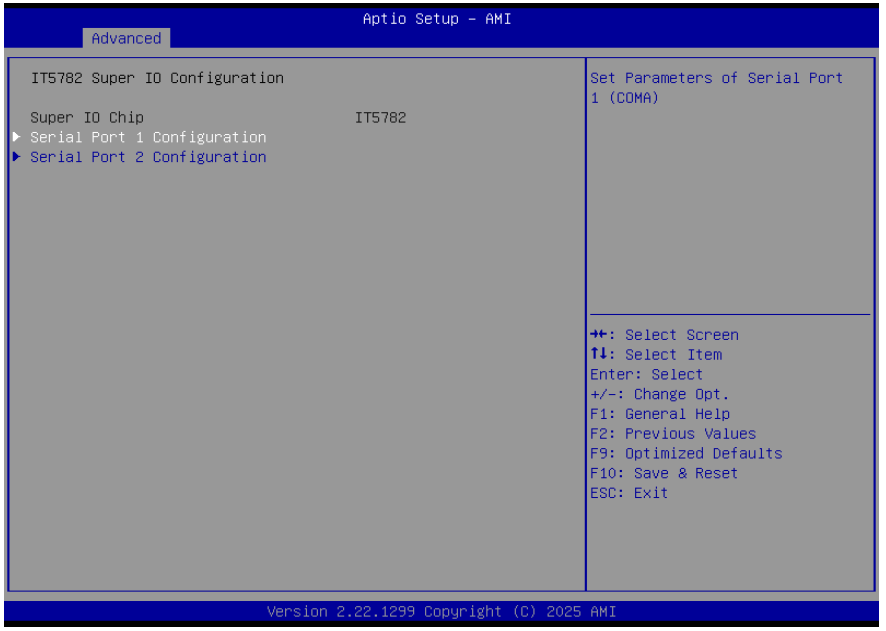
Security Device Support

This field is used to enable or disable BIOS support for the security device such as an TPM 2.0 to achieve hardware-level security via cryptographic keys.

Pending operation

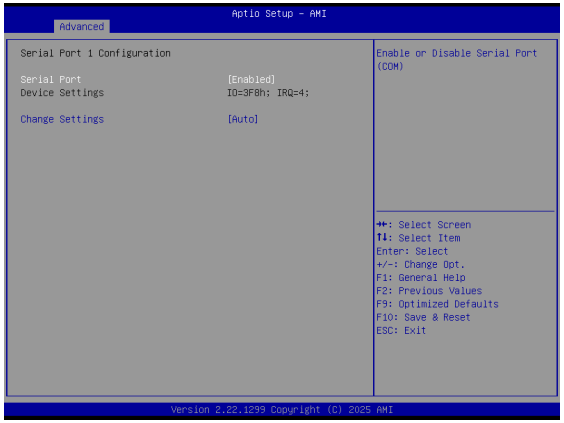
To clear the existing TPM encryption, select "TPM Clear" and restart the system. This field is not available when "Security Device Support" is disabled.

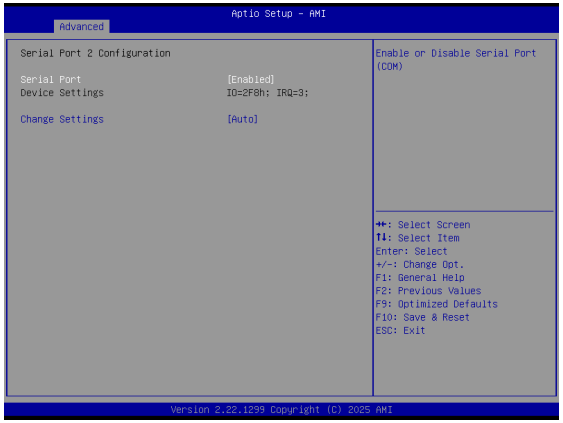
IT5782 Super IO Configuration



▶ Advanced

IT5782 Super IO Configuration ▶ Serial Port 1, 2 Configuration

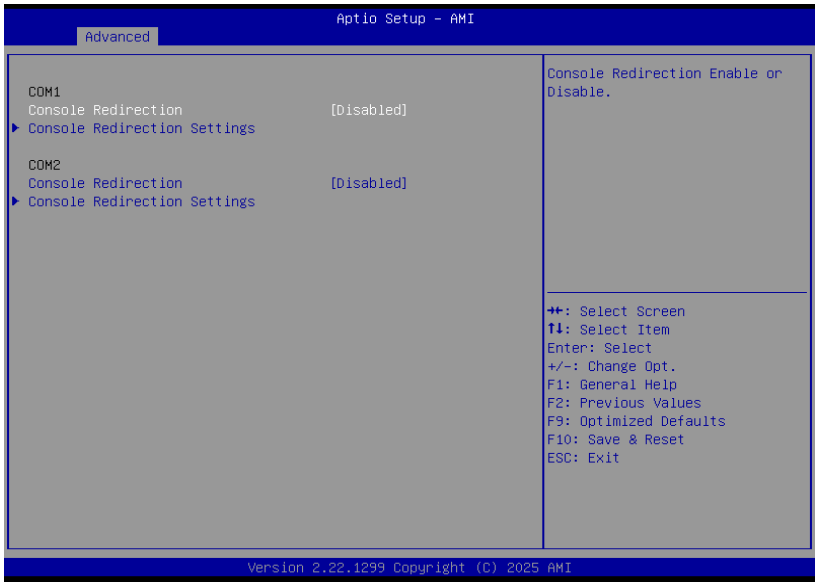




Serial Port
Enable or disable serial port.

▶ Advanced

Serial Port Console Redirection

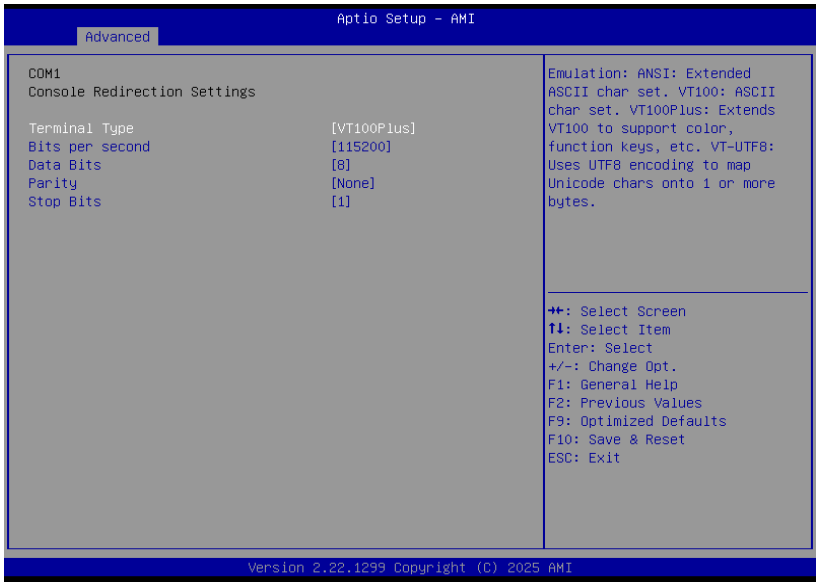


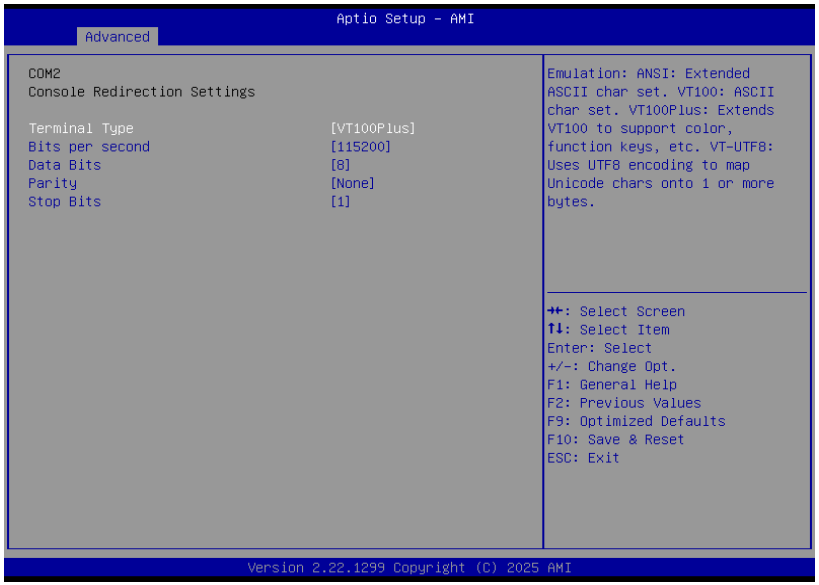
Console Redirection

By enabling Console Redirection of a COM port, the sub-menu of console redirection settings will become available for configuration as detailed in the following.

▶ Advanced

Serial Port Console Redirection ▶ Console Redirection Settings





Configure the serial settings of the current COM port.

Terminal Type

Select terminal type: VT100, VT100+, VT-UTF8 or ANSI.

Bits per second

Select serial port transmission speed: 9600, 19200, 38400, 57600 or 115200.

Data Bits

Select data bits: 7 bits or 8 bits.

Parity

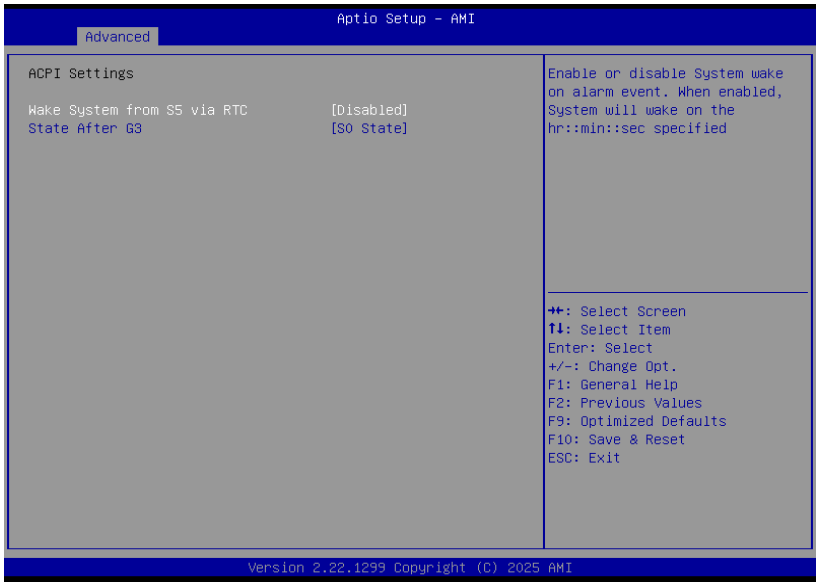
Select parity bits: None, Even, Odd, Mark or Space.

Stop Bits

Select stop bits: 1 bit or 2 bits.

▶ Advanced

ACPI Settings



Wake system from S5 via RTC

When Enabled, the system will automatically power up at a designated time every day. Once it's switched to [Enabled], please set up the time of day — hour, minute, and second — for the system to wake up.

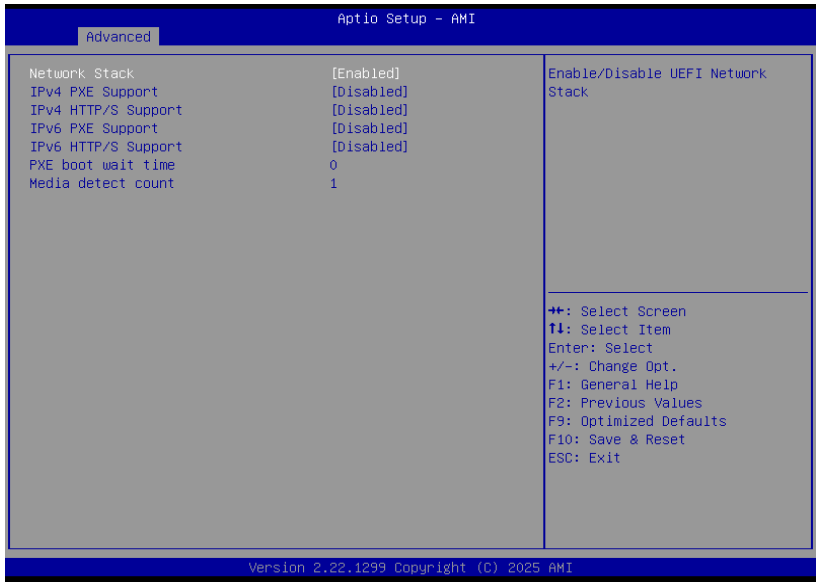
State After G3

Select between S0 State, and S5 State. This field is used to specify what state the system is set to return to when power is re-applied after a power failure (G3 state).

- **S0 State** The system automatically powers on after power failure.
- **S5 State** The system enter soft-off state after power failure. Power-on signal input is required to power up the system.

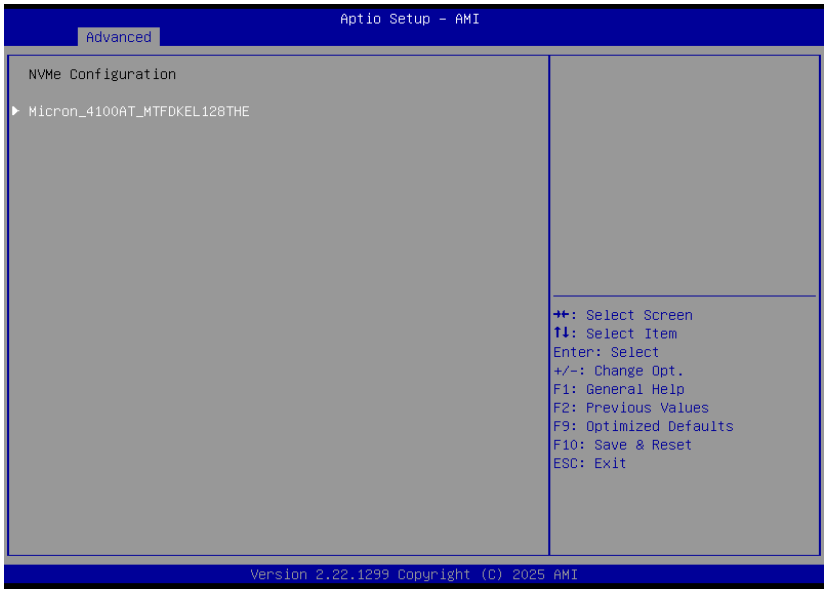
▶ Advanced

Network Stack Configuration



▶ Advanced

NVMe Configuration



Network Stack

Enable or disable UEFI network stack. The following fields will appear when this field is enabled.

Ipv4 PXE Support

Enable or disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.

Ipv4 HTTP Support / S Support

Enable or disable IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be avail-able.

Ipv6 PXE Support

Enable or disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.

Ipv6 HTTP Support/ S Support

Enable or disable IPv6 HTTP boot support. If disabled, IPv6 HTTP boot support will not be avail-able.

PXE boot wait time

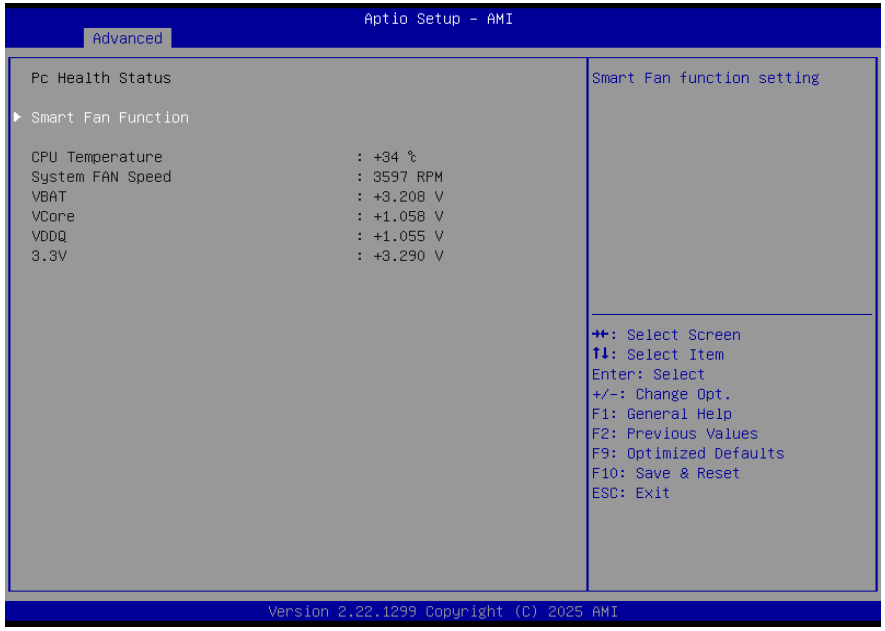
Set the wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.

Media detect count

Set the number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.

▶ Advanced

DFI EC HW Monitor



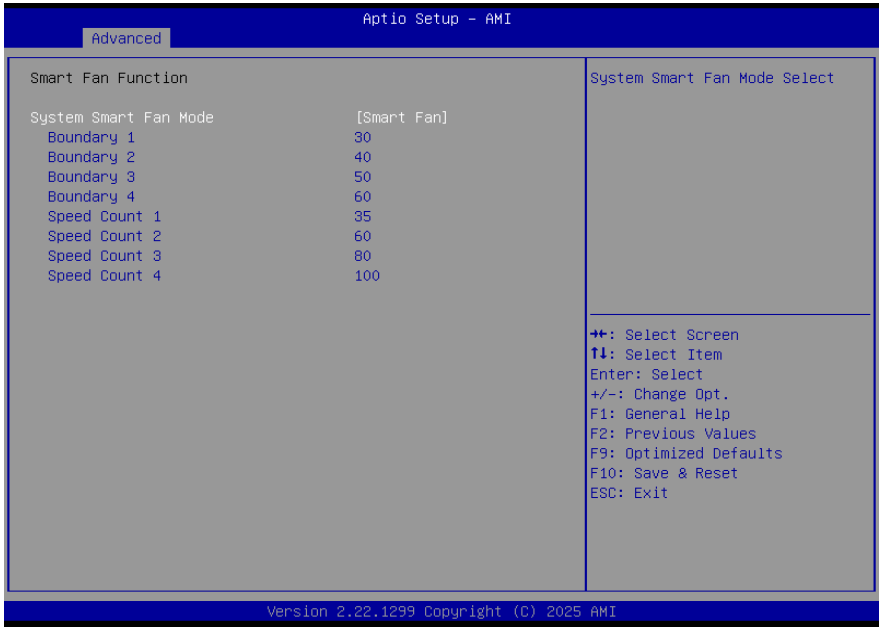
This section displays the system's health information, i.e. voltage readings, CPU and system temperatures, and fan speed readings

Smart Fan Function

Smart Fan Function Setting.

▶ Advanced

DFI EC HW Monitor ▶ Smart FAN Function



▼ SYS Smart Fan Mode = [Smart Fan]

Boundary 1 to Boundary 4

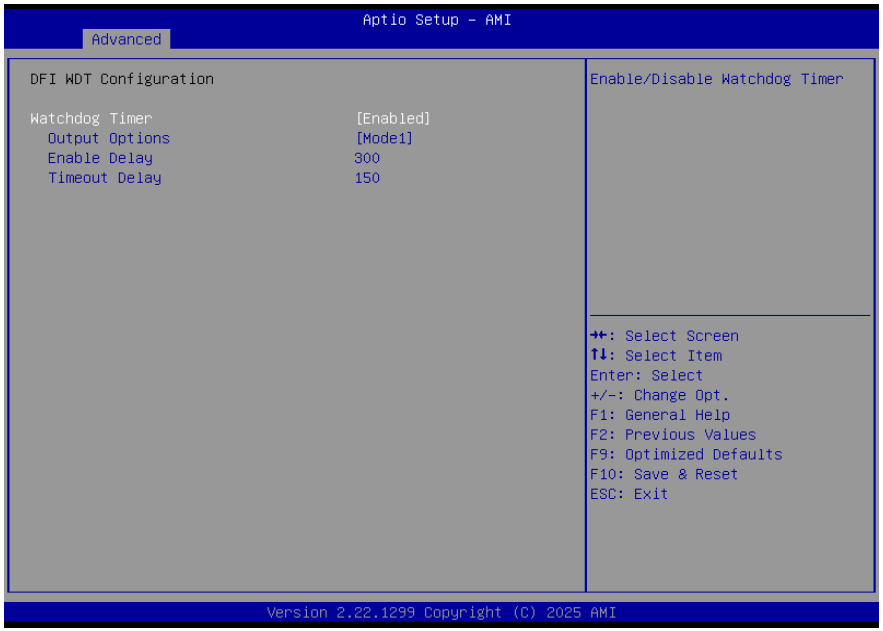
Set the boundary temperatures that determine the fan speeds accordingly, the value ranging from 0-127℃. For example, when the system temperature reaches Boundary 1 setting, the fan speed will be turned up to the designated speed of the Fan Speed Count 1 field.

Fan Speed Count 1 to Fan Speed Count 4

Set the fan speed, the value ranging from 1-100%, 100% being full speed. The fans will operate according to the specified boundary temperatures above-mentioned.

▶ Advanced

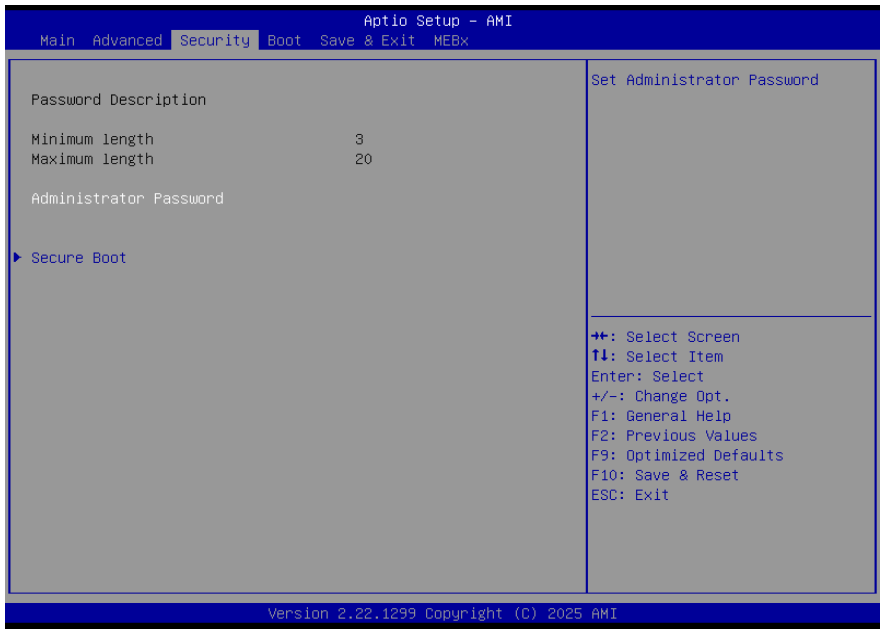
DFI WDT Configuration



Watchdog Timer

Enable or disable Watchdog Timer.

▶ Security



Administrator Password

Set the administrator password. To clear the password, input nothing and press enter when a new password is asked. Administrator Password will be required when entering the BIOS.

▶ Security

Secure Boot

Secure Boot

The Secure Boot store a database of certificates in the firmware and only allows the OSes with authorized signatures to boot on the system. To activate Secure Boot, please make sure that "Secure Boot" is "[Enabled]", Platform Key (PK) is enrolled, "System Mode" is "User", and CSM is disabled. After enabling/disabling Secure Boot, please save the configuration and restart the system. When configured and activated correctly, the Secure Boot status will be "Active".

Secure Boot Mode

Select the secure boot mode — Standard or Custom. When set to Custom, the following fields will be configurable for the user to manually modify the key database.

Restore Factory Keys

Force system to User Mode. Load OEM-defined factory defaults of keys and databases onto the Secure Boot. Press Enter and a prompt will show up for you to confirm.

Reset To Setup Mode

Clear the database from the NVRAM, including all the keys and signatures installed in the Key Management menu. Press Enter and a prompt will show up for you to confirm.

Expert Key Management

Enables expert users to modify Secure Boot Policy variables without full authentication.

▶ Boot

Setup Prompt Timeout

Set the number of seconds to wait for the setup activation key. 65535 (0xFFFF) denotes indefinite waiting.

Bootup NumLock State

Select the keyboard NumLock state: On or Off.

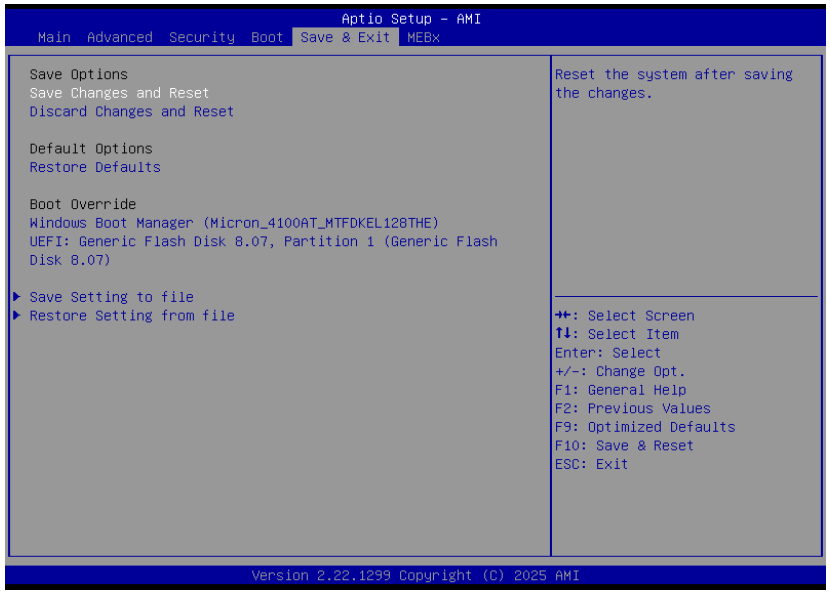
Quiet Boot

This section is used to enable or disable quiet boot option.

Boot Option Priorities

Rearrange the system boot order of available boot devices.

▶ Save & Exit



Save Changes and Reset

To save the changes, select this field and then press <Enter>. A dialog box will appear. Select Yes to reset the system after saving all changes made.

Discard Changes and Reset

To discard the changes, select this field and then press <Enter>. A dialog box will appear. Select Yes to reset the system setup without saving any changes.

Restore Defaults

To restore and load the optimized default values, select this field and then press <Enter>. A dia-log box will appear. Select Yes to restore the default values of all the setup options.

Boot Override

Move the cursor to an available boot device and press Enter, and then the system will immediately boot from the selected boot device. The Boot Override function will only be effective for the current boot. The “Boot Option Priorities” configured in the Boot menu will not be changed.

• **Save Setting to file** Select this option to save BIOS configuration settings to a USB flash device.

• **Restore Setting from file** This field will appear only when a USB flash device is detected. Select this field to restore set-ting from the USB flash device.

▶ MEBx

▶ Updating the BIOS

To update the BIOS, you will need the new BIOS file and a flash utility. Please contact technical support or your sales representative for the files and specific instructions about how to update BIOS with the flash utility.

▶ Notice: BIOS SPI ROM

- 1. The Intel® Management Engine has already been integrated into this system board. Due to the safety concerns, the BIOS (SPI ROM) chip cannot be removed from this system board and used on another system board of the same model.
- 2. The BIOS (SPI ROM) on this system board must be the original equipment from the factory and cannot be used to replace one which has been utilized on other system boards.
- 3. If you do not follow the methods above, the Intel® Management Engine will not be updated and will cease to be effective.

Note:

a. You can take advantage of flash tools to update the default configuration of the BIOS (SPI ROM) to the latest version anytime.

b. When the BIOS IC needs to be replaced, you have to populate it properly onto the system board after the EEPROM programmer has been burned and follow the technical person's instructions to confirm that the MAC address should be burned or not.

c. After updating unique MAC Address from manufacturing, NVM will be protected immediately after power cycle.
Users cannot update NVM or MAC address.