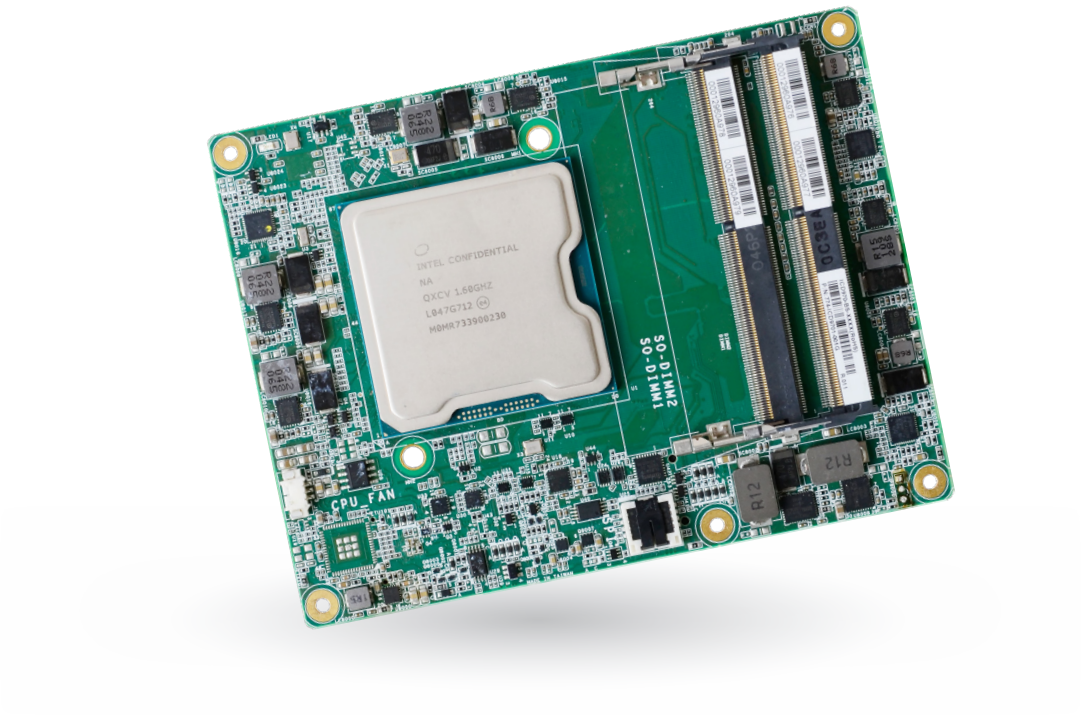
DFI



ICD970

COM Express Basic Module
User's Manual

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Changes after the publication's first release will be based on the product's revision. The website will always provide the most updated information.

Trademarks

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COM Express Specification Reference

PICMG® COM Express® Module Base Specification.
http://www.picmg.org/

FCC and DOC Statement on Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio TV technician for help.

Notice:

- The changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.
- Shielded interface cables must be used in order to comply with the emission limits.

Table of Contents

About this Manual

This manual can be downloaded from the website.

The manual is subject to change and update without notice, and may be based on editions that do not resemble your actual products. Please visit our website or contact our sales representatives for the latest editions.

Warranty

- Warranty does not cover damages or failures that occur from misuse of the product, inability to use the product, unauthorized replacement or alteration of components and product specifications.
- The warranty is void if the product has been subjected to physical abuse, improper installation, modification, accidents or unauthorized repair of the product.
- Unless otherwise instructed in this user's manual, the user may not, under any circumstances, attempt to perform service, adjustments or repairs on the product, whether in or out of warranty. It must be returned to the purchase point, factory or authorized service agency for all such work.
- We will not be liable for any indirect, special, incidental or consequential damages to the product that has been modified or altered.

Static Electricity Precautions

It is quite easy to inadvertently damage your PC, system board, components or devices even before installing them in your system unit. Static electrical discharge can damage computer components without causing any signs of physical damage. You must take extra care in handling them to ensure against electrostatic build-up.

- To prevent electrostatic build-up, leave the system board in its anti-static bag until you are ready to install it.
- Wear an antistatic wrist strap.
- Do all preparation work on a static-free surface.
- Hold the device only by its edges. Be careful not to touch any of the components, contacts or connections.
- Avoid touching the pins or contacts on all modules and connectors. Hold modules or connectors by their ends.

Important:
Electrostatic discharge (ESD) can damage your processor, disk drive and other components. Perform the upgrade instruction procedures described at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

Safety Measures

- To avoid damage to the system, use the correct AC input voltage range.
- To reduce the risk of electric shock, unplug the power cord before removing the system chassis cover for installation or servicing. After installation or servicing, cover the system chassis before plugging the power cord.

About the Package

The package contains the following items. If any of these items are missing or damaged, please contact your dealer or sales representative for assistance.

The accessories in the package may not come similar to the information listed below. This may differ in accordance with the sales region or models in which it was sold. For more information about the standard package in your region, please contact your dealer or sales representative.

- One ICD970 board

Optional Items

The board and accessories in the package may not come similar to the information listed above. This may differ in accordance with the sales region or models in which it was sold. For more information about the standard package in your region, please contact your dealer or sales representative.

Before Using the System Board

Before using the system board, prepare basic system components.
If you are installing the system board in a new system, you will need at least the following internal components.

- Storage devices such as hard disk drive, etc.

You will also need external system peripherals you intend to use which will normally include at least a keyboard, a mouse and a video display monitor.

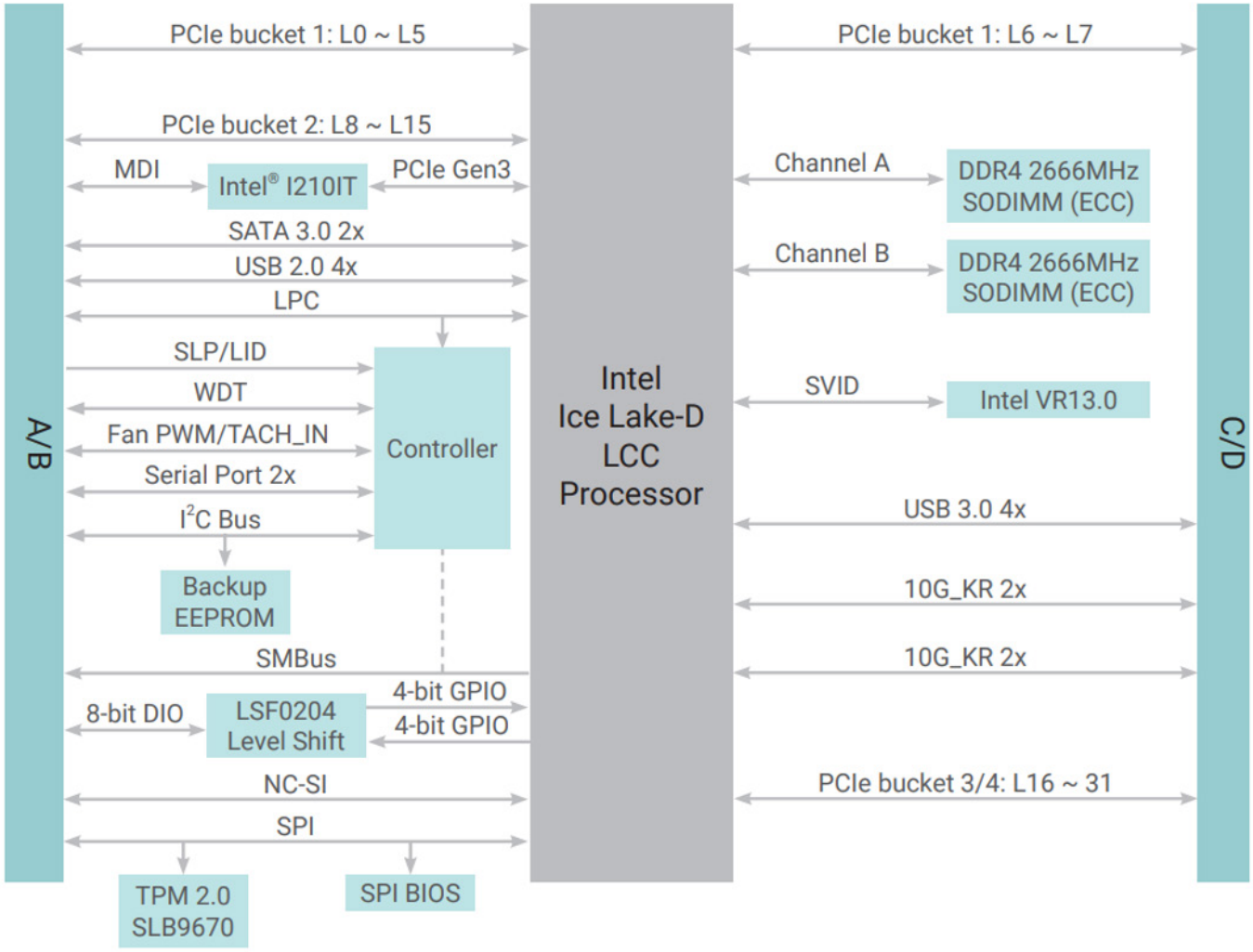
Chapter 1 - Introduction

▶ Specification

SYSTEM	Processor	3rd Gen Intel® Xeon® Scalable Processors D-1700 Family Intel® Xeon® D-1746TER Processor, 10 Cores, 15MB Cache, 2.0GHz, 67W Intel® Xeon® D-1735TR Processor, 8 Cores, 15MB Cache, 2.2GHz, 59W Intel® Xeon® D-1732TE Processor, 8 Cores, 15MB Cache, 1.9GHz, 52W Intel® Xeon® D-1715TER Processor, 4 Cores, 10MB Cache, 2.4GHz, 50W Intel® Xeon® D-1712TR Processor, 4 Cores, 10MB Cache, 2.0GHz, 40W
	Memory	Default 2 260-pin DDR4 2666 SO-DIMM, dual channel mode up to 64GB 3rd DIMM by request (SDPC mode by request to support DDR4 2933MHz)
	BIOS	Insyde SPI flash 512Mbit
EXPANSION	Interface	Default: B1: 1 x PCIe x8 or 2 x PCIe x4 or 4x PCIe x2 (Gen 3) B2: 1 x PCIe x8 or 2 x PCIe x4 or 4x PCIe x2 (Gen 3) B3/B4: 1 x PCIe x16 or 2 x PCIe x8 or 4x PCIe x4 (Gen 4)
		1 x LPC
		1 x I^2C
		1 x SMBus
		2 x UART (TX/RX)
ETHERNET	Controller	Supports up to 4 x 10GBASE-KR interfaces and max up to 4 x 10GbE MAC ports (maximum bandwidth 40Gb by activating the 4 x 10GbE at the same time) 1 x Intel® I210AT (10/100/1000Mbps) (0 to 60°C) or 1 x Intel® I210IT (10/100/1000Mbps) (-40 to 85°C)
I/O	USB	4 x USB 3.0 4 x USB 2.0 (USB 2.0 port 3 option, jumper-wire default to BMC)
	SATA	2 x SATA 3.0 (Up to 6Gb/s)
	DIO	1 x 8-bit DIO (Default 4 inputs and 4 outputs)
WATCHDOG TIMER	Output & Interval	System Reset, Programmable via Software from 1 to 255 Seconds
SECURITY	TPM	default TPM2.0, fTPM by request

Power	Type	12V, 5VSB, VCC_RTC (ATX mode) 12V, VCC_RTC (AT mode)
	Consumption	Typical: 71.36W Max: 72.36W
OS SUPPORT	OS Support	Windows Server 2019, 2022 Linux Ubuntu 20.04 CentOS 7.5
ENVIRONMENT	Temperature	Operating: 0 to 60°C, -40 to 85°C Storage: -40 to 85°C (Depends on SKU)
	Humidity	Operating: 5 to 90% RH Storage: 5 to 90% RH
	MTBF	277,731hrs @25°C 144,676hrs @45°C 81,589hrs @60°C 55,811hrs @70°C 37,526 @85°C Calculation model: Telcordia Issue 4 Environment: GB, GC – Ground Benign, Controlled
MECHANICAL	Dimensions	COM Express® Basic 95mm (3.74") x 125mm (4.9")
	Compliance	PICMG COM Express® R3.0, Type 7
STANDARDS AND CERTIFICATIONS	Certifications	CE, FCC, RoHS

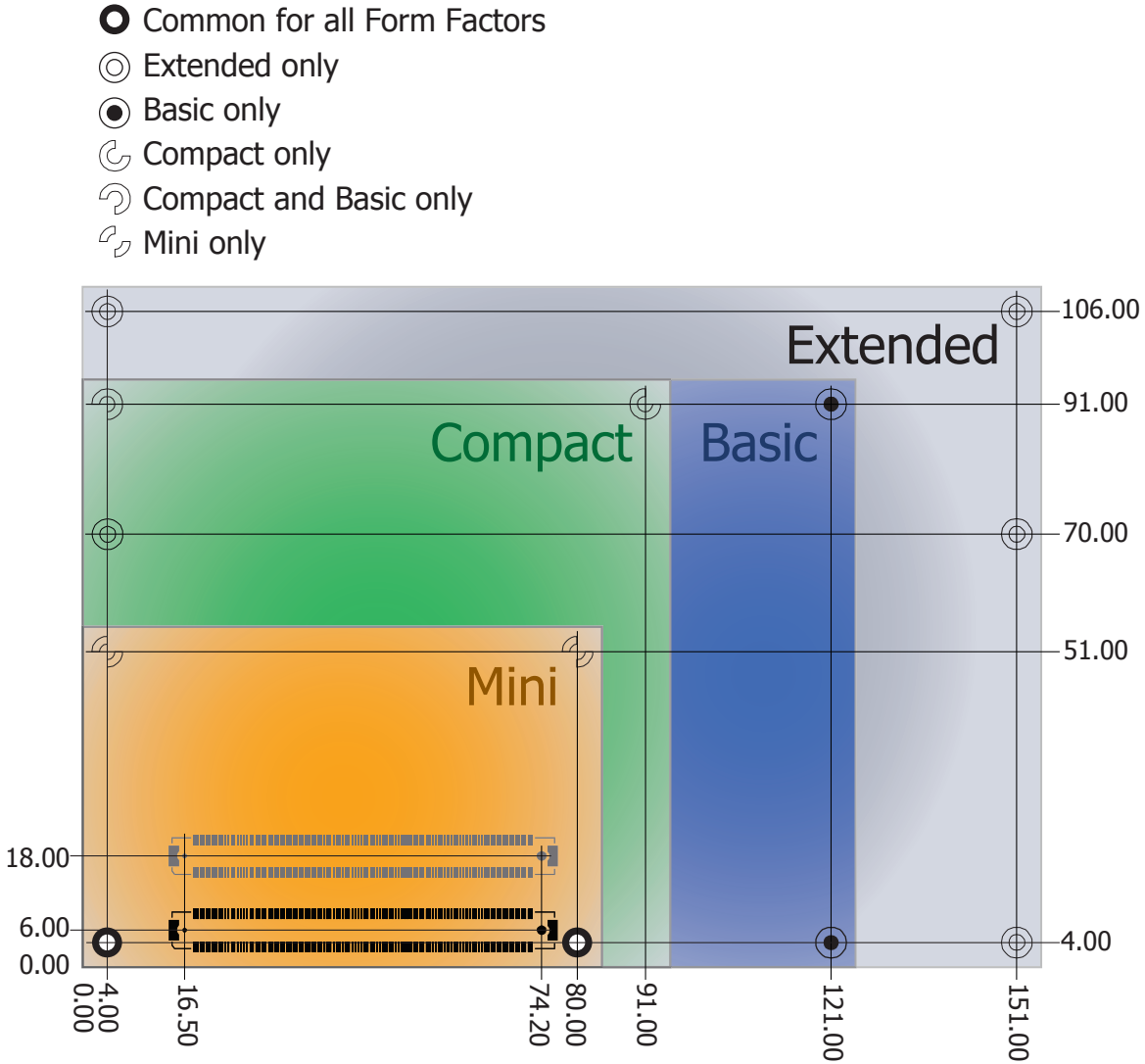
▶ Block Diagram



Chapter 2 - Concept

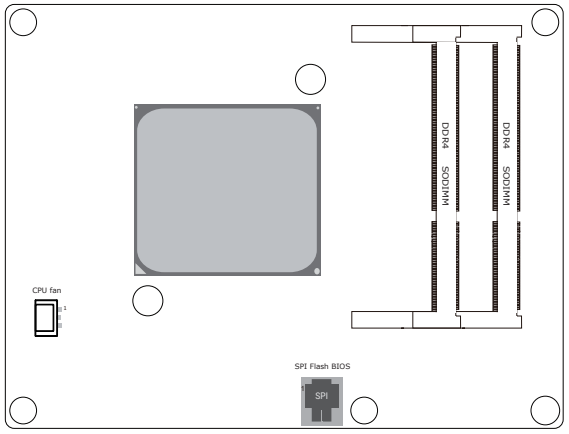
▶ COM Express Module Standards

The figure below shows the dimensions of the different types of COM Express modules.
ICD970 is a COM Express Basic. The dimension is 95mm x 125mm.

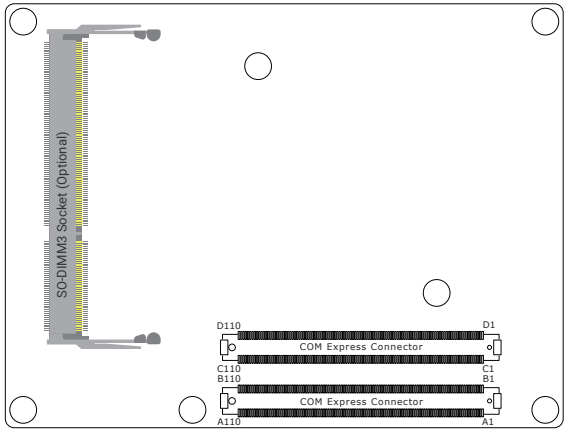


Chapter 3 - Hardware Installation

▶ Board Layout



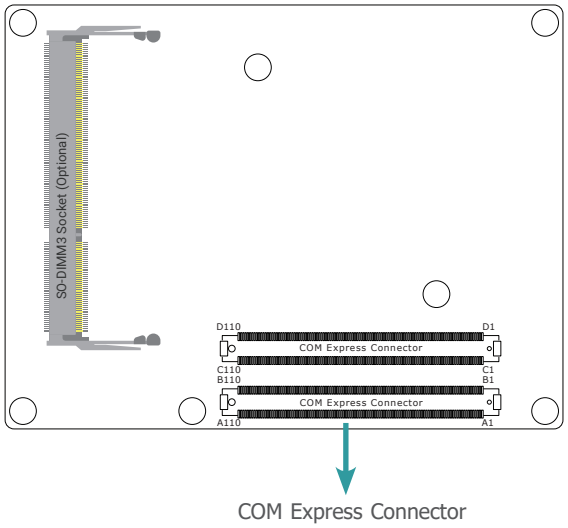
TOP VIEW



BOTTOM VIEW

▶ Connector

The COM Express connector is used to interface the ICD970 COM Express module board to a carrier board. Connect the COM Express connector (located on the solder side of the board) to the COM Express connector on the carrier board.Refer to the following pages for the pin functions of the connector.



The table below shows the COM Express standard specifications and the corresponding specifications supported on the ICD970 module.
Type 7 Based on Type 6. Modules trades all audio and video interfaces, 2 SATA ports and four USB 2.0 for additional PCI Express lanes, four 10 Gb Ethernet ports and an NC-SI management interface for the GbE port.

Connector	Feature	COM Express Module Base Specification Type 7 Min / Max	DFI ICD970 Type 7 (STD 000G/100G/200G)
• System I/O			
A-B	PCI Express Lanes 0 - 5	6 / 6	6
A-B , C-D	PCI Express Lanes 6 - 15	0 / 10	10
C-D	PCI Express Lanes 16 - 31	0 / 16	16
C-D	PCI Express Graphics (PEG)	NA	NA
C-D	10G LAN Ports 0 - 3	0 / 4	4
A-B	NC-SI	0 / 1	1
A-B	1Gb LAN Port 0	1 / 1	1
A-B	DDI 0	NA	NA
A-B	DDIs 1 - 3	NA	NA
A-B	LVDS Channel A	NA	NA
A-B	LVDS Channel B	NA	NA
A-B	eDP on LVDS CH A pins	NA	NA
A-B	VGA Port	NA	NA
A-B	Serial Ports 1 - 2	0 / 2	2
A-B	CAN interface on SER1	0 / 1	0
A-B	SATA Ports	0 / 2	2
A-B	HDA Digital Interface	NA	NA
A-B	USB 2.0 Ports	4 / 4	4
A-B	USB0 Client	0 / 1	0
A-B	USB7 Client	NA	NA
C-D	USB 3.0 Ports	0 / 4	4
A-B	LPC Bus or eSPI	1 / 1	1 LPC
A-B	SPI (Devices)	1 / 2	1
C-D	Rapid Shutdown	0 / 1	0 (to EC only)
• System Management			
A-B[6]	SDIO (muxed on GPIO)	0 / 1	0
A-B	General Purpose I/O	8 / 8	8
A-B	SMBus	1 / 1	1 (SOC Legacy SMBUS)
A-B	I2C	1 / 1	1 (SOC HDMA SMBUS)
A-B	Watchdog Timer	0 / 1	1
A-B	Speaker Out	1 / 1	1
A-B	Carrier Board BIOS Flash Support	0 / 1	1
A-B	Reset Functions	1 / 1	1
A-B	Trusted Platform Module	0 / 1	1
• Power Management			
A-B	Thermal Protection	0 / 1	1
A-B	Battery Low Alarm	0 / 1	1 (to SOC GPIO only)
A-B	Suspend/Wake Signals	0 / 3	2
A-B	Power Button Support	1 / 1	1
A-B	Power Good	1 / 1	1
A-B	VCC_5V_SBY Contacts	4 / 4	4
A-B[5]	Sleep Input	0 / 1	1 (SOC not support S3/ S4)
A-B[5]	Lid Input	0 / 1	1
A-B[5]	Carrier Board Fan Control	0 / 1	1
• Power			
A-B, C-D	VCC_12V Contacts	24 / 24	24

Note :
- A superscript five (5) indicates 12V-tolerant features on former VCC_12V signals.
- A superscript six (6) cells in the connected columns spanning rows provide a rough approximation of features sharing connector pins.

▶ COM Express Connector

The table below is a comprehensive list of all signal pins supported on the dual 220-pin COM Express connectors as defined for Type 7.
Signals described in the specification but not supported on the ICD970 are strikethrough.

Pin	Row A	ICD970 Difference	Row B	ICD970 Difference	Row C	ICD970 Difference	Row D	ICD970 Difference
1	GND(FIXED)		GND(FIXED)		GND(FIXED)		GND(FIXED)	
2	GBE0_MDI3-		GBE0_ACT#		GND		GND	
3	GBE0_MDI3+		LPC_FRAME#/ ~~ESPI_CS0#~~	LPC_FRAME#	USB_SSRX0-		USB_SSTX0-	
4	GBE0_LINK100#		LPC_AD0/~~ESPI_IO_0~~	LPC_AD0	USB_SSRX0+		USB_SSTX0+	
5	GBE0_LINK1000#		LPC_AD1/~~ESPI_IO_1~~	LPC_AD1	GND		GND	
6	GBE0_MDI2-		LPC_AD2/~~ESPI_IO_2~~	LPC_AD2	USB_SSRX1-		USB_SSTX1-	
7	GBE0_MDI2+		LPC_AD3/~~ESPI_IO_3~~	LPC_AD3	USB_SSRX1+		USB_SSTX1+	
8	GBE0_LINK#		LPC_DRQ0#/ ~~ESPI_ALERT0#~~	PU 10K	GND		GND	
9	GBE0_MDI1-		LPC_DRQ1#/ ~~ESPI_ALERT1#~~	PU 10K	USB_SSRX2-		USB_SSTX2-	
10	GBE0_MDI1+		LPC_CLK/~~ESPI_CK~~	LPC_CLK	USB_SSRX2+		USB_SSTX2+	
11	GND(FIXED)		GND(FIXED)		GND(FIXED)		GND(FIXED)	
12	GBE0_MDI0-		PWRBTN#		USB_SSRX3-		USB_SSTX3-	
13	GBE0_MDI0+		SMB_CK		USB_SSRX3+		USB_SSTX3+	
14	GBE0_CTREF	N.C.	SMB_DAT		GND		GND	
15	SUS_S3#		SMB_ALERT#		10G_PHY_MDC_SCL3		10G_PHY_MDIO_SDA3	
16	SATA0_TX+		SATA1_TX+		10G_PHY_MDC_SCL2		10G_PHY_MDIO_SDA2	
17	SATA0_TX-		SATA1_TX-		10G_SDP2		10G_SDP3	
18	SUS_S4#		SUS_STAT#/ ~~ESPI_RESET#~~	SUS_STAT#	GND		GND	
19	SATA0_RX+		SATA1_RX+		PCIE_RX6+		PCIE_TX6+	
20	SATA0_RX-		SATA1_RX-		PCIE_RX6-		PCIE_TX6-	
21	GND(FIXED)		GND(FIXED)		GND(FIXED)		GND(FIXED)	
22	PCIE_TX15+		PCIE_RX15+		PCIE_RX7+		PCIE_TX7+	
23	PCIE_TX15-		PCIE_RX15-		PCIE_RX7-		PCIE_TX7-	
24	SUS_S5#		PWR_OK		10G_INT2		10G_INT3	
25	PCIE_TX14+		PCIE_RX14+		GND		GND	
26	PCIE_TX14-		PCIE_RX14-		10G_KR_RX3+		10G_KR_TX3+	
27	BATLOW#		WDT		10G_KR_RX3-		10G_KR_TX3-	

Pin	Row A	ICD970 Difference	Row B	ICD970 Difference	Row C	ICD970 Difference	Row D	ICD970 Difference
28	(S)ATA_ACT#		RSVD		GND		GND	
29	RSVD	SOC_SMBPECI_CLK	RSVD	CLK_100M_G4PCIE_D0P	10G_KR_RX2+		10G_KR_TX2+	
30	RSVD	SOC_SMBPECI_DAT	RSVD	CLK_100M_G4PCIE_D0N	10G_KR_RX2-		10G_KR_TX2-	
31	GND(FIXED)		GND(FIXED)		GND(FIXED)		GND(FIXED)	
32	RSVD		SPKR		10G_SFP_SDA3		10G_SFP_SCL3	
33	RSVD		I2C_CK		10G_SFP_SDA2		10G_SFP_SCL2	
34	BIOS_DIS0#/ ~~ESPI_SAFS~~	BIOS_DIS0#	I2C_DAT		10G_PHY_RST_23	10G_O-PHY_RST0123#	10G_PHY_CAP_23	
35	THRMTRIP#		THRM#		10G_PHY_RST_01	10G_O-PHY_RST0123#	10G_PHY_CAP_01	
36	PCIE_TX13+		PCIE_RX13+		10G_LED_SDA		RSVD	
37	PCIE_TX13-		PCIE_RX13-		10G_LED_SCL		RSVD	
38	GND		GND		10G_SFP_SDA1		10G_SFP_SCL1	
39	PCIE_TX12+		PCIE_RX12+		10G_SFP_SDA0		10G_SFP_SCL0	
40	PCIE_TX12-		PCIE_RX12-		10G_SDP0		10G_SDP1	
41	GND(FIXED)		GND(FIXED)		GND(FIXED)		GND(FIXED)	
42	USB2-		USB3-		10G_KR_RX1+		10G_KR_TX1+	
43	USB2+		USB3+		10G_KR_RX1-		10G_KR_TX1-	
44	USB_2_3_OC#	USBOC_0123#	USB_0_1_OC#	USBOC_0123#	GND		GND	
45	USB0-		USB1-		10G_PHY_MDC_SCL1		10G_PHY_MDIO_SDA1	
46	USB0+		USB1+		10G_PHY_MDC_SCL0		10G_PHY_MDIO_SDA0	
47	VCC_RTC		ESPI_EN#		10G_INT0		10G_INT1	
48	RSVD		USB0_HOST_PRSNT	PD 47K	GND		GND	
49	GBE0_SDP		SYS_RESET#		10G_KR_RX0+		10G_KR_TX0+	
50	LPC_SERIRQ/ ~~ESPI_CS1#~~	LPC_SERIRQ#	CB_RESET#		10G_KR_RX0-		10G_KR_TX0-	
51	GND(FIXED)		GND(FIXED)		GND(FIXED)		GND(FIXED)	
52	PCIE_TX5+		PCIE_RX5+		PCIE_RX16+		PCIE_TX16+	
53	PCIE_TX5-		PCIE_RX5-		PCIE_RX16-		PCIE_TX16-	
54	GPI0		GPO1		TYPE0#	PD	RSVD	
55	PCIE_TX4+		PCIE_RX4+		PCIE_RX17+		PCIE_TX17+	
56	PCIE_TX4-		PCIE_RX4-		PCIE_RX17-		PCIE_TX17-	
57	GND		GPO2		TYPE1#	N.C.	TYPE2#	PD

Pin	Row A	ICD970 Difference	Row B	ICD970 Difference	Row C	ICD970 Difference	Row D	ICD970 Difference
58	PCIE_TX3+		PCIE_RX3+		PCIE_RX18+		PCIE_TX18+	
59	PCIE_TX3-		PCIE_RX3-		PCIE_RX18-		PCIE_TX18-	
60	GND(FIXED)		GND(FIXED)		GND(FIXED)		GND(FIXED)	
61	PCIE_TX2+		PCIE_RX2+		PCIE_RX19+		PCIE_TX19+	
62	PCIE_TX2-		PCIE_RX2-		PCIE_RX19-		PCIE_TX19-	
63	GPI1		GPO3		RSVD		RSVD	
64	PCIE_TX1+		PCIE_RX1+		RSVD		RSVD	
65	PCIE_TX1-		PCIE_RX1-		PCIE_RX20+		PCIE_TX20+	
66	GND		WAKE0#		PCIE_RX20-		PCIE_TX20-	
67	GPI2		WAKE1#		RAPID_SHUTDOWN		GND	
68	PCIE_TX0+		PCIE_RX0+		PCIE_RX21+		PCIE_TX21+	
69	PCIE_TX0-		PCIE_RX0-		PCIE_RX21-		PCIE_TX21-	
70	GND(FIXED)		GND(FIXED)		GND(FIXED)		GND(FIXED)	
71	PCIE_TX8+		PCIE_RX8+		PCIE_RX22+		PCIE_TX22+	
72	PCIE_TX8-		PCIE_RX8-		PCIE_RX22-		PCIE_TX22-	
73	GND		GND		GND		GND	
74	PCIE_TX9+		PCIE_RX9+		PCIE_RX23+		PCIE_TX23+	
75	PCIE_TX9-		PCIE_RX9-		PCIE_RX23-		PCIE_TX23-	
76	GND		GND		GND		GND	
77	PCIE_TX10+		PCIE_RX10+		RSVD		RSVD	
78	PCIE_TX10-		PCIE_RX10-		PCIE_RX24+		PCIE_TX24+	
79	GND		GND		PCIE_RX24-		PCIE_TX24-	
80	GND(FIXED)		GND(FIXED)		GND(FIXED)		GND(FIXED)	
81	PCIE_TX11+		PCIE_RX11+		PCIE_RX25+		PCIE_TX25+	
82	PCIE_TX11-		PCIE_RX11-		PCIE_RX25-		PCIE_TX25-	
83	GND		GND		RSVD		RSVD	
84	NCSI_TX_EN		VCC_5V_SBY		GND		GND	
85	GPI3		VCC_5V_SBY		PCIE_RX26+		PCIE_TX26+	
86	RSVD		VCC_5V_SBY		PCIE_RX26-		PCIE_TX26-	
87	RSVD		VCC_5V_SBY		GND		GND	

Pin	Row A	ICD970 Difference	Row B	ICD970 Difference	Row C	ICD970 Difference	Row D	ICD970 Difference
88	PCIE_CK_REF+		BIOS_DIS1#		PCIE_RX27+		PCIE_TX27+	
89	PCIE_CK_REF-		NCSI_RX_ER		PCIE_RX27-		PCIE_TX27-	
90	GND(FIXED)		GND(FIXED)		GND(FIXED)		GND(FIXED)	
91	SPI_POWER		NCSI_CLK_IN		PCIE_RX28+		PCIE_TX28+	
92	SPI_MISO		NCSI_RXD1		PCIE_RX28-		PCIE_TX28-	
93	GPO0		NCSI_RXD0		GND		GND	
94	SPI_CLK		NCSI_CRS_DV		PCIE_RX29+		PCIE_TX29+	
95	SPI_MOSI		NCSI_TXD1		PCIE_RX29-		PCIE_TX29-	
96	TPM_PP		NCSI_TXD0		GND		GND	
97	TYPE10#	N.C.	SPI_CS#		RSVD		RSVD	
98	SER0_TX		NCSI_ARB_IN		PCIE_RX30+		PCIE_TX30+	
99	SER0_RX		NCSI_ARB_OUT		PCIE_RX30-		PCIE_TX30-	
100	GND(FIXED)		GND(FIXED)		GND(FIXED)		GND(FIXED)	
101	SER1_TX		FAN_PWMOUT		PCIE_RX31+		PCIE_TX31+	
102	SER1_RX		FAN_TACHIN		PCIE_RX31-		PCIE_TX31-	
103	LID#		SLEEP#		GND		GND	
104	VCC_12V		VCC_12V		VCC_12V		VCC_12V	
105	VCC_12V		VCC_12V		VCC_12V		VCC_12V	
106	VCC_12V		VCC_12V		VCC_12V		VCC_12V	
107	VCC_12V		VCC_12V		VCC_12V		VCC_12V	
108	VCC_12V		VCC_12V		VCC_12V		VCC_12V	
109	VCC_12V		VCC_12V		VCC_12V		VCC_12V	
110	GND(FIXED)		GND(FIXED)		GND(FIXED)		GND(FIXED)	

▶ COM Express Connector Signal Description

Pin Types
I : Input to the Module
O : Output from the Module
I/O : Bi-directional input / output signal
OD : Open drain output
CMOS : Logic input or output. Input thresholds and output levels shall be 80% of supply rail for high side and 20% of the relevant supply rail for low side.
RSVD pins are reserved for future use and should be no connect. Do not tie the RSVD pins together.
Power Inputs used for power delivery to the Module electronics.
KR 10GBASE-KR compatible signal.

Gigabit Ethernet Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe Module PU/PD	ICD970 PU/PD	Module Base Specification R3.0
GBE0_MDI0+	A13	I/O Analog	3.3V max Suspend			Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. Some pairs are unused in some modes, per the following: 1000BASE-T / 100BASE-TX / 10BASE-T MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-
GBE0_MDI0-	A12	I/O Analog	3.3V max Suspend			
GBE0_MDI1+	A10	I/O Analog	3.3V max Suspend			
GBE0_MDI1-	A9	I/O Analog	3.3V max Suspend			
GBE0_MDI2+	A7	I/O Analog	3.3V max Suspend			
GBE0_MDI2-	A6	I/O Analog	3.3V max Suspend			
GBE0_MDI3+	A3	I/O Analog	3.3V max Suspend			
GBE0_MDI3-	A2	I/O Analog	3.3V max Suspend			
GBE0_ACT#	B2	OD CMOS	3.3V Suspend/3.3V		RSVD PU 10KΩ to 3V3DU	Gigabit Ethernet Controller 0 activity indicator, active low.
GBE0_LINK#	A8	OD CMOS	3.3V Suspend/3.3V		RSVD PU 10KΩ to 3V3DU	Gigabit Ethernet Controller 0 link indicator, active low.
GBE0_LINK100#	A4	OD CMOS	3.3V Suspend/3.3V		RSVD PU 10KΩ to 3V3DU	Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low.
GBE0_LINK1000#	A5	OD CMOS	3.3V Suspend/3.3V		RSVD PU 10KΩ to 3V3DU	Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.
GBE0_CTREF	A14	REF	GND min, 3.3V max		N.C.	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be limited to 250 mA or less.
GBE0_SDP	A49	I/O	3.3V Suspend/3.3V		RSVD PU 10KΩ	Gigabit Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1pps signal.

NC-SI Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe Module PU/PD	ICD970 PU/PD	Module Base Specification R3.0
NCSI_CLK_IN	B91	I CMOS	3.3V Suspend/3.3V	PD 10KΩ	PD 10KΩ to GND	NC-SI Clock reference for receive, transmit, and control interface.
NCSI_RXD0	B93	O CMOS	3.3V Suspend/3.3V		PD 3.3KΩ to GND	NC-SI Receive Data (from NC to BMC).
NCSI_RXD1	B92	O CMOS	3.3V Suspend/3.3V		PD 3.3KΩ to GND	NC-SI Receive Data (from NC to BMC).
NCSI_TXD0	B96	I CMOS	3.3V Suspend/3.3V	PD 10KΩ	PD 10KΩ to GND	NC-SI Transmit Data (from BMC to NC).
NCSI_TXD1	B95	I CMOS	3.3V Suspend/3.3V	PD 10KΩ	PD 10KΩ to GND	NC-SI Transmit Data (from BMC to NC).
NCSI_CRS_DV	B94	O CMOS	3.3V Suspend/3.3V		PD 10KΩ to GND	NC-SI Carrier Sense/Receive Data Valid to MC, indicating that the transmitted data from NC to BMC is valid.
NCSI_TX_EN	A84	I CMOS	3.3V Suspend/3.3V	PD 10KΩ	PD 10KΩ to GND	NC-SI Transmit enable.
NCSI_RX_ER	B89	O CMOS	3.3V Suspend/3.3V		PD 100KΩ to GND	NC-SI Receive error.
NCSI_ARB_IN	B98	I CMOS	3.3V Suspend/3.3V	PU 10KΩ	RSVD PU 1KΩ to 3.3V Suspend and PD 100KΩ	NC-SI hardware arbitration input.
NCSI_ARB_OUT	B99	O CMOS	3.3V Suspend/3.3V			NC-SI hardware arbitration output.

10Gb Ethernet Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe Module PU/PD	ICD970 PU/PD	Module Base Specification R3.0
10G_KR_TX0+	D49	O KR	AC coupled at receiver			10GBASE-KR ports, transmit output differential pairs. See section 'AC Coupling of 10G_KR_TX Signals' below for details on AC coupling
10G_KR_TX0-	D50	O KR	AC coupled at receiver			10GBASE-KR ports, transmit output differential pairs. See section 'AC Coupling of 10G_KR_TX Signals' below for details on AC coupling
10G_KR_TX1+	D42	O KR	AC coupled at receiver			10GBASE-KR ports, transmit output differential pairs. See section 'AC Coupling of 10G_KR_TX Signals' below for details on AC coupling
10G_KR_TX1-	D43	O KR	AC coupled at receiver			10GBASE-KR ports, transmit output differential pairs. See section 'AC Coupling of 10G_KR_TX Signals' below for details on AC coupling
10G_KR_TX2+	D29	O KR	AC coupled at receiver			10GBASE-KR ports, transmit output differential pairs. See section 'AC Coupling of 10G_KR_TX Signals' below for details on AC coupling
10G_KR_TX2-	D30	O KR	AC coupled at receiver			10GBASE-KR ports, transmit output differential pairs. See section 'AC Coupling of 10G_KR_TX Signals' below for details on AC coupling
10G_KR_TX3+	D26	O KR	AC coupled at receiver			10GBASE-KR ports, transmit output differential pairs. See section 'AC Coupling of 10G_KR_TX Signals' below for details on AC coupling
10G_KR_TX3-	D27	O KR	AC coupled at receiver			10GBASE-KR ports, transmit output differential pairs. See section 'AC Coupling of 10G_KR_TX Signals' below for details on AC coupling
10G_KR_RX0+	C49	I KR	AC coupled on Module		AC Coupling capacitor	10GBASE-KR ports, receive input differential pairs.
10G_KR_RX0-	C50	I KR	AC coupled on Module		AC Coupling capacitor	10GBASE-KR ports, receive input differential pairs.
10G_KR_RX1+	C42	I KR	AC coupled on Module		AC Coupling capacitor	10GBASE-KR ports, receive input differential pairs.
10G_KR_RX1-	C43	I KR	AC coupled on Module		AC Coupling capacitor	10GBASE-KR ports, receive input differential pairs.
10G_KR_RX2+	C29	I KR	AC coupled on Module		AC Coupling capacitor	10GBASE-KR ports, receive input differential pairs.
10G_KR_RX2-	C30	I KR	AC coupled on Module		AC Coupling capacitor	10GBASE-KR ports, receive input differential pairs.
10G_KR_RX3+	C26	I KR	AC coupled on Module		AC Coupling capacitor	10GBASE-KR ports, receive input differential pairs.
10G_KR_RX3-	C27	I KR	AC coupled on Module		AC Coupling capacitor	10GBASE-KR ports, receive input differential pairs.
10G_PHY_MDIO_SDA0	D46	O CMOS	3.3V Suspend/3.3V	I2C: PU 2.2KΩ	MDIO: PU 2.49KΩ to 3.3V Suspend I2C_SDA: PU 4.02K to 3.3V Suspend	**MDIO Mode:** Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY. **I2C Mode:** I2C data signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.
10G_PHY_MDIO_SDA1	D45					
10G_PHY_MDIO_SDA2	D16	I/O OD CMOS				
10G_PHY_MDIO_SDA3	D15					
10G_PHY_MDC_SCL0	C46	O CMOS	3.3V Suspend/3.3V	I2C: PU 2.2KΩ	MDC: PU 2.49KΩ to 3.3V Suspend I2C_SCL: PU 4.02K to 3.3V Suspend	**MDIO Mode:** Management Data I/O Interface mode clock signal for serial data transfers between the MAC and an external PHY. **I2C Mode:** I2C Clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.
10G_PHY_MDC_SCL1	C45					
10G_PHY_MDC_SCL2	C16	I/O OD CMOS				
10G_PHY_MDC_SCL3	C15					
10G_PHY_CAP_01	D35	I CMOS	3.3V Suspend/3.3V	PU 10KΩ	PU 10KΩ to 3.3V Suspend	Phy mode capability pin: Indicates if the PHY for 10G lanes 0 and 1 is capable of configuration by I²C. High indicates MDIO-only configuration, and low indicates configuration capability via I²C or MDIO. The actual protocol used for PHY configuration is determined by the module, in part based on this input. The actual protocol used is indicated over the dedicated I²C interface
10G_PHY_CAP_23	D34	I CMOS	3.3V Suspend/3.3V	PU 10KΩ	PU 10KΩ to 3.3V Suspend	Phy mode capability pin: Indicates if the PHY for 10G lanes 2 and 3 is capable of configuration by I²C. High indicates MDIO-only configuration, and low indicates configurationcapability via I²C or MDIO. The actual protocol used for PHY configuration is determined by the module, in part based on this input. The actual protocol used is indicated over the dedicated I²C interface
10G_SFP_SDA0	C39	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ	PU 4.02KΩ to 3.3V Suspend	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.
10G_SFP_SDA1	C38	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ	PU 2.49KΩ to 3.3V Suspend	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.
10G_SFP_SDA2	C33	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ	PU 3.01KΩ to 3.3V Suspend	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.
10G_SFP_SDA3	C32	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ	PU 3.01KΩ to 3.3V Suspend	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.

10G_SFP_SCL0	D39	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ	PU 4.02KΩ to 3.3V Suspend	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.
10G_SFP_SCL1	D38	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ	PU 2.49KΩ to 3.3V Suspend	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.
10G_SFP_SCL2	D33	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ	PU 3.01KΩ to 3.3V Suspend	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.
10G_SFP_SCL3	D32	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ	PU 3.01KΩ to 3.3V Suspend	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.
10G_LED_SDA	C36	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ	PU 2.2KΩ to 3.3V Suspend	I2C Data of the 2-wire interface that transfers LED signals and PHY straps for I2C or MDIO operation of optical PHYs. Refer to the details in I2C Data Mapping to Carrier Board Based PCA9539 I/O Expander.
10G_LED_SCL	C37	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ	PU 2.2KΩ to 3.3V Suspend	I2C Clock of the 2-wire interface that transfers LED and strap signals for I2C or MDIO operation of optical PHYs.
10G_INT0	C47	I CMOS	3.3V Suspend/3.3V	PU 2.2KΩ	PU 10KΩ to 3.3V Suspend	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller.
10G_INT1	D47	I CMOS	3.3V Suspend/3.3V	PU 2.2KΩ	PU 10KΩ to 3.3V Suspend	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller.
10G_INT2	C24	I CMOS	3.3V Suspend/3.3V	PU 2.2KΩ	PU 10KΩ to 3.3V Suspend	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller.
10G_INT3	D24	I CMOS	3.3V Suspend/3.3V	PU 2.2KΩ	PU 10KΩ to 3.3V Suspend	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller.
10G_SDP0	C40	I/O CMOS	3.3V Suspend/3.3V		PU 10KΩ to 3.3V Suspend	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal.
10G_SDP1	D40	I/O CMOS	3.3V Suspend/3.3V		PD 10KΩ to GND	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal.
10G_SDP2	C17	I/O CMOS	3.3V Suspend/3.3V		RSVD PU 10KΩ to 3.3V Suspend	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal.
10G_SDP3	D17	I/O CMOS	3.3V Suspend/3.3V		PU 10KΩ to 3.3V Suspend	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal.
10G_PHY_RST_01	C35	O CMOS	3.3V Suspend/3.3V		PD 20KΩ to GND	Output signal that resets an optical PHY on port 0 and port1 (with copper PHY this signal is not used).
10G_PHY_RST_23	C34	O CMOS	3.3V Suspend/3.3V		PD 20KΩ to GND	Output signal that resets an Optical PHY on port 2 and port 3 (with Copper PHY this signal is not used).

SATA Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe Module PU/PD	ICD970 PU/PD	Module Base Specification R3.0
SATA0_TX+	A16	O SATA	AC coupled on Module		AC Coupling capacitor	Serial ATA Channel 0 transmit differential pair.
SATA0_TX-	A17	O SATA	AC coupled on Module		AC Coupling capacitor	
SATA0_RX+	A19	I SATA	AC coupled on Module		AC Coupling capacitor	Serial ATA Channel 0 receive differential pair.
SATA0_RX-	A20	I SATA	AC coupled on Module		AC Coupling capacitor	
SATA1_TX+	B16	O SATA	AC coupled on Module		AC Coupling capacitor	Serial ATA Channel 1 transmit differential pair.
SATA1_TX-	B17	O SATA	AC coupled on Module		AC Coupling capacitor	
SATA1_RX+	B19	I SATA	AC coupled on Module		AC Coupling capacitor	Serial ATA Channel 1 receive differential pair.
SATA1_RX-	B20	I SATA	AC coupled on Module		AC Coupling capacitor	
(S)ATA_ACT#	A28	I/O CMOS	3.3V / 3.3V		AND Gate out, up to 3.3V	Serial ATA (activity indicator), active low.

General Purpose PCI Express Lanes Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe Module PU/PD	ICD970 PU/PD	Module Base Specification R3.0
PCIE_TX0+	A68	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 0
PCIE_TX0-	A69				AC Coupling capacitor	
PCIE_RX0+	B68	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 0
PCIE_RX0-	B69					
PCIE_TX1+	A64	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 1
PCIE_TX1-	A65				AC Coupling capacitor	
PCIE_RX1+	B64	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 1
PCIE_RX1-	B65					
PCIE_TX2+	A61	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 2
PCIE_TX2-	A62				AC Coupling capacitor	
PCIE_RX2+	B61	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 2
PCIE_RX2-	B62					
PCIE_TX3+	A58	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 3
PCIE_TX3-	A59				AC Coupling capacitor	
PCIE_RX3+	B58	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 3
PCIE_RX3-	B59					
PCIE_TX4+	A55	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 4
PCIE_TX4-	A56				AC Coupling capacitor	
PCIE_RX4+	B55	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 4
PCIE_RX4-	B56					
PCIE_TX5+	A52	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 5
PCIE_TX5-	A53				AC Coupling capacitor	
PCIE_RX5+	B52	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 5
PCIE_RX5-	B53					
PCIE_TX6+	D19	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 6
PCIE_TX6-	D20				AC Coupling capacitor	
PCIE_RX6+	C19	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 6
PCIE_RX6-	C20					
PCIE_TX7+	D22	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 7
PCIE_TX7-	D23				AC Coupling capacitor	
PCIE_RX7+	C22	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 7
PCIE_RX7-	C23					
PCIE_TX8+	A71	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 8
PCIE_TX8-	A72				AC Coupling capacitor	Different connector layout for Type 7
PCIE_RX8+	B71	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 8
PCIE_RX8-	B72					Different connector layout for Type 7
PCIE_TX9+	A74	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 9
PCIE_TX9-	A75				AC Coupling capacitor	Different connector layout for Type 7
PCIE_RX9+	B74	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 9
PCIE_RX9-	B75					Different connector layout for Type 7
PCIE_TX10+	A77	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 10
PCIE_TX10-	A78				AC Coupling capacitor	Different connector layout for Type 7
PCIE_RX10+	B77	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 10
PCIE_RX10-	B78					Different connector layout for Type 7
PCIE_TX11+	A81	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 11
PCIE_TX11-	A82				AC Coupling capacitor	Different connector layout for Type 7
PCIE_RX11+	B81	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 11
PCIE_RX11-	B82					Different connector layout for Type 7
PCIE_TX12+	A39	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 12
PCIE_TX12-	A40				AC Coupling capacitor	Different connector layout for Type 7
PCIE_RX12+	B39	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 12
PCIE_RX12-	B40					Different connector layout for Type 7
PCIE_TX13+	A36	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 13
PCIE_TX13-	A37				AC Coupling capacitor	Different connector layout for Type 7

PCIE_RX13+	B36	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 13
PCIE_RX13-	B37					Different connector layout for Type 7
PCIE_TX14+	A25	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 14
PCIE_TX14-	A26				AC Coupling capacitor	Different connector layout for Type 7
PCIE_RX14+	B25	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 14
PCIE_RX14-	B26					Different connector layout for Type 7
PCIE_TX15+	A22	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 15
PCIE_TX15-	A23				AC Coupling capacitor	Different connector layout for Type 7
PCIE_RX15+	B22	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 15
PCIE_RX15-	B23					Different connector layout for Type 7
PCIE_TX16+	D52	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 16
PCIE_TX16-	D53				AC Coupling capacitor	These are the same lines as Type 7 PEG_TX0±
PCIE_RX16+	C52	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 16
PCIE_RX16-	C53					These are the same lines as Type 7 PEG_RX0±
PCIE_TX17+	D55	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 17
PCIE_TX17-	D56				AC Coupling capacitor	These are the same lines as Type 7 PEG_TX1±
PCIE_RX17+	C55	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 17
PCIE_RX17-	C56					These are the same lines as Type 7 PEG_RX1±
PCIE_TX18+	D58	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 18
PCIE_TX18-	D59				AC Coupling capacitor	These are the same lines as Type 7 PEG_TX2±
PCIE_RX18+	C58	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 18
PCIE_RX18-	C59					These are the same lines as Type 7 PEG_RX2±
PCIE_TX19+	D61	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 19
PCIE_TX19-	D62				AC Coupling capacitor	These are the same lines as Type 7 PEG_TX3±
PCIE_RX19+	C61	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 19
PCIE_RX19-	C62					These are the same lines as Type 7 PEG_RX3±
PCIE_TX20+	D65	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 20
PCIE_TX20-	D66				AC Coupling capacitor	These are the same lines as Type 7 PEG_TX4±
PCIE_RX20+	C65	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 20
PCIE_RX20-	C66					These are the same lines as Type 7 PEG_RX4±
PCIE_TX21+	D68	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 21
PCIE_TX21-	D69				AC Coupling capacitor	These are the same lines as Type 7 PEG_TX5±
PCIE_RX21+	C68	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 21
PCIE_RX21-	C69					These are the same lines as Type 7 PEG_RX5±
PCIE_TX22+	D71	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 22
PCIE_TX22-	D72				AC Coupling capacitor	These are the same lines as Type 7 PEG_TX6±
PCIE_RX22+	C71	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 22
PCIE_RX22-	C72					These are the same lines as Type 7 PEG_RX6±
PCIE_TX23+	D74	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 23
PCIE_TX23-	D75				AC Coupling capacitor	These are the same lines as Type 7 PEG_TX7±
PCIE_RX23+	C74	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 23
PCIE_RX23-	C75					These are the same lines as Type 7 PEG_RX7±
PCIE_TX24+	D78	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 24
PCIE_TX24-	D79				AC Coupling capacitor	These are the same lines as Type 7 PEG_TX8±
PCIE_RX24+	C78	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 24
PCIE_RX24-	C79					These are the same lines as Type 7 PEG_RX8±
PCIE_TX25+	D81	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 25
PCIE_TX25-	D82				AC Coupling capacitor	These are the same lines as Type 7 PEG_TX9±
PCIE_RX25+	C81	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 25
PCIE_RX25-	C82					These are the same lines as Type 7 PEG_RX9±
PCIE_TX26+	D85	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 26
PCIE_TX26-	D86				AC Coupling capacitor	These are the same lines as Type 7 PEG_TX10±
PCIE_RX26+	C85	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 26
PCIE_RX26-	C86					These are the same lines as Type 7 PEG_RX10±
PCIE_TX27+	D88	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 27
PCIE_TX27-	D89				AC Coupling capacitor	These are the same lines as Type 7 PEG_TX11±
PCIE_RX27+	C88	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 27
PCIE_RX27-	C89					These are the same lines as Type 7 PEG_RX11±
PCIE_TX28+	D91	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 28
PCIE_TX28-	D92				AC Coupling capacitor	These are the same lines as Type 7 PEG_TX12±
PCIE_RX28+	C91	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 28
PCIE_RX28-	C92					These are the same lines as Type 7 PEG_RX12±
PCIE_TX29+	D94	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 29
PCIE_TX29-	D95				AC Coupling capacitor	These are the same lines as Type 7 PEG_TX13±

PCIE_RX29+	C94	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 29
PCIE_RX29-	C95					These are the same lines as Type 7 PEG_RX13±
PCIE_TX30+	D98	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 30
PCIE_TX30-	D99				AC Coupling capacitor	These are the same lines as Type 7 PEG_TX14±
PCIE_RX30+	C98	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 30
PCIE_RX30-	C99					These are the same lines as Type 7 PEG_RX14±
PCIE_TX31+	D101	O PCIE	AC coupled on Module		AC Coupling capacitor	PCI Express Differential Transmit Pairs 31
PCIE_TX31-	D102				AC Coupling capacitor	These are the same lines as Type 7 PEG_TX15±
PCIE_RX31+	C101	I PCIE	AC coupled off Module			PCI Express Differential Receive Pairs 31
PCIE_RX31-	C102					These are the same lines as Type 7 PEG_RX15±
PCIE_CLK_REF+	A88	O PCIE	PCIE			Reference clock output for all PCI Express and PCI Express Graphics lanes.
PCIE_CLK_REF-	A89					
RSVD (PCIE1_CK_REF+)	B29	O PCIE	PCIE		2nd PCIe Gen4 CLK+	Reserved pin.
RSVD (PCIE1_CK_REF-)	B30				2nd PCIe Gen4 CLK-	for COMe R3.1 new define with second reference clock output for higher speed PCI Express implementation on Lanes 16 to 31, for Type 7 implementations only,

USB Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe Module PU/PD	ICD970 PU/PD	Module Base Specification R3.0
USB0+	A46	I/O USB	3.3V Suspend/3.3V			USB differential pairs, channels 0. For type 7 only, USB0 may be configured as a USB client or as a host, or both at the Module designer's discretion. All other USB ports, if implemented, shall be host ports.
USB0-	A45					
USB1+	B46	I/O USB	3.3V Suspend/3.3V			USB differential pairs, channel 1.
USB1-	B45					
USB2+	A43	I/O USB	3.3V Suspend/3.3V			USB differential pairs, channel 2.
USB2-	A42					
USB3+	B43	I/O USB	3.3V Suspend/3.3V			USB differential pairs, channel 3.
USB3-	B42					
USB_0_1_OC#	B44	I CMOS	3.3V Suspend/3.3V	PU 10KΩ to 3.3V Suspend	PU 10KΩ to 3V3 Suspend.	USB over-current sense, USB channels 0 and 1. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_2_3_OC#	A44	I CMOS	3.3V Suspend/3.3V	PU 10KΩ to 3.3V Suspend	PU 10KΩ to 3V3 Suspend.	USB over-current sense, USB channels 2 and 3. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_SSTX0+	D4	O USB	AC coupled on Module		AC Coupling capacitor	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSTX0-	D3				AC Coupling capacitor	
USB_SSRX0+	C4	I USB	AC coupled off Module			Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSRX0-	C3					
USB_SSTX1+	D7	O USB	AC coupled on Module		AC Coupling capacitor	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSTX1-	D6				AC Coupling capacitor	
USB_SSRX1+	C7	I USB	AC coupled off Module			Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSRX1-	C6					
USB_SSTX2+	D10	O USB	AC coupled on Module		AC Coupling capacitor	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSTX2-	D9				AC Coupling capacitor	
USB_SSRX2+	C10	I USB	AC coupled off Module			Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSRX2-	C9					
USB_SSTX3+	D13	O USB	AC coupled on Module		AC Coupling capacitor	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSTX3-	D12				AC Coupling capacitor	
USB_SSRX3+	C13	I USB	AC coupled off Module			Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSRX3-	C12					
USB0_HOST_PRSNT	B48	I COMS	3.3V Suspend/3.3V		PD 47KΩ to GND	Module USB client may detect the presence of a USB host on USB0. A high value indicates that a host is present.

LPC and eSPI Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe Module PU/PD	ICD970 PU/PD **(LPC mode)**	Module Base Specification R3.0
LPC_AD0 / ESPI_IO_0	B4	I/O CMOS	3.3V / 3.3V 1.8V Suspend / 1.8V		not support ESPI mode.	**LPC Mode:** LPC multiplexed address, command and data bus. **ESPI Mode:** eSPI Master Data Input / Outputs These are bi-directional input/output pins used to transfer data between master and slaves.
LPC_AD1 / ESPI_IO_1	B5				not support ESPI mode.	
LPC_AD2 / ESPI_IO_2	B6				not support ESPI mode.	
LPC_AD3 / ESPI_IO_3	B7				not support ESPI mode.	
LPC_FRAME# / ESPI_CS0#	B3	O CMOS	3.3V / 3.3V 1.8V Suspend / 1.8V		not support ESPI mode.	**LPC Mode:** LPC frame indicates the start of an LPC cycle **ESPI Mode**: eSPI Master Chip Select Outputs Driving Chip Select0#. A lowselects a particular eSPI slave for the transaction. Each of the eSPI slaves is connected to a dedicated Chip Selectn# pin.
LPC_DRQ0# / ESPI_ALERT0#	B8	I CMOS	3.3V / 3.3V 1.8V Suspend / 1.8V	ESPI mode: PU 1KΩ	PU 10KΩ to 3.3V, not support ESPI mode.	**LPC Mode:** LPC serial DMA request **ESPI Mode:** eSPI pins used by eSPI slave to request service from the eSPI master.
LPC_DRQ1# / ESPI_ARERT1#	B9			ESPI mode: PU 1KΩ	PU 10KΩ to 3.3V, not support ESPI mode.	
LPC_SERIRQ / ESPI_CS1#	A50	I/O CMOS O CMOS	3.3V / 3.3V 1.8V Suspend / 1.8V	LPC_SERIRQ : PU 8.2KΩ	PU 10KΩ to 3.3V not support ESPI mode.	**LPC Mode:** LPC serial interrupt **ESPI Mode**: eSPI Master Chip Select Outputs Driving Chip Select# A low selects a particular eSPI slave for the transaction. Each of the eSPI slaves is connected to a dedicated Chip Selectn# pin.
LPC_CLK / ESPI_CK	B10	O CMOS	3.3V / 3.3V 1.8V Suspend / 1.8V	ESPI_CK : series 33Ω resistor	series 33Ω resistor not support ESPI mode.	**LPC Mode:** LPC clock output - 33MHz nominal **ESPI Mode:** eSPI Master Clock Output This pin provides the reference timing for all the serial input and output operations.
SUS_STAT# / ESPI_RESET#	B18	O CMOS	3.3V Suspend / 3.3V 1.8V Suspend / 1.8V		PD 10KΩ to GND and series AND Gate to BTB pin. not support ESPI mode.	**LPC Mode:** SUS_STAT# indicates imminent suspend operation. It is used to notify LPC devices that a low power state will be entered soon. LPC devices may need to preserve memory or isolate outputs during the low power state. **ESPI Mode:** eSPI Reset, Reset the eSPI interface for both master and slaves. eSPI Reset# is typically driven from eSPI master to eSPI slaves.
ESPI_EN#	B47	I CMOS	NA	PU 20KΩ to logic high.	PU 20KΩ to 3V3 Suspend and series diode to BTB pin.	This signal is used by the Carrier to indicate the operating mode of the LPC/eSPI bus. If left unconnected on the carrier, LPC mode (default) is selected. If pulled to GND on the carrier, eSPI mode is selected. This signal is pulled to a logic high on the module through a resistor. The Carrier should only float this line or pull it low.
BIOS_DIS0#	A34	I CMOS	NA	PU 10KΩ	PU 10KΩ to 3V3 Suspend.	Selection straps to determine the BIOS boot device. The Carrier should only float these or pull them low, please refer to 4.13 for strapping options of BIOS disable signals.
BIOS_DIS1#	B88			PU 10KΩ	PU 10KΩ to 3V3 Suspend.	

SPI Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe Module PU/PD	ICD970 (SPI_3VDU) PU/PD	Module Base Specification R3.0
SPI_CS#	B97	O CMOS	3.3V Suspend / 3.3V 1.8V Suspend / 3.3V		PU 10KΩ to 3V3 Suspend.	Chip select for Carrier Board SPI - may be sourced from chipset SPI0 or SPI1
SPI_MISO	A92	I CMOS	3.3V Suspend / 3.3V 1.8V Suspend / 3.3V	Series resistor 33Ω	PU 10KΩ to 3V3 Suspend and series resistor 33Ω	Data in to Module from Carrier SPI
SPI_MOSI	A95	O CMOS	3.3V Suspend / 3.3V 1.8V Suspend / 3.3V		PU 10KΩ to 3V3 Suspend.	Data out from Module to Carrier SPI
SPI_CLK	A94	O CMOS	3.3V Suspend / 3.3V 1.8V Suspend / 3.3V		PU 10KΩ to 3V3 Suspend.	Clock from Module to Carrier SPI
SPI_POWER	A91	O	3.3V Suspend / 3.3V 1.8V Suspend / 3.3V			Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier Board.

General Purpose Serial Interface Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe Module PU/PD	ICD970 PU/PD	Module Base Specification R3.0
SER0_TX	A98	O CMOS-T	3.3V/12V		Isolate by Diode	General purpose serial port 0 transmitter
SER0_RX	A99	I CMOS-T	3.3V/12V		PU 10KΩ to 3.3V & isolate by Diode	General purpose serial port 0 receiver
SER1_TX / CAN_TX	A101	O CMOS-T	3.3V/12V		Isolate by Diode	General purpose serial port 1 transmitter CAN(Controller Area Network) TX output for CAN Bus channel 0.
SER1_RX / CAN_RX	A102	I CMOS-T	3.3V/12V		PU 10KΩ to 3.3V & isolate by Diode	General purpose serial port 1 receiver CAN(Controller Area Network) RX input for CAN Bus channel 0.

Note: These signals use reclaimed VCC_12V pins. Refer to Section 5.8 'Protecting COM.0 Pins Reclaimed from the VCC_12V Pool' for additional design considerations.

I2C Signal Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe Module PU/PD	ICD970 PU/PD	Module Base Specification R3.0
I2C_CK	B33	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	PU 2.2KΩ to 3.3V Suspend	General purpose I2C port clock output
I2C_DAT	B34	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	PU 2.2KΩ to 3.3V Suspend	General purpose I2C port data I/O line

Miscellaneous Signal Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe Module PU/PD	ICD970 PU/PD	Module Base Specification R3.0
SPKR	B32	O CMOS	3.3V / 3.3V			Output for audio enunciator - the "speaker" in PC-AT systems. This port provides the PC beep signal and is mostly intended for debugging purposes.
WDT	B27	O CMOS	3.3V / 3.3V		PD 100KΩ to GND.	Output indicating that a watchdog time-out event has occurred.
FAN_PWMOUT	B101	O OD CMOS	3.3V / 12V		RSV PD 100KΩ to GND	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.
FAN_TACHIN	B102	I OD CMOS	3.3V / 12V	PU 47KΩ to 3.3V	PU 47KΩ to 3.3V	Fan tachometer input for a fan with a two pulse output.
TPM_PP	A96	I CMOS	3.3V / 3.3V	PD to GND.	PD 100KΩ to GND.	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.

Power and System Management Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe Module PU/PD	ICD970 PU/PD	Module Base Specification R3.0
PWRBTN#	B12	I CMOS	3.3V Suspend/3.3V	PU 10KΩ to 3.3V Suspend	PU 10KΩ to 3.3V Suspend	A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off and other suspend states, as well as powering the system down.
SYS_RESET#	B49	I CMOS	3.3V Suspend/3.3V	PU 10KΩ to 3.3V Suspend	PU 10KΩ to 3.3V Suspend	Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used.
CB_RESET#	B50	O CMOS	3.3V Suspend/3.3V		PD 100KΩ to GND	Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software.
PWR_OK	B24	I CMOS	3.3V / 3.3V	PU to 3.3V	PU 10KΩ to 5V with PD 20KΩ that divide to 3.3V then plus series diode to BTB pin.	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGAs or other configurable devices time to be programmed.
SUS_STAT#	B18	O CMOS	3.3V Suspend / 3.3V		PD 10KΩ to GND and series AND Gate to BTB pin. not support ESPI mode.	Indicates imminent suspend operation; used to notify LPC devices. Not used in eSPI implementations.
SUS_S3#	A15	O CMOS	3.3V Suspend/3.3V		PD 100KΩ to GND	Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board may be used to enable the non-standby power on a typical ATX supply.
SUS_S4#	A18	O CMOS	3.3V Suspend/3.3V		PD 100KΩ to GND	Indicates system is in Suspend to Disk state. Active low output.
SUS_S5#	A24	O CMOS	3.3V Suspend/3.3V		PD 100KΩ to GND	Indicates system is in Soft Off state.
WAKE0#	B66	I CMOS	3.3V Suspend/3.3V	PU 10KΩ to 3.3V Suspend	PU 2.2KΩ to 3.3V Suspend	PCI Express wake up signal.
WAKE1#	B67	I CMOS	3.3V Suspend/3.3V	PU 10KΩ to 3.3V Suspend		General purpose wake up signal. May be used to implement wake-up on PS2 keyboard or mouse activity.
BATLOW#	A27	I CMOS	3.3V Suspend/ 3.3V	PU 10KΩ to 3.3V Suspend	PU 10KΩ to 3.3V Suspend	In a T6,T10 system, Indicates that external battery is low. This port provides a battery-low signal to the Module for orderly transitioning to power saving or power cut-off ACPI modes. In a type 7 system, BATLOW# can be used as a power fail indication.
LID#	A103	I OD CMOS	3.3V Suspend/12V	PU 47KΩ to 3.3V Suspend	PU 47KΩ to 3.3V Suspend & isolate by Diode	LID switch. Low active signal used by the ACPI operating system for a LID switch.
SLEEP#	B103	I OD CMOS	3.3V Suspend/12V	PU 47KΩ to 3.3V Suspend	PU 47KΩ to 3.3V Suspend & isolate by Diode	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.

Rapid Shutdown Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe Module PU/PD	ICD970 PU/PD	Module Base Specification R3.0
RAPID_SHUTDOWN	C67	I CMOS	5.0V Suspend / 5.0V		PD 100KΩ to GND	Trigger for Rapid Shutdown. Must be driven to 5V though a <=50 ohm source impedance for ≥ 20 µs.

Thermal Protection Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe Module PU/PD	ICD970 PU/PD	Module Base Specification R3.0
THRM#	B35	I CMOS	3.3V / 3.3V		PU 10KΩ to 3.3V	Input from off-Module temp sensor indicating an over-temp situation.
THRMTRIP#	A35	O CMOS	3.3V / 3.3V		series 1G17 to BTB pin	Active low output indicating that the CPU has entered thermal shutdown.

SMBUS Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe Module PU/PD	ICD970 PU/PD	Module Base Specification R3.0
SMB_CK	B13	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	PU 2.2KΩ to 3.3V Suspend	System Management Bus bidirectional clock line.
SMB_DAT	B14	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	PU 2.2KΩ to 3.3V Suspend	System Management Bus bidirectional data line.
SMB_ALERT#	B15	I CMOS	3.3V Suspend/3.3V		PU 2.2KΩ to 3.3V Suspend	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.

GPIO Signals Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe Module PU/PD	ICD970 PU/PD	Module Base Specification R3.0
GPO0	A93	O CMOS	3.3V / 3.3V		RSVD PU 10KΩ to 3.3V Suspend	General purpose output pins. Upon a hardware reset, these outputs **should** be low.
GPO1	B54				RSVD PU 10KΩ to 3.3V Suspend	
GPO2	B57				RSVD PU 10KΩ to 3.3V Suspend	
GPO3	B63				RSVD PU 10KΩ to 3.3V Suspend	
GPI0	A54	I CMOS	3.3V / 3.3V		PU 47KΩ to 3.3V	General purpose input pins. Pulled high internally on the Module.
GPI1	A63				PU 47KΩ to 3.3V	
GPI2	A67				PU 47KΩ to 3.3V	
GPI3	A85				PU 47KΩ to 3.3V	

Power and GND Signal Descriptions						
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe Module PU/PD	ICD970 PU/PD	Module Base Specification R3.0
VCC_12V	A104~A109 B104~B109 C104~C109 D104~D109	Power				Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.
VCC_5V_SBY	B84~B87	Power				Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.
VCC_RTC	A47	Power				Real-time clock circuit-power input. Nominally +3.0V.
GND	A1, A11, A21, A31, A38, A41, A51, A57, A60, A66, A70, A73, A76, A79, A80, A83, A90, A100, A110, B1, B11, B21 ,B31, B38, B41, B51, B60, B70, B73, B76, B79, B80, B83, B90, B100, B110, C1, C2, C5, C8, C11, C14, C18, C21, C25, C28, C31, C41, C44, C48, C51, C60, C70, C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D18, D21, D25, D28, D31, D41, D44, D48, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Power				Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.

Module type Signal Descriptions

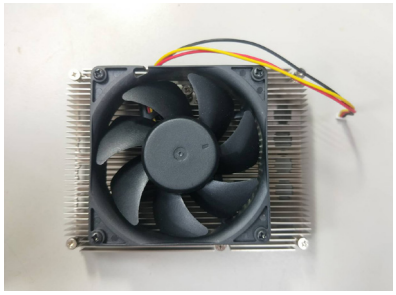
Signal	Pin#	Pin Type	Pwr Rail /Tolerance	COMe Module PU/PD	ICD970 PU/PD (T7)	Module Base Specification R3.0
TYPE0#	C54	PDS			PD 0Ω to GND	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module. The pins are tied on the Module to either ground (GND) or are no-connects (NC). For Pin-out Type 1 and Type 10, these pins are not present (X). TYPE2# TYPE1# TYPE0# X X X Pin-out Type 10, Pin out Type 1 (deprecated) NC NC NC Pin out Type 2 (deprecated) NC NC GND Pin out Type 3 (no IDE) (deprecated) NC GND NC Pin out Type 4 (no PCI) (deprecated) NC GND GND Pin out Type 5 (no IDE、PCI) (deprecated) GND NC NC Pin out Type 6 (no IDE, no PCI) GND NC GND Pin out Type 7 * The Carrier Board should implement combinatorial logic that monitors the Module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible Module pin out type is detected. The Carrier Board logic may also implement a fault indicator such as an LED.
TYPE1#	C57	PDS			N.C.	
TYPE2#	D57	PDS			PD 0Ω to GND	
TYPE10#	A97	PDS			N.C.	Dual use pin. Indicates to the Carrier Board that a Type 10 Module is installed. Indicates to the Carrier that a Rev 1.0 or a Rev 2.0/3.0 Module is installed. TYPE10# NC Pin-out R2.0 PD Pin-out Type 10 pull down to ground with 47K resistor 12V Pin-out R1.0 This pin is reclaimed from the VCC_12V pool. In R1.0 Modules this pin will connect to other VCC_12V pins. In R2.0 this pin is defined as a no connect for types 1-6. In R3.0 this pin is defined as a no connect for types 6 and 7. A Carrier can detect a R1.0 Module by the presence of 12V on this pin. R2.0 Module types 1-6 will no connect this pin. R3.0 Module types 6 and 7 will no connect this pin. Type 10 Modules shall pull this pin to ground through a 47K resistor.

▶ Cooling Option

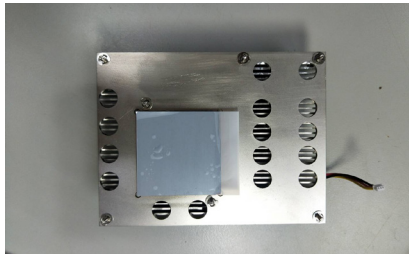
Heat Sink

The COM Express connector is used to interface the ICD970 COM Express board to a carrier board. Connect the COM Express connector (located on the solder side of the board) to the COM Express connector on the carrier board.

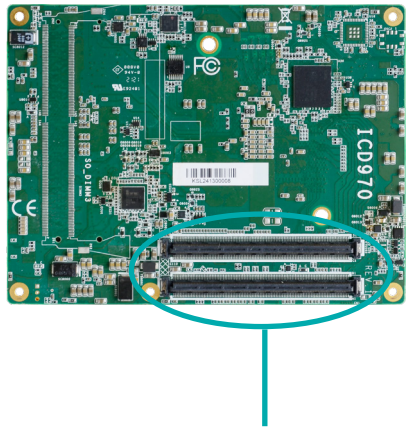
Important:
The carrier board (COM333) used in this section is for reference purpose only and may not resemble your carrier board. These illustrations are mainly to guide you on how to install ICD970 onto the carrier board of your choice. .



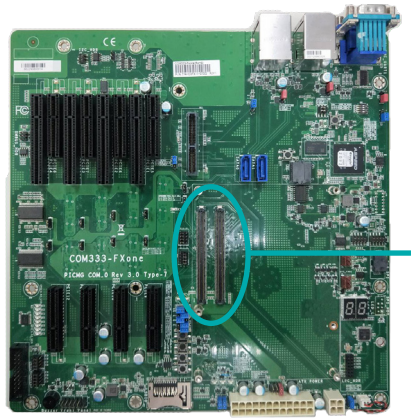
Top View of the Heat Sink



Bottom View of the Heat Sink



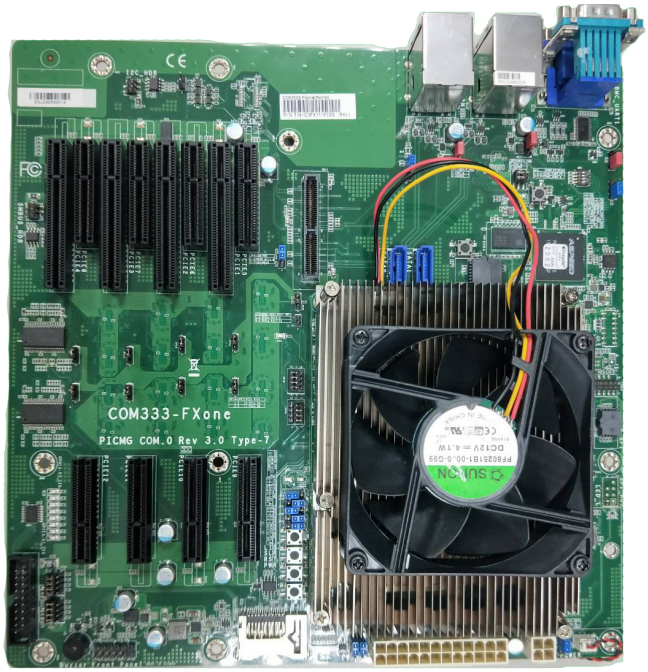
COM Express connector on ICD970



COM Express connector on the carrier board

Important:
Remove the plastic covering from the thermal pads prior to mounting the heat sink onto board.

2. Align the mounting holes of the heatsink with the mounting holes of the module. Use the provided mounting screws to install the heat sink onto the module.



Chapter 4 - BIOS Setup

▶ Overview

The BIOS is a program that takes care of the basic level of communication between the CPU and peripherals. It contains codes for various advanced features found in this system board. The BIOS allows you to configure the system and save the configuration in a battery-backed CMOS so that the data retains even when the power is off. In general, the information stored in the CMOS RAM of the EEPROM will stay unchanged unless a configuration change has been made such as a hard drive replaced or a device added.
It is possible that the CMOS battery will fail causing CMOS data loss. If this happens, you need to install a new CMOS battery and reconfigure the BIOS settings.

Note:
The BIOS is constantly updated to improve the performance of the system board; therefore the BIOS screens in this chapter may not appear the same as the actual one. These screens are for reference purpose only.

Default Configuration
Most of the configuration settings are either predefined according to the Load Optimal Defaults settings which are stored in the BIOS or are automatically detected and configured without requiring any actions. There are a few settings that you may need to change depending on your system configuration.

Entering the BIOS Setup Utility
The BIOS Setup Utility can only be operated from the keyboard and all commands are keyboard commands. The commands are available at the right side of each setup screen.
The BIOS Setup Utility does not require an operating system to run. After you power up the system, the BIOS message appears on the screen and the memory count begins. After the memory test, the message "Press DEL to run setup" will appear on the screen. If the message disappears before you respond, restart the system or press the "Reset" button. You may also restart the system by pressing the <Ctrl> <Alt> and <Del> keys simultaneously.

Legends

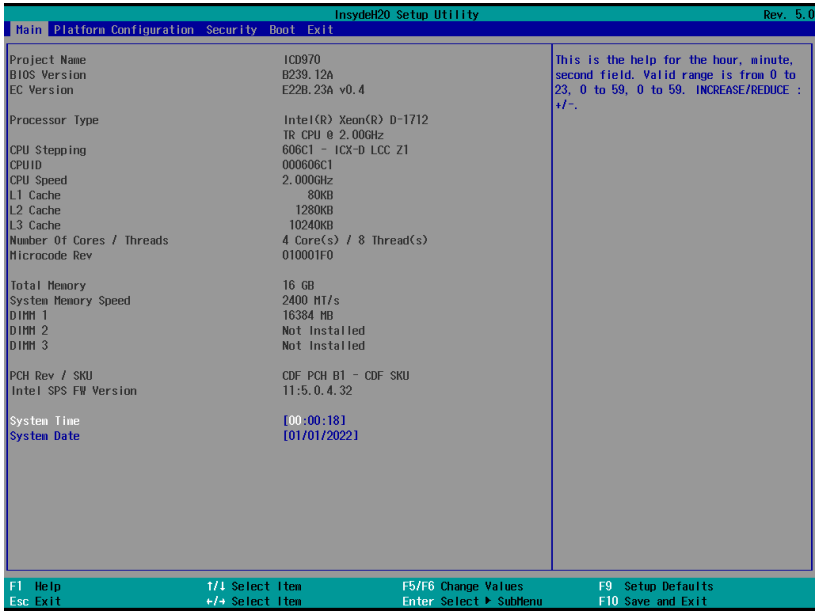
Keys	Function
Right / Left arrow	Move the highlight left or right to select a menu
Up / Down arrow	Move the highlight up or down between submenus or fields
<Enter>	Enter the highlighted submenu
+ (plus key)/F6	Scroll forward through the values or options of the highlighted field
- (minus key)/F5	Scroll backward through the values or options of the highlighted field
<F1>	Display general help
<F2>	Display previous values
<F7>	Popup Boot Device List
<F9>	Optimized defaults
<F10>	Save and Exit
<Esc>	Return to previous menu

Scroll Bar
When a scroll bar appears to the right of the setup screen, it indicates that there are more available fields not shown on the screen. Use the up and down arrow keys to scroll through all the available fields.

Submenu
When "▶" appears on the left of a particular field, it indicates that a submenu which contains additional options are available for that field. To display the submenu, move the highlight to that field and press <Enter>.

▶ Main

The Main menu is the first screen that you will see when you enter the BIOS Setup Utility.



System Date

The date format is <month>, <date>, <year>. Press "Tab" to switch to the next field and press "-" or "+" to modify the value.

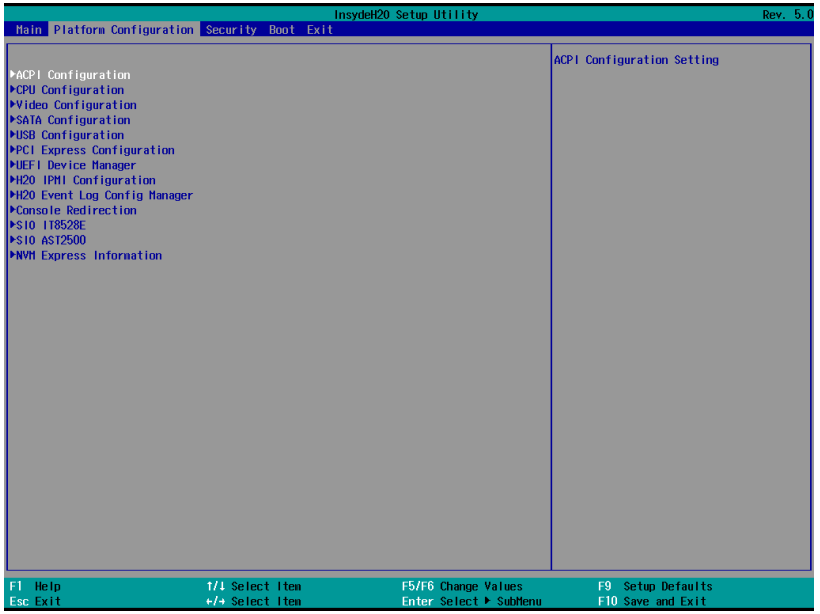
System Time

The time format is <hour>, <minute>, <second>. The time is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Hour displays hours from 00 to 23. Minute displays minutes from 00 to 59. Second displays seconds from 00 to 59.

▶ Advanced

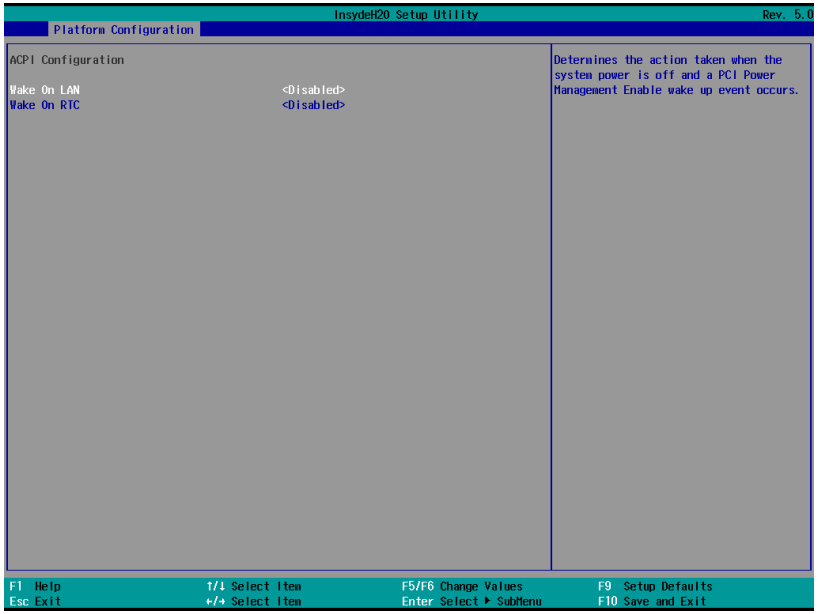
The Advanced menu allows you to configure your system for basic operation. Some entries are defaults required by the system board, while others, if enabled, will improve the performance of your system or let you set some features according to your preference.

Important:
Setting incorrect field values may cause the system to malfunction.



▶ Advanced

ACPI Configuration



Wake On LAN

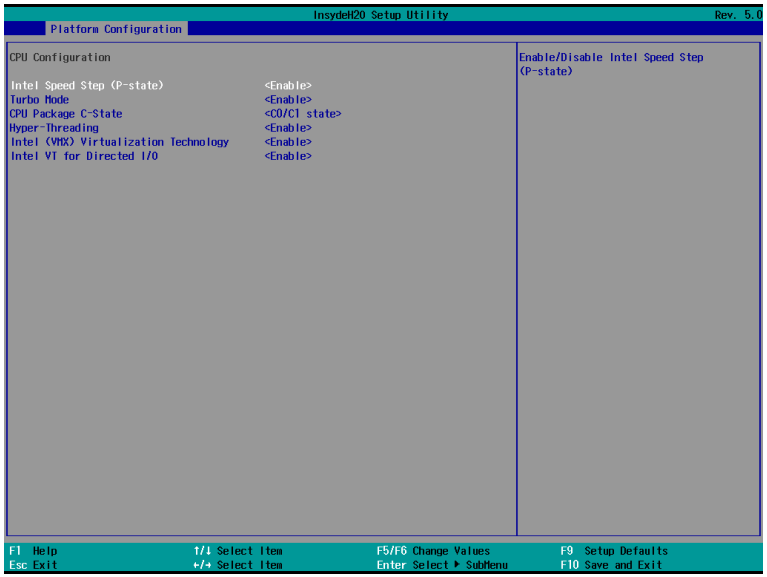
Enable or Disable this field to allow LAN signal to power up the system.

Wake On RTC

When Enabled, the system will automatically wake up from S4/S5 state at a designated time every day via the Real-time clock (RTC) battery.

▶ Advanced

CPU Configuration



Intel Speed Step

This field is used to enable or disable the Enhanced Intel SpeedStep® Technology (EIST), which helps optimize the balance between system's power consumption and performance. After it is enabled in the BIOS, EIST features can then be enabled via the operating system's power management.

Turbo Mode

Enable or disable turbo mode of the processor. This field will only be displayed when "Intel Speed Step" is enabled. This field is not available when CPU does not support Turbo Mode.

CPU Package C-State

Change CPU Package C-State limit among C0/C1, C2, C6, Auto.

Hyper-threading

Enable or disable Hyper-threading. When it is enabled, a physical core will perform as two logical processors, and the user may experience better computational efficiency of the system. This field is not available when the equipped CPU does not support Hyper-threading.

Intel VMX Virtualization Technology

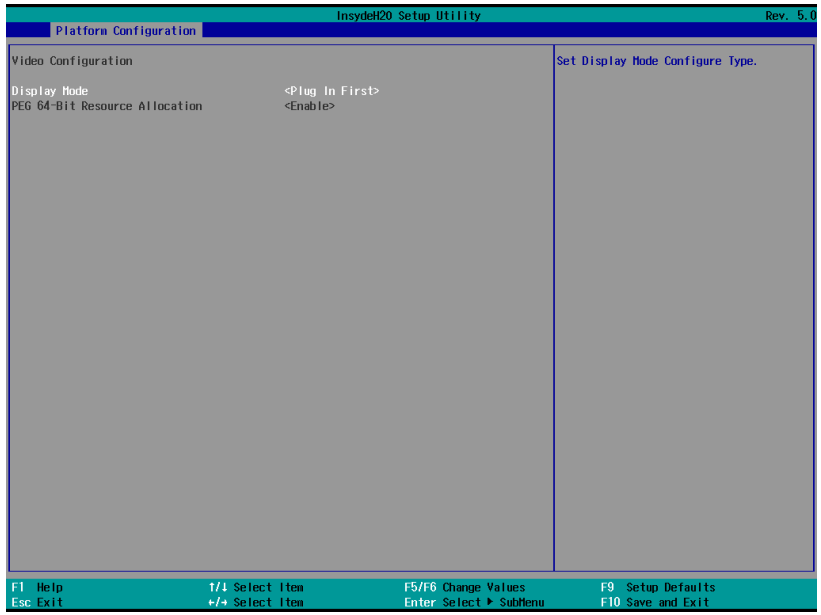
When this field is set to Enabled, the VMM can utilize the additional hardware capabilities provided by Vanderpool Technology

Intel VT for Directed I/O

Enable or disable Intel VT-d features.

▶ Advanced

Video Configuration



Display Mode

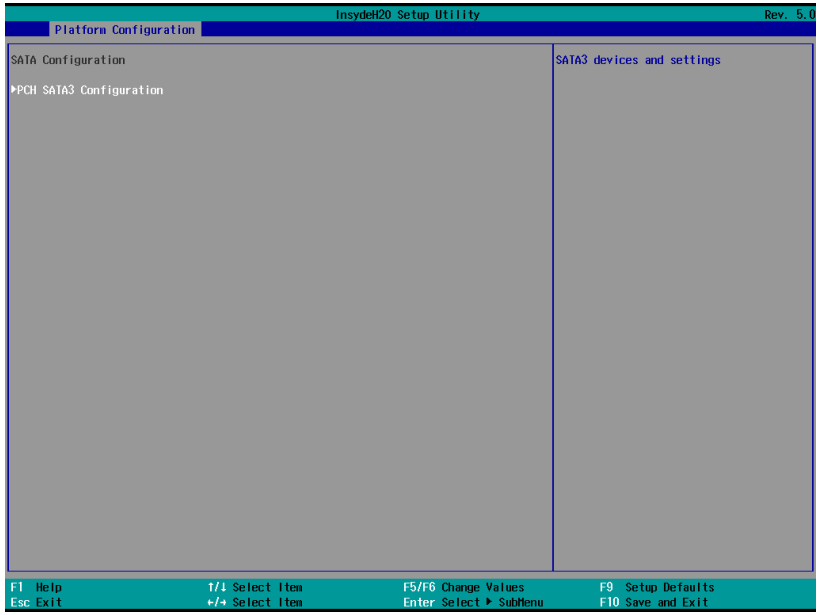
Select among On Board First and Plug In First to specify the display I/O source.

PCIE 64-bits MMIO decode

Select Enabled or Disabled to allocate MMIO resource of PCIE VGA card at 64-bits address. Enable it for specific VGA card that need huge resource. But it may cause VGA card to not display during boot in dual/legacy mode.

▶ Advanced

SATA Configuration

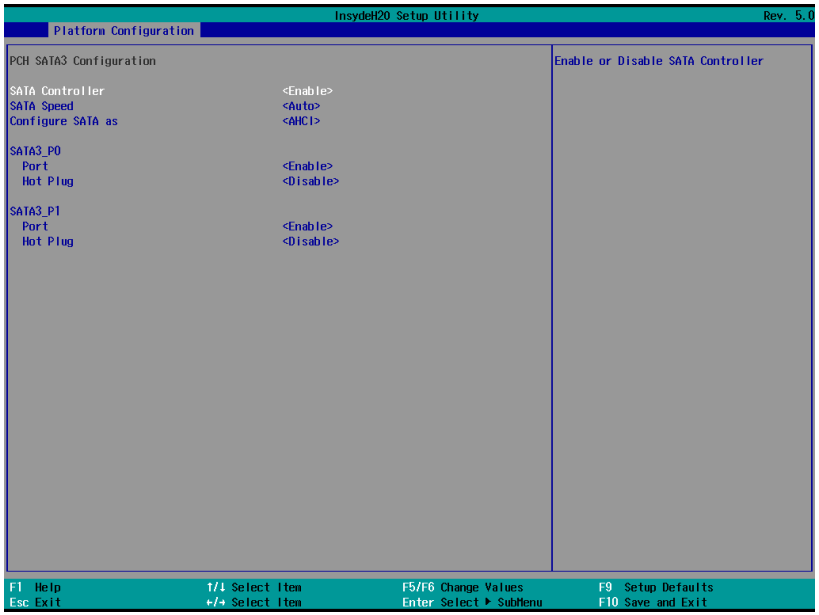


▶PCH SATA3 Configuration

SATA3 devices and settings.

▶ Advanced ▶ SATA Configuration

SATA Configuration▶PCH SATA3 Configuration



SATA Controller(s)

Enable or disable the Serial ATA controller. This following fields will only be displayed when this field is enabled.

SATA Speed

Select Serial ATA controller(s) speed — Auto, Gen1 (1.5 Gbit/s), Gen2 (3 Gbit/s) or Gen 3 (6 Gbit/s).

Configure SATA as

The mode selection determines how the SATA controller(s) operates.

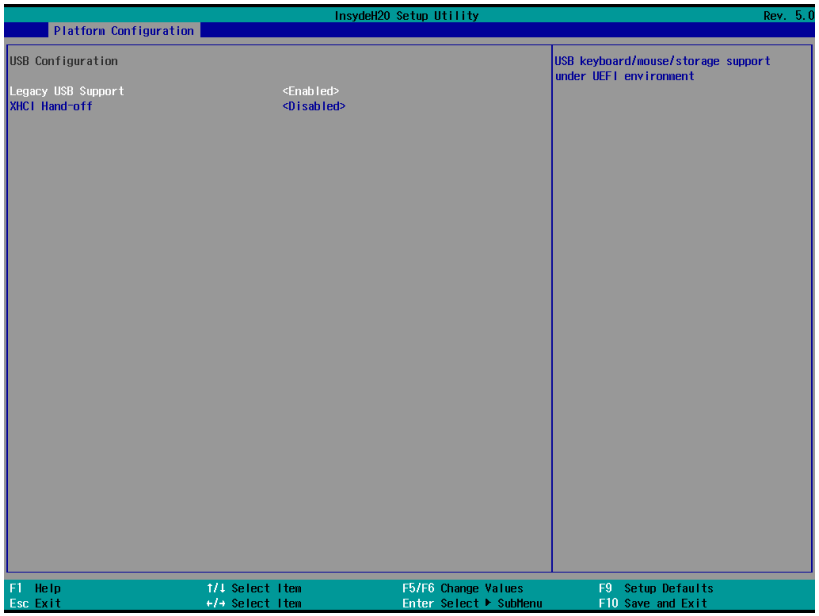
- **AHCI** This option allows the Serial ATA controller(s) to use AHCI (Advanced Host Controller Interface).

SATA3 Ports and Hot Plug

Enable or disable the Serial ATA port and its hot plug function.

▶ Advanced

USB Configuration



Legacy USB Support

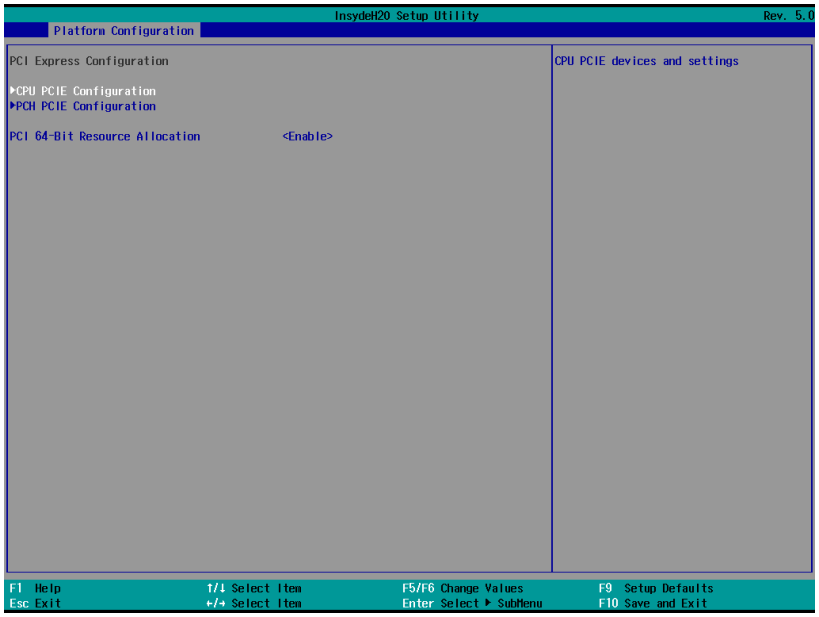
- **Enabled** Enable Legacy USB support.
- **Disabled** Keep USB devices available only for EFI applications.

XHCI Hand-off

Enable or disable XHCI Hand-off.

▶ Advanced

PCI Express Configuration



►CPU PCIE Configuration

Press Enter to enter the sub-menu and configure the PCIE ports — PCIE1, PCIE2, PCIE3, PCIE4.

►PCH PCIE Configuration

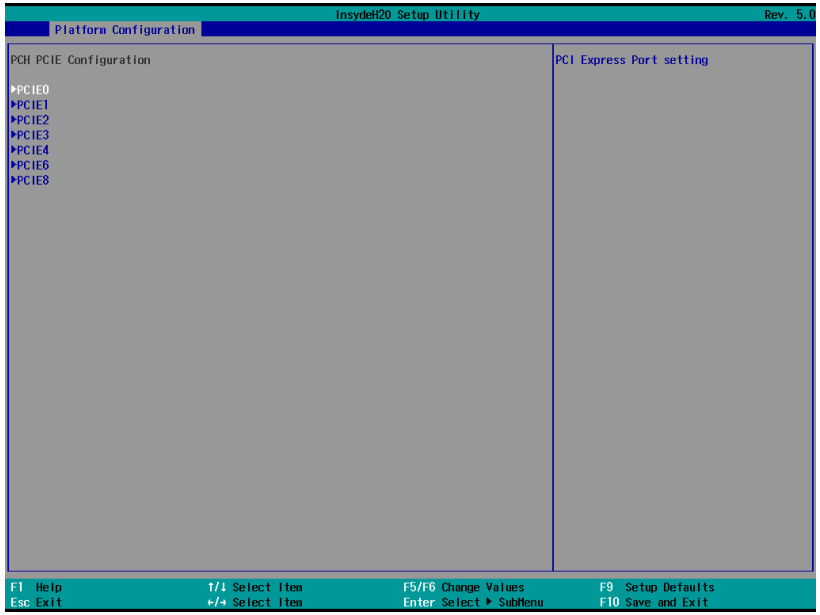
Press Enter to enter the sub-menu and configure the PCIE devices — LAN1, LAN2, and M.2 slot.

PCI 64-Bit Resource Allocation

Enable or disable the allocation of 64-bit resources for PCI.

▶ Advanced

PCI Express Configuration ► PCH PCIE Configuration



Select one of the PCI Express channels and press enter to configure the following settings.

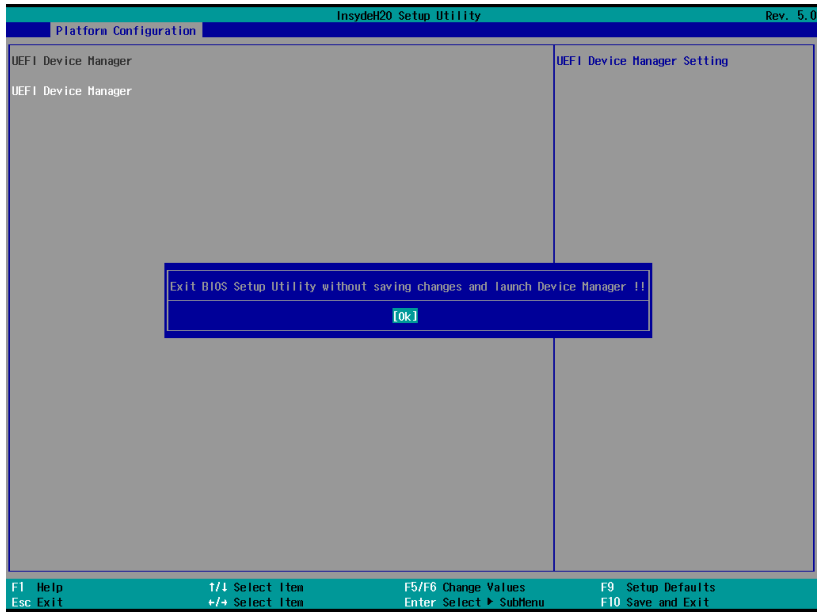
PCIE 0,1,2,3,4,6,8

Control the PCI Express Root Port.

▶ Advanced

UEFI Device Manager

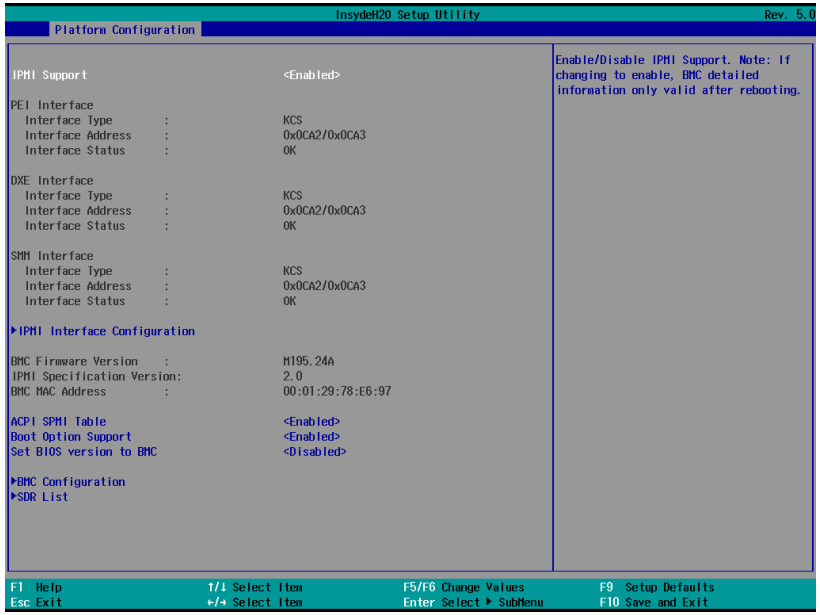
Configure UEFI device with option ROM, such as LAN card, etc.



Press “Enter” and “OK” to enter UEFI Device Manager setup page. More device settings can be configured in the UEFI Device Manager, including LAN, Network Stacks, and etc.

▶ Advanced

H2O IPMI Configuration



IPMI Support

Enable or disable the IPMI functions. When it is set to "Enable", BMC detailed information will only be valid after reboot.

IPMI Interface Configuration

IPMI Interface Configuration page. This page contains IPMI Interface realted settings.

ACPI SPMI Table

Enable or disable this field for IPMI driver installation.

Boot Option Support

Enable or disable IPMI boot option function.

BMC Configuration

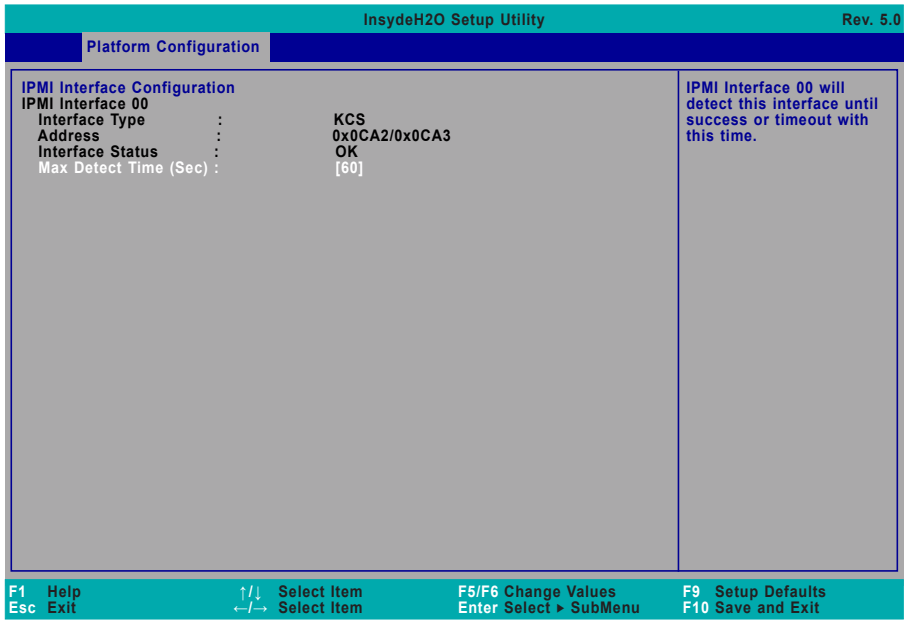
Configure the BMC's users in this sub-menu. The settings of all the 15 users are listed in the lower part of the sub-menu.

SDR List

Enable or disable the Sensor Data Record (SDR). All recorded information is listed in the lower part of the page.

▶ Advanced

H2O IPMI Configuration ▶ IPMI Interface Configuration

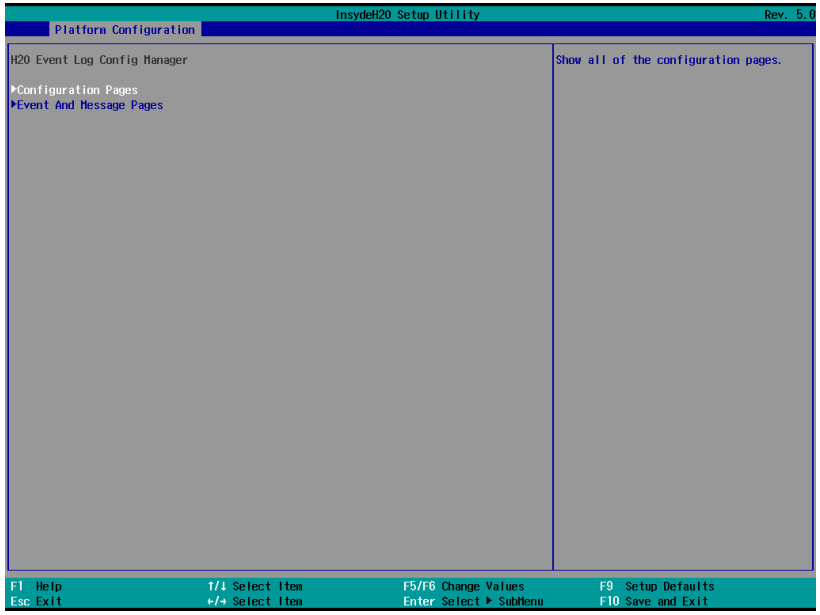


Max Detect Time (Sec)

IPMI Interface 00 will detect this interface until success or timeout with this time.

▶ Advanced

H2O Event Log Config Manager



Configuration Pages

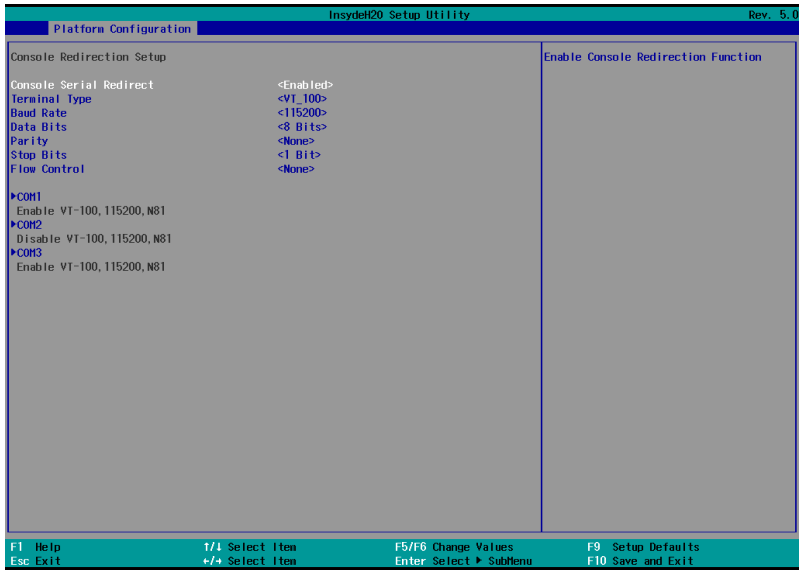
Show all of the configuration pages.

Event and Message Pages

Show all of the Event and Message pages.

▶ Advanced

Console Redirection



Console Serial Redirection

By enabling Console Redirection of a COM port, the sub-menu of console redirection settings will become available for configuration as detailed in the following.

Terminal Type

Select terminal type — VT_100, VT_100+, VT_UTF8 or PC_ANSI.

Baud Rate

Select baud rate — 115200, 57600, 38400, 19200, 9600, 4800, 2400 or 1200.

Data Bits

Select data bits — 7 bits or 8 bits.

Parity

Select parity bits — none, even or odd.

Stop Bits

Select stop bits — 1 bit or 2 bits.

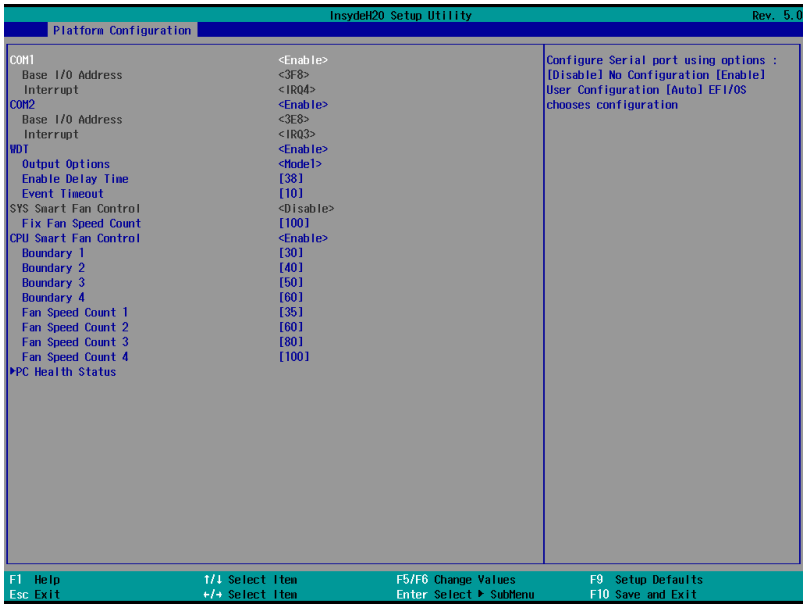
Flow Control

Select flow control type — none.

▶ Advanced

SIO IT8528E

View the super I/O settings in this submenu.



COM1~2

Configure Serial port using options:
[Disable] No Configuration
[Enable] User Configuration
[Auto] EFI/OS chooses configuration.

WDT

- **Output Options :** Mode1: Reset, Mode3: NMI
- **Enable Delay Time :** The delay time counter rangers from 1 to 255 seconds.
- **Event Timeout :** The event time-out counter rangers from 1 to 255, unit: 0.1 second.

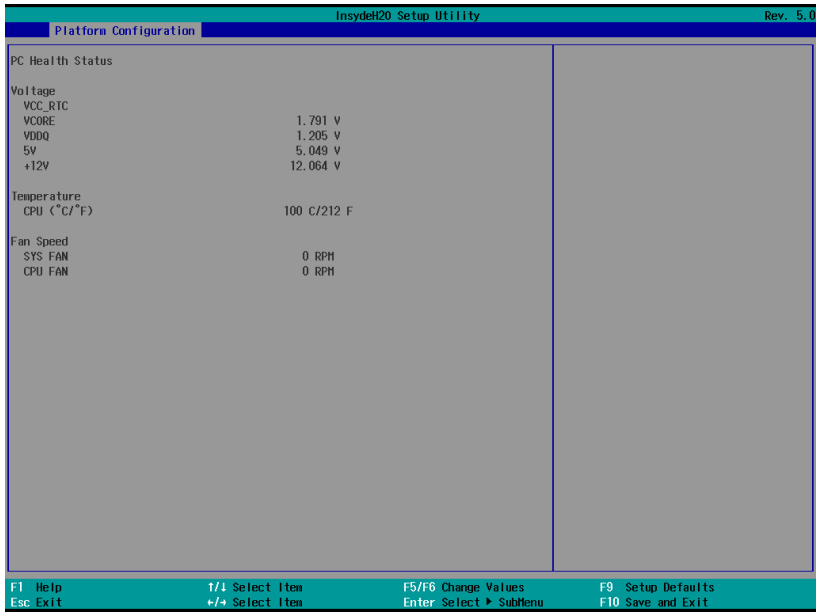
Fix Fan Speed Count

Fan Speed set from 1 -100%.

CPU Smart Fan Control

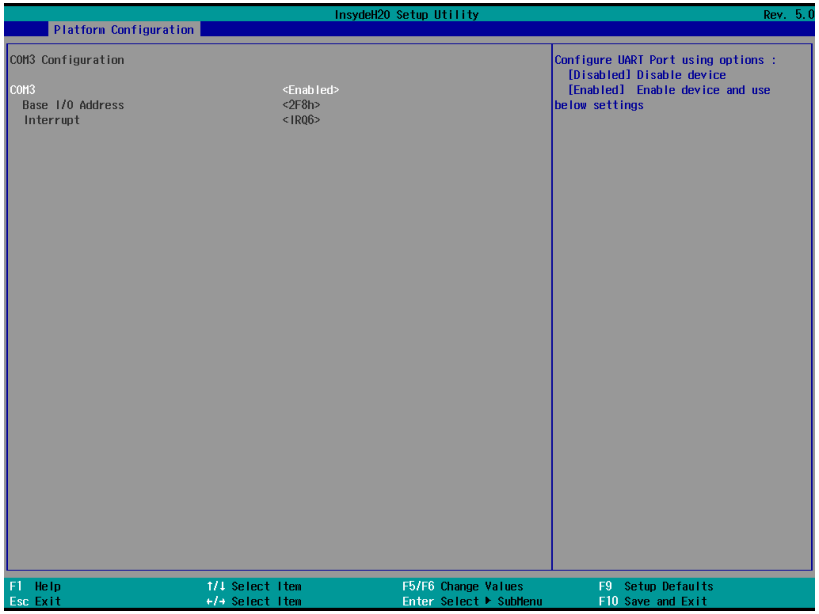
- **Boundary 1~4 :** Boundary Temperature set from 0-127°C
- **Fan Speed Count 1~4 :** Fan Speed set from 1-100%

SIO IT8528E ▶ PC Health Status



SIO AST2500

View the super I/O settings in this submenu.



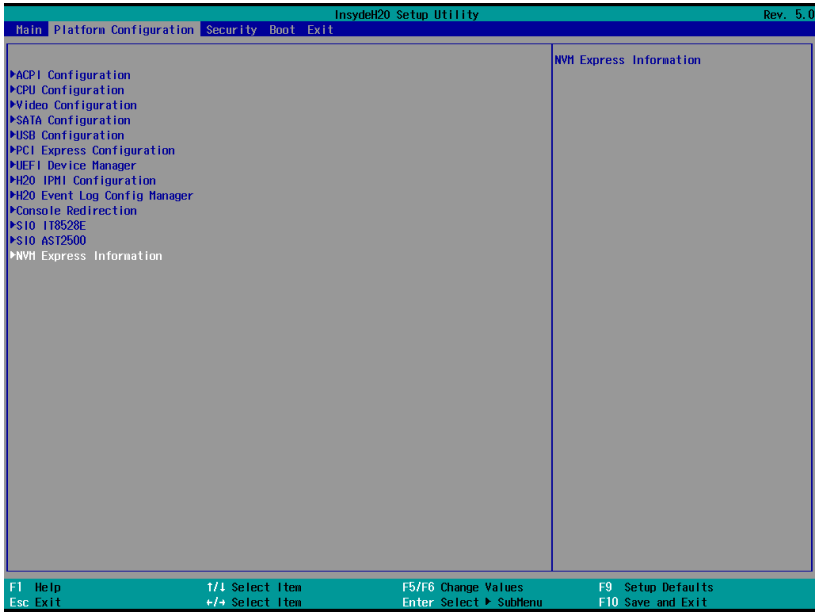
COM3 Configuration

Configure UART Port using options:
[Disable] Disable Device
[Enabled] Enabl device and use the settings

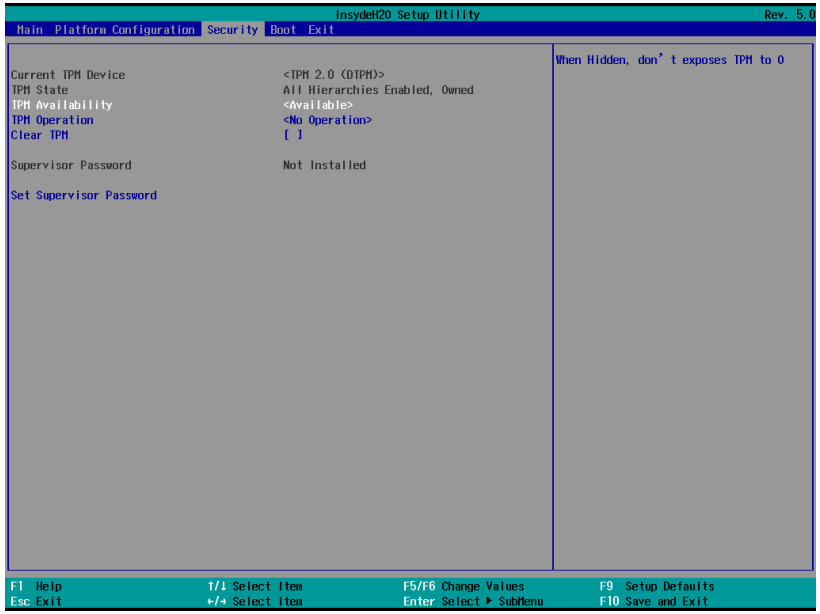
▶ Advanced

NVM Express Information

To show NVM Express information.



▶ Security



TPM Availability

Show or hide the TPM availability and its configurations.

TPM Operation

Select one of the supported operation to change TPM2 state — No Operation, Enable, or Disable.

Clear TPM

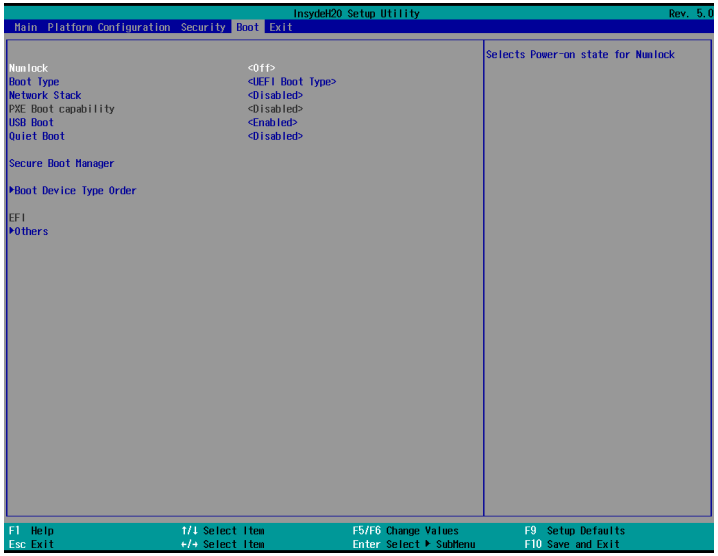
Remove all TPM context associated with a specific Owner.

Set Supervisor Password

Set the supervisor's password. The length of the password must be greater than one character.

Note:
The devices shown here are based on a carrier board that may not resemble your actual carrier board. The actual I/O devices depend entirely on those present on your actual carrier board.

▶ Boot



Numlock

Select the power-on state for numlock.

Boot Type

Select the boot type — UEFI Boot Type, Legacy Boot Type or Dual Boot Type. If you select “UEFI Boot Type” or “Dual Boot Type”, the “Network Stack”, “PXE Boot capability”, “USB Boot” and “Quiet Boot” will show up. If you select “Legacy Boot Type”, “PXE Boot to LAN”, “USB Boot” and

“Quiet Boot” will show up.

Network Stack

This field is used to enable or disable network stacks, i.e. IPv4 or IPv6 network protocols.

USB Boot

Disables or enables booting to USB boot devices.

Quiet Boot

Disables or enables booting in Text Mode.

Secure Boot Manager

Secure Boot Manager Setting.

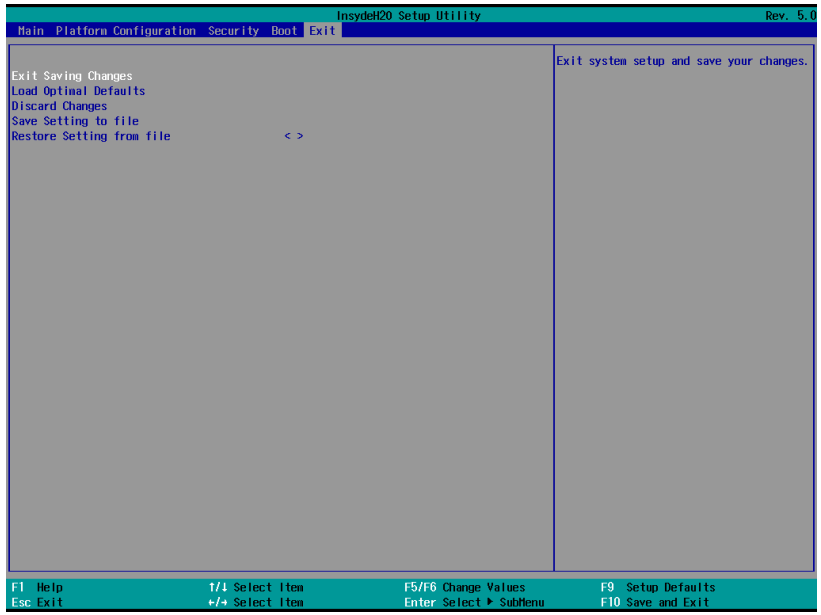
Boot Device Type Order

Change Boot Device Type Order.

Others

Change other device boot Order

▶ Exit



Exit Saving Changes

Select Yes and press <Enter> to exit the system setup and save your changes.

Load Optimal Defaults

Select YES and press <Enter> to load optimal defaults.

Discard Changes

Select YES and press <Enter> to exit the system setup without saving your changes.

Save Setting to file

Select this option to save BIOS configuration settings to a USB flash device.

Restore Setting from file

This field will appear only when a USB flash device is detected. Select this field to restore setting from the USB flash device.

▶ Updating the BIOS

To update the BIOS, you will need the new BIOS file and a flash utility. Please contact technical support or your sales representative for the files and specific instructions about how to update BIOS with the flash utility.

▶ Notice: BIOS SPI ROM

- 1. The Intel® Management Engine has already been integrated into this system board. Due to the safety concerns, the BIOS (SPI ROM) chip cannot be removed from this system board and used on another system board of the same model.
- 2. The BIOS (SPI ROM) on this system board must be the original equipment from the factory and cannot be used to replace one which has been utilized on other system boards.
- 3. If you do not follow the methods above, the Intel® Management Engine will not be updated and will cease to be effective.

Note:

a. You can take advantage of flash tools to update the default configuration of the BIOS (SPI ROM) to the latest version anytime.

b. When the BIOS IC needs to be replaced, you have to populate it properly onto the system board after the EEPROM programmer has been burned and follow the technical person's instructions to confirm that the MAC address should be burned or not.

Appendix A- Mapping Table List

▶ BTB PCIe Mapping Table List

Please refer to the following list of the mapping table list.

ICX-D LCC						ICD970 (BIOS)	PICMG COM.0 R3.0 Type-7 PCIE Lanes Mapping		Customer Carrier Board
CLKOU_SRC_DP/DN[1]							A88/A89	PCIE_CK_REF±	
Lanes NO.						Lanes	Bucket	Lanes NO.	
PCH HSIO Lane 0	PCIe Root Port Cluster 0	RP0 x8	RP0 x4	RP0 x2	x1	x2 (default)	B1	Lane 0	
PCH HSIO Lane 1								Lane 1	
PCH HSIO Lane 2				RP1 x2	x1	x2 (default)		Lane 2	
PCH HSIO Lane 3								Lane 3	
PCH HSIO Lane 4			RP2 x4	RP2 x2	x1	x2 (default)		Lane 4	
PCH HSIO Lane 5								Lane 5	
PCH HSIO Lane 6				RP3 x2	x1	x2 (default)		Lane 6	
PCH HSIO Lane 7								Lane 7	
PCH HSIO Lane 8	PCIe Root Port Cluster 1	RP4 x8	RP4 x4	RP4 x2	x1	x4 (default)	B2	Lane 8	
PCH HSIO Lane 9								Lane 9	
PCH HSIO Lane 10				RP5 x2	x1			Lane 10	
PCH HSIO Lane 11								Lane 11	
PCH HSIO Lane 12			RP6 x4	RP6 x2	x1	x4 (default)		Lane 12	
PCH HSIO Lane 13								Lane 13	
PCH HSIO Lane 14				RP7 x2	x1			Lane 14	
PCH HSIO Lane 15								Lane 15	
CLK_100M_G4PCIE_D0[P/N] (from external PCIe Gen4 clock)							B29/B30	G4_PCIe_CLK±	
Lanes NO.						Lanes	Bucket	Lanes NO.	
CPU HSIO Lane 0	RP_0a x16	RP_0a x8	RP_0a x4			x4 (default)	B3	Lane 16	
CPU HSIO Lane 1								Lane 17	
CPU HSIO Lane 2								Lane 18	
CPU HSIO Lane 3								Lane 19	
CPU HSIO Lane 4			RP_0b x4			x4 (default)		Lane 20	
CPU HSIO Lane 5								Lane 21	
CPU HSIO Lane 6								Lane 22	
CPU HSIO Lane 7								Lane 23	
CPU HSIO Lane 8		RP_0c x8	RP_0c x4			x4 (default)	B4	Lane 24	
CPU HSIO Lane 9								Lane 25	
CPU HSIO Lane 10								Lane 26	
CPU HSIO Lane 11								Lane 27	
CPU HSIO Lane 12			RP_0d x4			x4 (default)		Lane 28	
CPU HSIO Lane 13								Lane 29	
CPU HSIO Lane 14								Lane 30	
CPU HSIO Lane 15								Lane 31	
PCH HSIO Lane 16	PCIe Root Port Cluster 2	RP8 x8	RP8 x4	RP8 x2	x1	GbE_i210	1GbE_MDI		
PCH HSIO Lane 17						N.C.			
PCH HSIO Lane 18				RP9 x2	x1	SATA3_P0	SATA3	SATA3_P0	
PCH HSIO Lane 19						SATA3_P1		SATA3_P1	
PCH HSIO Lane 20			RP10 x4	RP10 x2	x1	USB3_P0	USB3	USB3_P0	
PCH HSIO Lane 21						USB3_P1		USB3_P1	
PCH HSIO Lane 22				RP11 x2	x1	USB3_P2		USB3_P2	
PCH HSIO Lane 23						USB3_P3		USB3_P3	
Qual0_Lan0		25G	40G	25G	10G	Q0_Lan0	10G KR	10G_P0	
Qual0_Lan1		25G			10G	Q0_Lan1		10G_P1	
Qual0_Lan2		25G		25G	10G	Q0_Lan2		10G_P2	
Qual0_Lan3		25G			10G	Q0_Lan3		10G_P3	